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Innovative and Expandable Physical Implementation Method for High-Speed Triple Modular Redundant Digital Integrated Circuits in Radiation-Hard Designs

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We present an innovative and expandable physical implementation method for high-speed Triple Modular Redundant (TMR) digital integrated circuits. The implementation uses a new interleaved placement approach in comparison to a generally used bulk 3-bank constraining method. To optimally constrain the placement of sequential cells as well as combinational cells. The TMR netlist information is used to divide the netlist into banks which do not interact logically and allow SEE charge sharing without compromising reliability. The technique was simulated in a 65 nm CMOS technology and resulted in a reduced total net length of 47 % dynamic power consumption of 25%.

Summary

It has been generally known that ionizing radiation can cause Single Event Effects (SEEs) in CMOS integrated circuits, particularly in scaled technologies. Generally, Triple Modular Redundancy (TMR) is used to overcome errors. Commonly TMR blocks are spaced sufficiently to avoid multi-cell upsets at the cost of difficult routing and increased power consumption. Another strategy for physical usage of TMR in high-speed digital circuits is presented in this paper. The design approach avoids long interconnections between voters by using interleaved placement constraints. A TMR fan-in tracing algorithm is utilized to partition the combinational logic in clusters (A, B, C) corresponding to triplicated branches. Ideally, every cell is guided with a spacing requirement to space them correctly, with maximum freedom. Nowadays such features are accessible in the most recent place-and-route releases. This can be utilized to guarantee the spacing distance between flip-flops, however, the spacing between the combinational logic cells cannot be ensured in the same way since the number of constraints would be too high. In moderate to complex data-paths, constraining flip-flops only is not sufficient.

In the proposed method, a floorplan is made using 6 physical constrain groups (A1, A2, B1, B2, C1, C2), or noted as ABC1 and ABC2. Each group A1-C2 has a height of the required spacing distance and occupies the entire width of the design. Vertically, all groups are subsequently repeated multiple times to fill the vertical design space (e.g. ⋯A1-A2-B1-B2-C1-C2-A1-A2 ⋯). A TMR datapath is placed in either ABC1 or ABC2. As such, one ABC group acts as spacers to each other. To ensure maximal area efficiency, TMR datapaths are balanced between ABC1 and ABC2 if they do not interact logically and thus are allowed to share multi-cell upsets.

The major advantage of this approach is that the place-and-route tool has more freedom to distribute logic across the floorplan. In contrast to the 3-blocks approach, interconnections between voters do not need to cross a big center block that results in major routing complexity and power consumption. With the proposed method, the total net length is drastically reduced since the connected logic can be placed closely together, still ensuring minimal spacing for SEEs. As a consequence, the switching power is also reduced, as a result of the reduction in the total net length. For the tested circuits, the total net length reduced by up to 47% while the switching power consumption is reduced by 25%. Furthermore, the routing complexity was significantly simplified compared to a bulk 3-block physical floorplan. By using the placement balancing between ABC1 and ABC2, there is no area penalty.

Primary authors: APPELS, Karel (KU Leuven Association); KULIS, Szymon (CERN); PRINZIE, Jeffrey (KU Leuven)

Presenter: VAN BOCKEL, Bjorn

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