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## Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments

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The KINTEX-7 FPGA is to be used in the new digital readout of the upgraded LHCb-RICH sub-detectors. This summary presents the measurements done to evaluate the reliability of this FPGA under ionizing radiation exposure with different types of particle beams: ions, protons and X-rays. Single-event effect cross-sections for critical resources - such as Flip-Flops, RAM blocks, configuration memory, and I/O blocks - have been evaluated for multiple values of total ionizing dose, linear energy transfer, proton energy, and particle flux. A list of firmware constrains for this RICH application was deduced based on extrapolation to upgraded LHCb and 50 fb<sup>-1</sup>.

### Summary

Following the Long Shutdown 2 of the LHC, the LHCb single arm forward spectrometer will be upgraded to operate at higher luminosity and at a higher trigger rate. The LHCb-RICH sub-detectors were redesigned to allow operation for higher HEH fluence –close to 1012 cm<sup>-2</sup>. Multi-anode photomultiplier tubes (MaPMTs) are RICH photodetectors and the triggered signals from their frontend electronics are read by DAQ through dedicated digital boards controlled by a KINTEX-7 FPGA. These FPGAs are widely used in high energy physics experiments due to their lower price and high logic density. Due to the large integrated dose - 200 krad (Si) total ionising dose (TID) - it was needed to qualify the viability of KINTEX-7 when operating in the LHCb-RICH environment. Several test beams with different particle were used: ions at the LNL in Italy and at the Cyclotron Resource Centre in Louvain Belgium; 200 MeV protons at the Paul Scherrer Institute from Switzerland and 35 MeV protons at the Nuclear Physics Institute in Juelich Germany; and an X-ray facility from the University of Padova.

Different firmware versions have been designed to test individual FPGA critical resources: user Flip-Flops, block RAM, configuration memory and the I/O blocks. Mitigation techniques were included in each of the firmware versions: triple modular redundancy (TMR) architectures for user Flip-Flops, and Soft Error Mitigation IP Core to detect and correct errors in configuration memory. To monitor and control the FPGA test board, a custom DAQ system has been designed.

Using ions, within a broad range of linear energy transfer (LET) from  $1.3 \pm 0.26$  to  $32.4 \pm 6.48$  MeV cm<sup>2</sup>/mg, the FPGA was tested for single-event effects. Attention was given to the single-event latch-ups and single event upsets (SEUs) in user Flip-Flops and configuration memory. The threshold for SEUs in the configuration memory has been found to be below 1.3, though we estimate it is very close to this value.

The proton beam test was used to estimate the possible TID or other cumulative effects, as well as for proton-induced single-event effects in FPGA resources. SEU cross-section ( $\sigma$ ) values of order of 10<sup>-7</sup> cm<sup>2</sup>/device have been extracted for the configuration memory and the BRAM blocks. This device has been proven resilient against TID up to 1 Mrad (Si). The X-Ray beam test confirmed the TID effect absence in this device.

Several failures have been seen in the I/O blocks, induced either by ions or protons. The cross-section for 35 MeV proton-induced I/O failures has been found to be lower than 10<sup>-11</sup> cm<sup>2</sup>/device.

We give qualitative conclusions and cross-section values for each critical resource tested, as function of total ionizing dose, proton energy and LET. As an example, we extrapolate these testing results for an LHCb-RICH system with thousands of FPGAs, operating in the first Phase of an LHCb Upgraded detector with 50 fb<sup>-1</sup> integrated luminosity.

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