SEU test of 110 nm CMOS UMC technology

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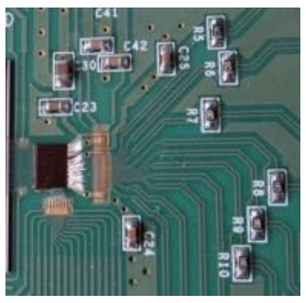
SEU TEST using the CHANNEL CONFIGURATION REGISTERS of PASTA , FIRST PROTOTYPE of the READOUT ELECTRONICS of the SILICON STRIP DETECTOR of PANDA



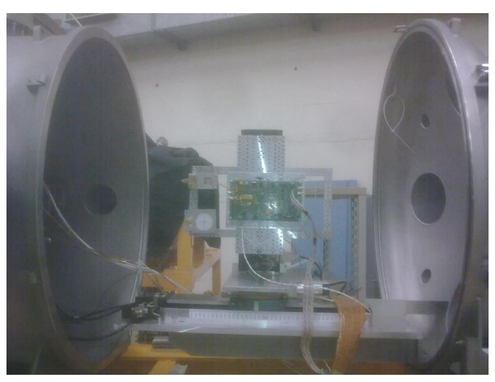
Testing board with PASTA

- PASTA ASIC developed by JLU Giessen, FZ Juelich and INFN Torino
- Chip developed in 110 nm UMC technology
- Challenging requests on power dissipation (≈ 4mW/ch) and size (4.5 x 3.2 mm^2)
- 64 channels, nominal clock frequency of 160 MHz
- ToT measurements, 8 bit (dyn. range) charge resolution
- Radiation tolerant circuits to Single Event Upset (SEU) effects are implemented
- **TMR (Triple Modular Redundancy) technique for registers just 1 bit long**
- **Hamming Encoding for registers longer than 1 bit**
- **Channel configuration word 42 bits long (13 bits with TMR and 8 registers with Hamming Encoding for a total of 29 bits)**

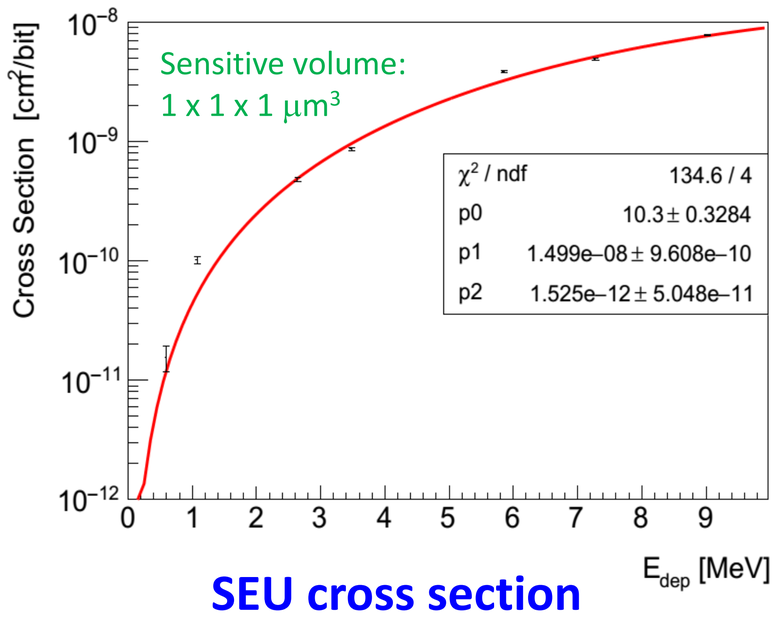
TEST with ION BEAMS @ SIRAD FACILITY in the LABORATORIO NAZIONALE di LEGNARO – INFN (ITALY)

- **DAQ based on LABView and VIRTEX 6 FPGA**
- **Balanced sequence of 1 and 0 is used to configure the channel configuration register of each channel** (TMR: 5 bits set to 1, 8 bits to 0; Hamming Encoding: 12 bits set to 1, 17 bits to 0)
- The **procedure to detect SEU** events foresees:
  - a writing command to configure the ASIC
  - a reading phase till a SEU is detected
  - the SEU event is registered
  - the sequence starts again from a new writing command
- The **DAQ program counts the number of times when a bit changes its value** and writes it to the output file

- D.U.T. is placed in the vacuum chamber
- Long cables limit clock frequency to 50 MHz
- 7 different type of ions were used to evaluate the SEU cross section of the chip under test (2688 bits for the 64 channels)



Ion	E [MeV]
C	87.66
O	95.40
Si	141.61
Cl	162.66
Ni	190.81
Br	218.91
Ag	247.04



SEU cross section in hadronic environment
Σ : 3.6 · 10^{-16} cm^2 /bit
(following the procedure described in ref: M. Huhtinen and F. Faccio, NIMA 450 (2000))

TEST with PROTON BEAM @ the EXPERIMENTAL ROOM of INFN-TIFPA in the PROTON-THERAPY CENTRE of TRENTO (ITALY)

- D.U.T. is placed in front of the beam line exit
- Short cables allow to perform measurements at the nominal clock frequency of 160 MHz
- To compare information to the results obtained at LNL, additional measurements with 50MHz clock frequency were performed
- Proton beam energy : 131.3 MeV
- Beam current up to 300 nA

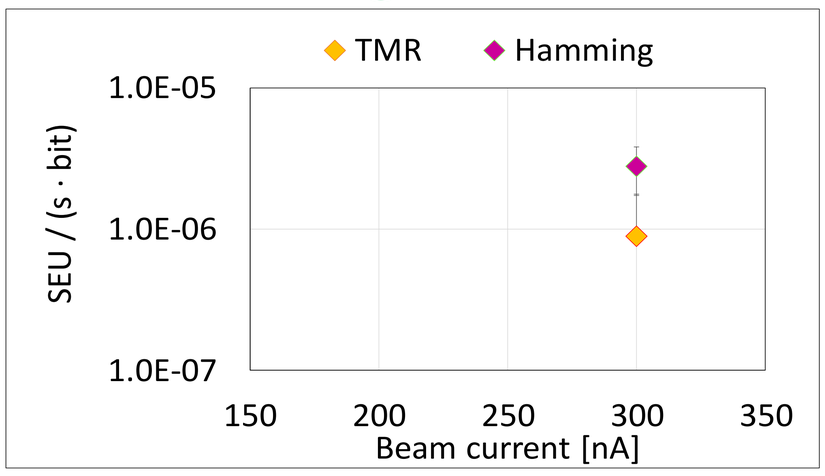
Beam current [nA]		
100	200	300
Proton flux on the chip [p/s] (10% of error)		
2.8 · 10^8	5.5 · 10^8	7.8 · 10^8
-	50 MHz	50 MHz
160 MHz	160 MHz	-

COMPARISON of RESULTS obtained with IONS and PROTONS

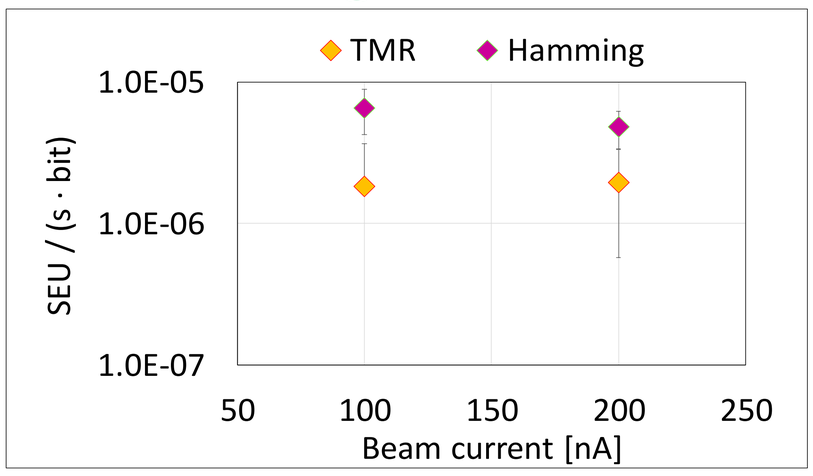
@ 7.8 · 10^8 p/s on the chip

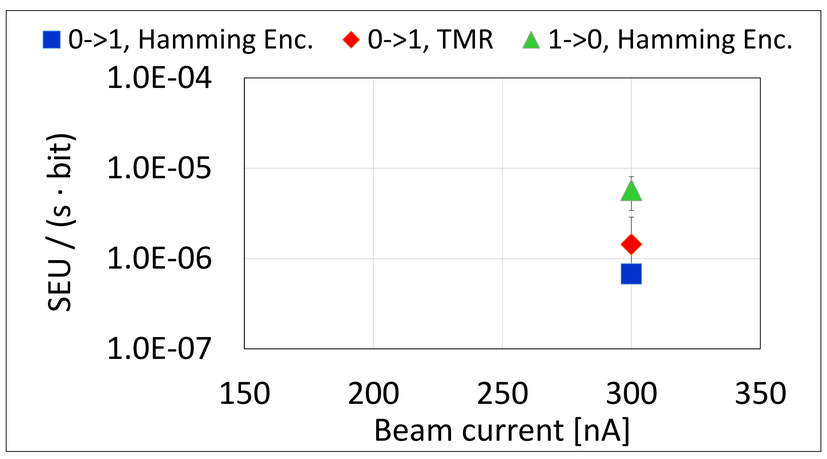
- proton test → direct measurement
  2.19 · 10^{-6} SEU/(s·bit)
- ion test → using evaluated Σ
  2.26 · 10^{-6} SEU/(s·bit)

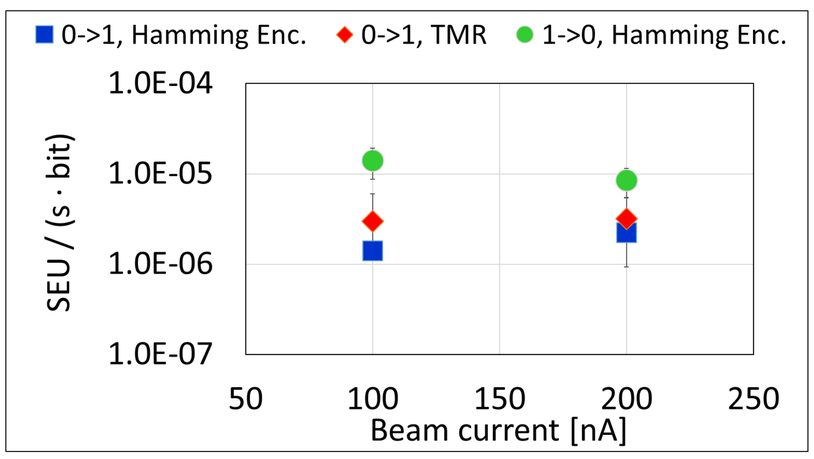
Clock @ 50 MHz



Clock @ 160 MHz







- The number of SEUs for all the bits with TMR (and for registers with Hamming Encoding) increases with the beam intensity since at 200 nA no SEUs were detected
- Bits protected with TMR are more tolerant with respect to bits of registers implementing Hamming Encoding for 1→0 flip event; vice-versa for 0→1 events

- The number of SEUs for all the bits of registers with Hamming Encoding decreases in the range of tested beam intensity. In the case of TMR, the SEUs number is stable.
- Bits protected with TMR are more tolerant with respect to bits of registers using Hamming Encoding for 1→0 flip event; vice-versa for 0→1 events