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A multi-channel trigger and acquisition board for TDC-based readout: application to the cosmic rays detector of the PolarQuEEEst 2018 project.

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In the 2018 summer the PolarQuEEEst experiment accomplished a measurement
of cosmic rays flux in the Arctic. The detector, installed on a sailboat, was based on
scintillation tiles read by a total of 16 SiPM.
A multi-channel board (called TRB) has been designed to process the discriminated SiPM signals providing self-trigger capability and
time-to-digital conversion. It was based on a Cyclone-V Intel FPGA. TDC
conversion has been implemented in FPGA and in a HPTDC chip (as a backup). The board will be described, main
features and performance will be enlightened and, lastly, future
improvements and potential application will be discussed.

Summary

The PolarQuEEEst 2018 expedition have been accomplished in the last summer: a sailboat that circumnavigated the Svalbard archipelago was equipped with specific instrumentation in order to perform a set of scientific measurements in the Arctic region. In particular, a cosmic rays detector have been designed to properly run in those harsh environmental condition so as to measure flux at the sea level beyond the 70°N lat. The detector was based on
scintillation tiles read by a total of 16 SiPM, each of them is digitized by applying discrimination over a programmable thresholds. Signals are sent, as LVDS standard, to a FPGA-based custom board aimed to self-triggering and event readout purposes, which is called TRB. The trigger logic is configurable and implemented within the FPGA. The trigger signal is used as a reference for time-to-digital conversion of both leading and trailing edges of the 16 inputs, thus measuring time-over-threshold. TDC conversion is implemented both into FPGA and with Cern HPTDC chip. The latter was initially foreseen as a backup solution in case of either excessive power consuption or high FPGA resources utilization. Afterwards, because of the satisfactory operation of the TDC into FPGA, HPTDC has been kept to profit from for calibration and redundancy purposes during the expedition as well. TRB is interfaced to GPS navigation system to provide precise time stamp of the events. Trigger, TDC and GPS information are packed in formatted event and sent to a commercial RaspPI3+ single board computer, aimed to data recording, TRB configuration and detector monitoring using a set of sensors (pressure, humidity, temperaure, position, etc...). Main hardware elements are: the Cyclone V Intel FPGA, the piggy board hosting the HPTDC, the off-the-shelf piggy board to interface the RaspPi3+ via USB.
In this document we are going to describe the hardware, major highlights of the FPGA firmware, performances achieved by the system and future possible improvements.
Three features can be outlined as example. First, the FPGA TDC sensitivity which has been restricted to about 30 ps by or-ing 4 delay steps together and that can be pushed over if needed. Second, the sustainable output data rate, now limited at 60 Mbit/s by the USB connection with the RaspPi3+ that

can be increased by implementing on firmware the already foreseen high-speed transceiver port, runnign at a maximum of about 6 Gb/s. Last, the number of available input channels in this first TRB version are 32, common to FPGA and HPTDC (only 16 implemented in the FPGA firmware so far); In a future PCB version channel number could be increased by distinguish among readout-only channels (via HPTDC) and the ones that should provide self-triggering too (via FPGA).

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