First IpGBT-based prototype of the End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade

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On behalf of the EoS team
ATLAS ITk Upgrade

• High Luminosity LHC (HL-LHC) will be a very challenging environment for ATLAS

• Inner tracker (ITk) will be replaced by an all-new, upgraded silicon tracker
  – Better resolution, larger coverage, less material
  – ~60 millions channels. Almost ten times the current system!
  – ATLAS-TDR-025
End of Substructure (EoS) card

- Act as the interface between on- and off-detector components
  - Handle data, command, and power delivery
  - Also host NTC thermistor for temperature interlock system

- Sit on the "ear/nose" of stave and petal
  - Far away from the other EoS on a different stave/petal as much as possible

- If broken, stave/petal will be lost
  - Need to be reliable!
EoS Card

- Radiation-hard active components from CERN:
  - Low-power Gigabit Transceiver (lpGBT) ASIC
    - 65nm, integrated slow-control features
  - Bi-directional optical link (VL+)
    - Much smaller footprint
  - DCDC convertor (BPOL12 and BPOL2.5)

- Multi-layer board using industry-standard PCB technology.
  - Nominal thickness 1.6 mm, maximum 1.8 mm
  - Total height after population < 5 mm (constrain from detector design/assembly)

- Two variants called the “Master” and the “Slave”
  - Glued to each side of the mechanical structure (see next slide)
  - Mostly independent electrically. Limited losses in case of failure
  - 1.27mm pitch inter-connector between them for a few signals and high voltage traces
  - 1 or 2 lpGBT each and a VL+ each

- Master will house the thick components
  - Mechanical interface to external fiber
  - DCDC converters (details in a few slide)

- Flex lead in PCB for HV and monitor signals
EoS Card

Master EoS:
Housing all thick components like DCDC and optical interface

Keep the slave thin for clearance

1 or 2 IpGBT each and a VL+ each
Some part of the detector need higher resolution → more bandwidth

Flexible connection to service ring with connector to PP0 either on master (petal) or slave (stave)

Connector for master-slave interconnect

Carbon fiber of substructure
A master and a slave board are glued on each side
DCDC Convertor

- From 11V input, need 2.5V and 1.2V for IpGBT and VL+
- Use CERN designs:
  - 11V → 2.5V: bPOL12v
  - 2.5V → 1.2V: bPOL2v5
- The coils and shielding boxes made the DCDC convertor too thick to be on the same 1.6mm PCB with the rest of the EoS
- The EoS design has a cutout for the DCDC convertor board
- DCDC layout is based on a similar part from module power board and CERN PCB for bPOL2V5
  - Designed by the team at Niels Bohr Institute, University of Copenhagen
  - The first test will be done separately from the EoS
GBTx-based Prototype

Quick Recap
EoS Prototype

- Built GBTx-based prototypes to learn about implementing the hardware and software
Test Result Summary

• Functionality tests – all good
  – ✔ All ELinks and clocks signals
  – ✔ Both high (HV) and low (LV) voltage lines
  – ✔ Slow control
    • ✔ Internal control (Read/write GBTx registers)
    • ✔ External control (Operate GBT-SCA)

• Flatness: slightly higher in the middle after population, but within spec

• Thermal: PCB is a good heat spreader. No problem with cooling

• Bit error rate test (BERT): already better than aimed $<10^{-12}$
  – Full data path, like the real setup
  – Up to 70h error-free

• EoS with Real Stave: it works!
  – Put together by the team at Rutherford
IpGBT-based Prototype

The First Working Implementation Outside CERN
IpGBT/VL+ based Prototype

- First IpGBT and VL+ received mid-April
- First populated board tested in May
- Working firmware shortly after
- Dual IpGBT version in June
- A master prototype tested together with the first barrel substructure
Test Firmware

- Firmware running on Xilinx kc705 board
  - Put together from CERN's lpGBT-FPGA modules with some modifications
  - Slow-control IP core from GBT-SC project, with our own bug fixes
  - 160 MHz reference clock. Can be generated on the board or provided externally

- Include bit error rate test (BERT) functionality
- Connect to PC via UART-USB interface
**Functionality Tests**

- Configure both the first and second IpGBT to operational ("Idle") state
  - Operate the IpGBT #1’s I²C master to config the IpGBT #2
- Optical link established; Tx/Rx locked
- No problem with preliminary test on the HV line
- All signal lines on both IpGBTs
  - External Control (EC) line
- Two uplinks and the downlink on the VL+
- Read/write registers via optical link (IC line)
• Eye diagram does not look great, but most likely due to our equipment and setup
ELink Rx

- All Rx ELinks checked out at 640 Mbps
  - Also at the right bits in the frame received on the FPGA!

1 MHz, 20% duty cycle input

Group 6 link 2 @ 640 Mbps
ELink Tx/Clock Signal

- All Tx ELinks checked out
  - Also at the right bits in the frame sent from the FPGA!
  - 160 Mbps for general ELinks
  - 80 Mbps for the external control (EC) line to the AMAC

- 320 MHz Bunch clock
  - Not very pretty currently, but should improve with better test setup and equipment

CMD0 signal line. Sending 0111 @ 40 MHz.

BC0 line @ 320 MHz.
Bit Error Rate Test

- **Preliminary setup**
  - Expect better result with proper connections
- **Full data path in both directions**
  - FPGA <-> Optical link <-> EoS <-> ELink
- **Test ELinks on both IpGBTs**
BERT Results

- Only ELink #0 in the group
- Time: 6 h, 0 m, 5.8533623 s
- Number of packets: $8.6 \times 10^{11}$
- Two types of error:
  - FEC field indicates that the package need correction
  - Actual bit mismatch
- Not quite the aimed $<10^{-12}$
  - Should improve with better setup
  - Our firmware stored the last good and the error packages for debugging purpose

<table>
<thead>
<tr>
<th>IpGBT</th>
<th>Direction</th>
<th>Error Type</th>
<th>#Error</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>Uplink</td>
<td>FEC</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>#1</td>
<td>Uplink</td>
<td>Bit</td>
<td>2</td>
<td>$1.45 \times 10^{-13}$</td>
</tr>
<tr>
<td>#2</td>
<td>Uplink</td>
<td>FEC</td>
<td>432</td>
<td>$\sim 1.95 \times 10^{-12}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5.00 x $10^{-10}$ if we discard the whole package</td>
</tr>
<tr>
<td>#2</td>
<td>Uplink</td>
<td>Bit</td>
<td>8</td>
<td>$5.79 \times 10^{-13}$</td>
</tr>
<tr>
<td>#1</td>
<td>Downlink</td>
<td>Bit</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Action Items

• Power up and config the lpGBT without I\(^2\)C line
  – Need to burn minimum config to E-fuse
  – We identified the 5 registers needed to bring up the optical link and procedure to E-fuse
    • [https://lpqbt-support.web.cern.ch/t/e-fusing-procedure/99](https://lpqbt-support.web.cern.ch/t/e-fusing-procedure/99)
  – Our firmware is ready

• Improve test setup
  – Needle prober in the near future

• Perform the rest of the tests planned:
  – Thermal
  – Flatness
  – Noise on power line
    • DESY summer student has done a set of test on our old GBTx prototype, with good results so far
  – Etc.

• Combine test with DCDC prototype
Summary

- We built IpGBT/VL+ based EoS
- Our designs work! Including the dual-IpGBT version!!
- Developed a test firmware
  - Config and control both IpGBTs
  - BERT functionality included
- Functionality tests all ok
- Preliminary BERT results are promising
  - Investigating the FEC error. Better setup should help
- Will proceed with the rest of the test planned
- Moving steadily toward production

Thank you
Backup
Test Setup

- The basic setup are:
  - EoS board
  - FPGA board (currently Xilinx KC705)
  - PC
  - USB-I\textsuperscript{2}C for configuring the GBTx (preliminary setup only)
    - To be replaced by IC via optical line

- We developed the firmware for the FPGA board based on the GBT-FPGA project from CERN

- We wrote a software on PC to control the testing on FPGA board

- Standalone instead of full ATLAS DAQ system
  - Good enough for our needs
  - Simpler to develop and debug.
  - Can be ready as soon as we have the boards and not rely on other developments
Firmware
Test Result (So Far)

- All Tx Elinks checked out
  - Also at the right bits in the frame sent from the FPGA!
  - 80 Mbps for the external control (EC) line to the AMAC
Test Plan

- EoS sits on a single point of failure for a large part of the detector => need to be well-tested

Future Plan

PCB Manufacture
- Connectivity
- Optical test of trace width, surface, etc.
- Measurement of test strips (resistivity/impedance)

DESY Production – Unpopulated board
- Resistivity, Impedance
- Optical Inspection:
  - Trace width
  - Missing pads
- X-ray/Destructive solder ball test
- Optical Inspection:
  - Assembly
  - Traces
  - Outer row of BGAs
- Impedance and current measurements

DESY Production – Populated board
- Mechanics
- Current consumption
- Initialization
- Infrared imagine
- Temperature test
- HV line test
  - 1.5 kV for 60s

DESY ATLAS – Pre test
- LV/HV line resistor
- Current consumption @ Boot/Init/Min/Typical/Max of supply voltage
- Reset procedure
- Clock/Control/Data signal
- I²C Bus/ADC/DAC/GPIO
- NTC
- Bit error rate
- Robustness/Variation
- Noise on power line

DESY ATLAS – Full test
- Resistivity, Impedance
- Optical Inspection:
  - Trace width
  - Missing pads
- X-ray/Destructive solder ball test
- Optical Inspection:
  - Assembly
  - Traces
  - Outer row of BGAs
- Impedance and current measurements
Optical Link Clock Recovery

Wish module for clock recovery from data stream, not jitter between

320MHz is more like a sine-wave bad for timing jitter

Adding many uninteresting phase jitters

EoS