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# Integration, Commissioning and First Experience of ALICE ITS Control and Readout Electronics

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For the third running period of the CERN LHC, the ALICE experiment will undertake several upgrades of its sub-detectors. One of the detectors to be upgraded is the Inner Tracking System, featuring the new ALPIDE pixel chip. Control and readout of the 24120 chips are handled by 192 custom FPGA-based readout units. Each readout unit can forward 9.6Gbps of data to another custom PCIe card that aggregates the data from several units and transmits it for further offline/online analysis. Integration and commissioning of the system is underway and this paper describes the first experiences and results of this effort.

## Summary

During the ongoing Long Shutdown 2 of the CERN LHC, the ALICE experiment will replace the existing Inner Tracking System (ITS), which is based on silicon strip sensors, silicon drift sensors and silicon hybrid pixel sensors, with a completely new detector based on Monolithic Active Pixel Sensor (MAPS) technology. 24120 ALPIDE pixel sensors are mounted onto 192 azimuthally overlapping staves arranged into seven coaxial cylinders of increasing diameters, providing improved tracking and event-rate capability compared to the previous detector. The cylinders are separated into inner and outer barrel, consisting of three and four cylinders, respectively. The aim of the upgrade is to be able to handle 50 kHz Pb–Pb interaction rate and 200 kHz pp interaction rate. However, the current design is aimed at achieving double the rate for Pb–Pb and 1 MHz for pp.
Trigger distribution, readout, control, power management, and monitoring (voltages, currents, and temperatures) of the sensors is handled by 192 custom FPGA-based Readout Units (RUs) based on a Xilinx UltraScale FPGA, one per stave. The RU can operate both in triggered and continuous readout mode,
whereas in continuous mode the RU generates the triggers to the sensors internally. Three optical transceivers, each supporting a maximum throughput of 3.2 Gbps, connects each RU to the Common Readout Unit (CRU) hosted in the First Level Processor (FLP). Each FLP can host up to four CRUs and each CRU can receive data from up to eight RUs.
Assembly of the detector, both inner and outer barrel, is well advanced and the commissioning of the complete readout chain, with all final systems, has started. This paper will present the performance of the full system in terms of readout-rate capabilities in both triggered and continuous readout mode under different running conditions: at low detector occupancy and high rates, simulating running with pp interactions at rates up to 1 MHz, and at high occupancy

and low rates, simulating Pb–Pb minimum bias collisions at rates up to 100 kHz.

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