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The OBDT board: A prototype for the Phase 2 Drift Tubes on detector electronics

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We present here the design and performance of the OBDT board, which is the new prototype built to substitute the CMS DT muon on-detector electronics. The OBDT is responsible of the time digitization of the DT signals, allowing further tracking and triggering of the barrel muons. It is also in charge of the slow control tasks of the DT chamber systems. A prototype of this board has been produced and is being tested both in the laboratory and also in test stands with real DT chambers. The full functionality in real conditions is being evaluated, showing very satisfactorily results.

Summary

The on-detector electronics of the CMS (Compact Muon Solenoid) DT (Drift Tubes) chambers will need to be replaced for the HL-LHC (High Luminosity Large Hadron Collider) operation due to the increase of occupancy and trigger rates in the detector, which cannot be sustained by present system. The OBDT (On Board Electronics for DT) is the new prototype of the electronics that will be attached to the DT chamber, inside the CMS volume. It will be in charge of performing the 1 ns time digitization of the DT chamber signals and the multiplexing for further transmission to the readout and trigger backend electronics. This board is also in charge of the slow control tasks needed by the full DT chamber system.

The OBDT board has been built around a Microsemi Polarfire FPGA which is responsible of the time digitization of up to 240 input signals. It implements a deserialization method which runs at a clock frequency of 600 MHz and allows obtaining a time bin of 0.833 ns. The input data is multiplexed according to certain criteria and forwarded to the output optical link for data transmission to the readout and trigger chains. This prototype of the OBDT board contains two different optical link bidirectional chains. One that goes to a QSFP+ transceiver to the gigabit transceiver embedded on the Microsemi FPGA and is used mainly for outputting the timing data from the OBDT to the backend system. The protocol implemented so far follows the GBT protocol. Another optical link goes through a SFP+ transceiver to the GBTx chip in the OBDT board and is in charge of performing the slow control tasks, serving also as a backup transmission protocol.

The GBTx chip plus a SCA chip in the board allow clock and synchronization reception as well as e-link implementation for the configuration and monitoring of the Microsemi FPGA. Through this link it is also possible to implement the different slow control functionality of the barrel system, such as setting the front end discriminators thresholds and bias values, implementation of the I2C links for temperature monitoring and channel masking, communication to the RPC and Alignment slow control chains and finally, implementation of the test pulse generation mechanisms that allows to perform the DT chamber time measurements calibration.

A prototype of this board has been produced and is being tested both in the laboratory and also in different test stands with real DT chambers. The different functionality of the OBDT board has been verified and the overall architecture has been validated both through specific tests and through cosmics ray data-taking integrated with the rest of the DT systems. The OBDT architecture together with its performance results will be presented in this contribution, showing the goodness of the design for the expected functionality during HL-LHC.

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