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Commissioning High-speed readout for the LHCb VELO Upgrade

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The new LHCb Vertex Locator for LHCb, comprising a new pixel detector and readout electronics will be installed in 2020 for data-taking in Run 3 at the LHC. The electronics centre around the “VeloPix” ASIC at the front-end operating in a triggerless readout at 40 MHz. Custom serialisers send zero-suppressed data from the VeloPix at a line rate of 5.13 Gb/s. Signal integrity tests of the data path components showing characteristic impedance and jitter measurements will be presented. System tests of the complete electronic and optical chain, along with early results from the VELO module production sites will be shown.

Summary

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s/ASIC and produce an output data rate of over 15 Gb/s, and totalling 2.85 Tb/s of data for the 40M pixels of the whole VELO.

This paper will present an overview of VELO front-end and back-end electronics, with an emphasis on tests of the high speed transmission. The detector consists of 208 tiles of 3 VeloPix flip chipped to a silicon sensor surrounding the beam as close as 5 mm in a secondary vacuum tank and extremely high and inhomogeneous radiation environment.

The VeloPix transmits zero suppressed, time-stamped, unsorted packets with binary hit information over 5.13 Gb/s links. The VELO detector opens during LHC beam injection, to prevent damage from the unstable beams. To facilitate movement, the high speed links are implemented with low mass, flexible data tapes. Signals are driven out of the vacuum chamber through a Vacuum Feed-through Board (VFB) and subsequently converted from electrical to optical in the Opto-Power Board (OPB). 300 metre optical links originating at the OPB drive the data from the LHCb cavern to the PCIe40 back-end data acquisition boards in the surface, where they are recovered, synchronized, sorted, packed and sent in real time to the CPU farm to be further processed.

As the project enters its early production phase, several full system integration tests have been performed to qualify the modules for production. Signal integrity (eye diagram, S-parameters, characteristic impedance, BER) of the different parts of the readout chain (hybrids, flexible data tapes, VFB, OPB) has been controlled. The DAQ system was tested using three full-scale prototype modules in a beam test in November 2018. Results of the readout performance and synchronisation between the modules will be shown.

Some of the latest test results include:

- Jitter measurements of the VeloPix output links have been performed and show a relation to VeloPix serialiser PLL phase. We scan the phases to find the optimal minimum bit-error rate ($<1e-14$). These scans are supplemented with eye diagrams at the end of the electronic readout chain.
- An equalisation procedure is used to tune the analogue parameters of the VeloPix. Extra noise on odd columns of the VeloPix matrix have been identified during this procedure. An alternative calibration method, using the high speed output links, and not suffering this extra noise will be shown.

A full readout chain slice of the detector has been qualified prior to the electronics module production. New results are expected of these high rate scans at the nominal operating temperature of the detector at -30C.

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