The upgraded readout electronics of the CMS ECAL: system overview

Simona Cometti on behalf of CMS collaboration
High Luminosity LHC

HL-LHC main objective: deliver a much larger dataset for physics to the LHC experiments

- New physics searches
- Higgs boson coupling measurements
- Precision tests of the standard model

Goals:
- Peak luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ after 2026
- Integrated luminosity of 250 fb$^{-1}$ per year
The upgrade is needed to retain the CMS ECAL performance during HL-LHC:

- Higher luminosity and increased data rates
- Good detector performance in the harsh radiation environment
- Higher average level of pileup events
- Higher fraction of anomalous APD signals ("spikes") → rejection

**EB electronics: principal requirements:**

- CMS Level-1 trigger latency: **12.5 μs** (currently: 3.4 μs)
- CMS Level-1 trigger rate: up to **750 kHz** (currently 100 kHz)
The legacy readout system will not be able to satisfy the new requirements in terms of **bandwidth** and **latency**.
Legacy vs upgraded on-detector readout

- **Multi-gain pre-amplifier (MPGA):**
  - Charge sensitive amplifier
  - 3 outputs, gain values: \(x1, x6\) and \(x12\)

- **Multi-channel ADC:**
  - ADC resolution: **12-bit**
  - ADC sampling frequency: **40 MS/s**
  - Selection unit

- **Front-End card:**
  - Data pipeline
  - Trigger primitives generation
  - Trigger data granularity: 5x5 crystals

- **CATIA ASIC:**
  - Trans-impedance Amplifier (TIA) architecture
  - 2 outputs, gain values: \(x1\) and \(x10\)

- **LiTE-DTU ASIC:**
  - ADC resolution: **12-bit**
  - ADC sampling frequency: **160 MS/s**
  - Selection and compression unit

- **New Front-End card:**
  - Fast rad-hard optical links to stream crystal data off-detector through CERN lpGBT/VL
  - Trigger data granularity: crystal level
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TWEPP 2019

Simona Cometti
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CATIA ASIC

- Technology: CMOS 130 nm
- Input stage: Regulated Common-Gate (RCG) Trans-Impedance Amplifier (TIA)
- Full dynamic range splitted in two sub-ranges:
  - Gain x10 differential amplifier: 10 MeV – 200 GeV
  - Gain x1 differential amplifier: 10 MeV – 2 TeV
- $V_{CM} = 0.6 \text{ V} \pm 0.6 \text{ V}$
- Radiation tolerance validation

- Integrity of APD signal shape
- anomalous signal rejection
- Internal 5-bit DAC for output pedestal tuning
- Temperature sensor
- I²C interface for slow control

CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade

Olivier Gevin
**CATIA ASIC**

**CATIA v0 (2016): Demonstrator**
- TIA part integration with the two gains in a single-ended output version
- Optimization of the TIA dynamic range
- Full characterization with detector and radiation test

**CATIA v1 (2018): Validator**
- Two differential voltage
- 5-bits DAC is used for output pedestal tuning
- Test with detector and radiation test
- Target: System test with commercial ADC
  System test with LiTE-DTU ASIC

**Final CATIA**: submission foreseen in 2020
- Target: System test with Lite-DTU and lpGBT
  Radiation hardness of VFE board
CATIA ASIC – beam test results

- One ECAL tower (25 channels) equipped with CATIA v1 chip and 160 MHz commercial ADC
- **Electron beam**, energy range: **25 - 250 GeV**
- Setup kept at 18 °C (current ECAL operating temperature)

**Energy resolution matches legacy electronics**

**Time resolution matches targets**

- Good time resolution to improve pileup mitigation and spike rejection
LiTE-DTU ASIC

- Technology: CMOS 65 nm
- Die size: 2 x 2 mm²
- 63 pads
- Radiation tolerance validation
  - TID tolerance up to 100 kGy
  - SEU-protected control logic

- 2 ADC IP blocks
- Data compression and transmission unit: DTU
- I²C interface
- Phase Locked Loop (inherited from lpGBT project)
- Synchronization unit
ADC IP block

- Designed by an external company with experience in design of high resolution, high sampling rate converters
- Successive approximation architecture
- Resolution: **12-bit** at Nyqvist frequency
- Sampling rate: **160 MS/s**
- Input common mode: 600 mV
- Input voltage swing: 600 mV
- Must withstand up to total ionizing dose of 100 kGy
- Single event upset protected control logic
Data Transmission Unit architecture - selection

Baseline subtraction unit
Two 8-bit registers

Sample selection unit
Look-ahead algorithm: sample saturation check prevents the mixing of samples from different gains in the same APD signal
Data Transmission Unit architecture - compression

Online lossless data compression

Simplified Huffman encoding: compression based on the statistical distribution of the input values

32-bit words data packet generation

Direct connections between LiTE-DTU and lpGBT e-links

- LiTE-DTU rate: 13-bit words @ 160 MHz → 2.08 Gb/s
- lpGBT e-link rate: 1.28 Gb/s
- LiTE-DTU rate after compression → 1.08 Gb/s
Data Transmission Unit architecture - transmission

Frame generation and trailer insertion

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1101</td>
<td># Samples (8 bits)</td>
</tr>
<tr>
<td>1112</td>
<td>CRC 12</td>
</tr>
<tr>
<td>1112</td>
<td>Frame ID (8 bits)</td>
</tr>
</tbody>
</table>

Packet synchronization and IDLE words insertion

- **32-bit data storage FIFO**: packet rate variation compensation (intrinsic to the compression process)
- Idle packet transmission when storage FIFO is empty

<table>
<thead>
<tr>
<th>Code</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110</td>
<td>1010101010101010101010101010</td>
</tr>
</tbody>
</table>

High speed serial data transmission

Output data stream transmitted at 1.28 Gb/s
LiTE-DTU – ongoing test and future work

PLL test
• Clock quality qualification

ADC test
• ADC performance tests and radiation tolerance test

Full ASIC test
• Selection and compression algorithms validation
• Full ASIC radiation tolerance test

System test
• Test of the LiTE-DTU connected with CATIA ASIC
New Front-End card prototype

Streaming of digitized data generated on the VFE cards to the CMS ECAL back-end electronics system

Initialization and control of all VFE components

Precise clock distribution to all the VFE cards

- 4 uplinks at 10.24 Gb/s (data links)
- 1 downlink at 2.56 Gb/s (control link)
- eLink serial interface to ADC, clock, and i²C interface

**v1 demonstrator:**
- 5 Gb/s links, GBTx based
- 1 VTRx + 2 VTTx VL modules

**Future work:**

**v2 validator:** using 10 Gb/s links

**v3 prototype:** fine tuning and bug fixes
VICE ++ card

VICE ++: VFE Interface Converting Electronics

The board is designed to provide all data, clock, and control signals for VFE and FE prototypes

Useful for evaluating VFE, FE and FE-BE systems as well as for data-taking under test-beams → **VICE++ can emulate:**

- most of the functionalities of the VFE and FE card prototypes
- large fraction of the on-detector electronics functionality for the upgrade off-detector electronics
Barrel Calorimeter Processor

- Receive LHC clock and distribute to on-detector electronics
- Handle slow-control of the on-detector electronics
- Transmit to the Level-1 trigger a pre-processed set of trigger primitives
- Buffer and transmit data to CMS DAQ after Level-1 accept signal (single crystal granularity)
- Receive, decompress and analyze data
- Reject the anomalous APD signals (spikes)

v1 demonstrator:
1 FPGA and many test functions
Design being finalized
Summary

The **HL-LHC** phase will bring **exciting** opportunities for precision measurements and new physics searches. But the challenging conditions foreseen the HL-LHC will require:

- Longer data pipeline, more bandwidth
- Improved spike rejection at trigger level
- Mitigation of increased APD noise
- Precision timing for vertex determination and pile-up mitigation

**Action foreseen:**

- Replace/optimize VFE and FE to cope with increased noise, pileup, spikes
- Precise timing for electrons and photons
- New off-detector readout cards to process higher granularity/bandwidth
- Move all algorithms off-detector

**With this Phase-2 upgrade, the CMS ECAL barrel will continue its excellent performance throughout HL-LHC**
Backup slide
APD spikes vs scintillation signals

- The APD pulses from spikes have a **faster rise time** and **shorter duration** than scintillation pulses
- APD spikes arise from **direct ionization in the silicon** rather than the **de-excitation of electrons** from excited states which is responsible for scintillation

- The legacy preamplifier used CR-RC shaping which made the spike and scintillation pulses very similar and **limited the ability to discriminate** between the two
- The proposed TIA has a very **fast response** and a **short shaping time**, which preserves the **spike discrimination** and significantly enhances the timing resolution
ADC IP block

- Successive approximation architecture
- Resolution: 12-bit at Nyqvist frequency
- Sampling rate: 160 MS/s
- Input common mode: 600 mV
- Input voltage swing: 600 mV
- Foreground calibration
- Two clocks:
  - main clock: 1.28 GHz
  - sampling clock: 160 MHz
- Maximum total ionizing dose of 100 kGy
- Single event upset protected control logic
- ADC LSB: 488 MeV (gain x1 channel)
- ADC LSB: 48.8 MeV (gain x10 channel)
Fault tolerant strategies

- **CRC-12 codification:**
  - error detection and correction for the 32-bit encoded words
  - polynomial generator: $g(x) = x^{12} + x^{11} + x^3 + x^2 + x + 1$
  - last updated CRC-12 is inserted in the frame trailer by CU

- **Hamming code:**
  - 6 Hamming bit cover each 32-bit data packet stored in the FIFO

- **Triple Modular Redundancy:**
  - applied to registers and finite state machines of LiTE-DTU sub-systems

- **Spatial separation:**
  - between triplicated entities in order to avoid radiation-induced errors on more than one entity copy (at least 20 μm)
Advantages vs disadvantages of data compression

• To improve time resolution (better spike id, primary vertex id) the sampling frequency was increased to 160 MHz

• At 12-bit sampling + 1-bit gain id, this translates into a 2080 Mbit/s bandwidth per channel

• With off-detector Level-1 trigger formation, most of the samples will contain baseline and its fluctuations

• Bandwidth compression gives the opportunity to use three less fibers per trigger tower, saving O(1M CHF), and reducing per channel bandwidth to 1.28 Gb/s

• Added latency

• Some uncertainty in bandwidth occupation

• Management of noisy channels
The decompression logic in the BCP uses a LUT-based FIFO real dual port per each channel.

The decompression logic is implemented in a KCU105 FPGA.

It is designed to handle data received by the IpGBT deserializer block in order to decompress and feed the BCP Trigger Primitive Generator and the DAQ with synchronized 13-bit samples at 160MHz.

The main logic is simple and contains two blocks:
- Decompression Decoder
- FiFo