Contribution ID: **54** Type: **Oral**

The upgraded readout electronics of the CMS ECAL: system overview

Thursday, 5 September 2019 10:15 (25 minutes)

The readout electronics of the CMS electromagnetic calorimeter (ECAL) barrel will be upgraded to meet the Level-1 trigger requirements at HL-LHC. The new very front-end (VFE) electronics will mitigate the increasing noise from the avalanche photodiodes (APDs), discriminate against anomalous APD signals, and provide the extra bandwidth needed to maintain the integrity of the detector signal shape. The front-end (FE) card will provide the streaming of data from VFE to back-end electronics, which will have increased granularity (tower-level to single crystal-level). The design of the full ECAL barrel readout chain and the status of the components R&D will be presented.

Summary

During High-Luminosity LHC phase (HL-LHC), the CMS ECAL will have to cope with a challenging increase in the number of interactions per bunch crossing and radiation levels. The ECAL barrel (EB) on-detector and off-detector electronics have been completely redesigned to preserve detector performance with the goals of providing precision timing, low noise, and added flexibility in the trigger system.
Two custom ASICs have been developed for the very front-end (VFE) upgrade: CATIA (CAlorimeter Trans-Impedance Amplifier), a fully analog ASIC, and LiTE-DTU, a digital signal processing unit, designed in commercial CMOS 130 nm and 65 nm technology, respectively. CATIA and LiTE-DTU ASICs will manage to cope with the new requirements in terms of input bandwidth, conversion and transmission rates, and radiation tolerance. The two ASICs will be hosted by a VFE board with the same form factor and cooling system as the legacy system. The current readout chip (MGPA) based on Charge Sensitive Amplifier (CSA) will be replaced by a high speed Trans-Impedance Amplifier (TIA), 50 MHz of bandwidth. The output dynamic of CATIA ASIC is split into two ranges: 200 GeV (achieved through a gain10 stage after the TIA) and 2 TeV. The two output gains are fed to a dual 12-bit, 160 MS/s ADC hosted by the LiTE-DTU ASIC. The high speed TIA and the high speed ADC will enable the mitigation of the increasing noise induced by avalanche photodiode (APD) ageing, to improve the suppression capability of APD anomalous signals, and to help to discriminate between energy deposits coming from different overlapping events.
The EB upgrade will face to an increasing of sampling frequency from 40 MS/s to 160 MS/s and a granularity from tower-level (5x5 crystals) to single crystal-level. In addition, the EB system will have to fulfill the maximum trigger rate requirement of 750 kHz and event pipeline of 500 bunch crossings 12.5 us). Each readout channel will produce an amount of data which will require fast data transmission circuitry and high speed serial links. A new digital architecture has been developed in order to decrease the data bandwidth by means of lossless data compression. This function has been integrated in the LiTE-DTU, which performs compression based on a simplified version of Huffman coding taking advantage of the relatively low compression rate needed (around 0.6). This method allows the readout to easily manage two different code lengths while avoiding transmission errors. The new front-end (FE) card will host LpGBT chips that concentrate and stream all data, generated on the VFE cards, and send them to back-end (BE) electronics via Versatile+ links. This will allow the trigger primitive generation (TPG) and the DAQ of the legacy FE to be moved to a new BE system. The latter will also handle the FE control. In addition, a high precision clock, essential in a high pile-up environment, is foreseen to be distributed to the front-end boards.

CATIA, LiTE-DTU, and front-end designs will be presented, along with the verification of the compression scheme and the test results of the prototypes.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience