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First results of CIC data aggregation ASIC for the future CMS Tracker

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The Concentrator Integrated Circuit ASIC is a front-end chip for both Pixel-Strip and Strip-Strip modules of the future Phase-2 CMS Outer Tracker upgrade. It collects the digital data coming from eight upstream front-end chips, formats the signal in data packets containing the trigger information from eight bunch crossings and the raw data from events passing the first trigger level, and finally transmits them to the LpGBT unit. A first prototype in a 65nm CMOS technology integrating all functionalities for system level operation, CIC1, has been tested in early 2019. The design and its implementation, along with test results, are presented.

Summary

The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). A first prototype in a 65nm CMOS technology integrating all functionalities for system level operation, CIC1, has been tested in early 2019. The design and its implementation, along with test results, are presented, along with the current development of the final CIC version. The future tracker detection module, named pT-module, is a key element of the future detector.The most internal areas will be equipped with so-called PS module (pixels/strips), of greater granularity.

The basic principle, two silicon layers separated by a few mm, is relatively standard in current tracking detectors. Readout electronics, on the other hand, is entirely new. Indeed, as can be seen in the figure on the right, the signal of the 2 layers can be put in coincidence in the module itself, therefore allowing a significant reduction of the detector output data rate. This coincidence is performed by 2 very front-end ASICs types: CBC and MPA for 2S and PS modules respectively. Each pT-module contains 16 such ASICs.
The Concentrator Integrated Chip (CIC) performs a further data compression stage. The CIC is a fully digital ASIC that must be compatible with 2 different modules flavours.

The integrated circuit receives information from 8 identical MPAs or CBCs, it reformats these data, processes them, and groups them in packets before the send to another ASIC that transmits the signal outside the detector. Each pT-module will contain 2 CICs, so there will be about 30000 CICs in the future tracker.

In order to validate the CIC model, a first version was developed and implemented, along with a complete standalone testbench. The CIC1 incorporates all the functionalities of the final chip and has the same footprint for the card wiring. The main difference is that the radiation hardness techniques were not used for its design, whereas it will be the case for the final version.

First CIC1 samples were received in February 2019. Thanks to the test system presented previously, it was possible to rapidly verify the correct functioning of the ASIC: the processing of the data received corresponds to the specifications. Detailed power measurements were performed in order to characterize the architecture.

The results observed so far are very encouraging for the future: the next stage of the project is the completion by the end of 2019 of a pre-production version of the ASIC, the CIC2. This chip will be resistant to radiation and will include modifications to reduce the nominal consumption. The final output of the 30,000 CICs that will be installed in the future tracker is planned for 2020.

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