Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

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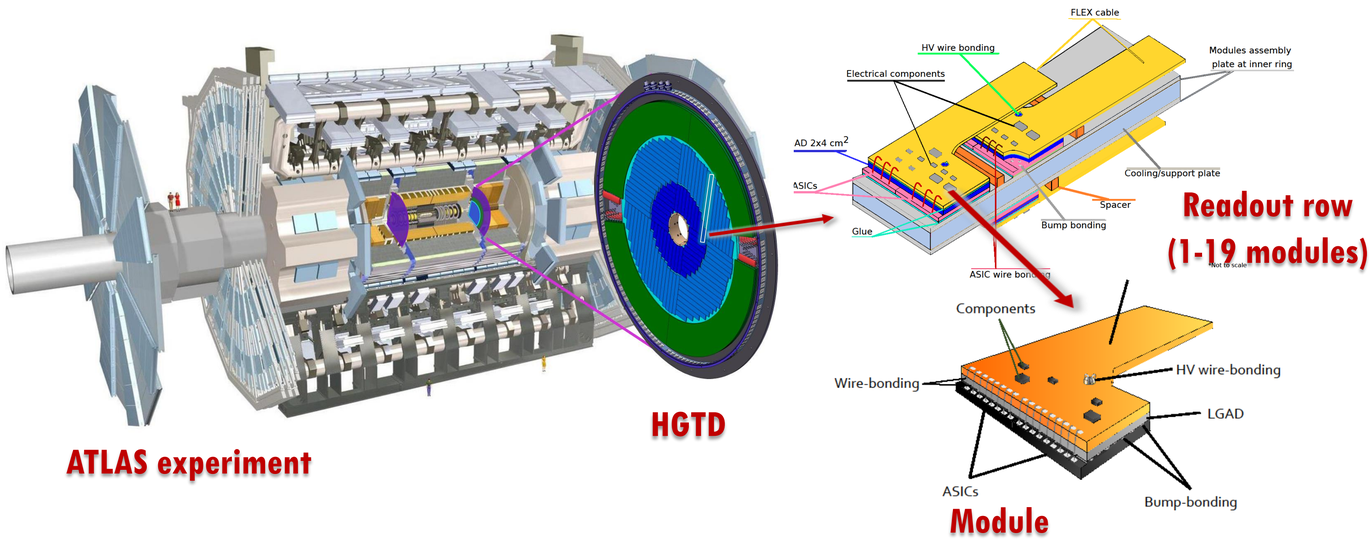
High-Granularity Timing Detector (HGTD)



The High Granularity Timing Detector for the High Luminosity ATLAS Phase II upgrade, will provide precise timing information (30 ps per track) at CERN LHC. Placed in the endcap regions, the detector active area consists of 8000 modules (detector basic unit) placed in the so-called redout rows

Module (2x4 cm²): A Low Gain Avalanche Detector (LGAD) is bumped to 2 ASICs and then glued and wire-bonded to a Flexible Printed Circuit (FLEX cable)

FLEX cable: Requirements and Specifications

The Flexible Printed Circuit is the most appropriate technology due to the compact design of the HGTD. The FLEX cable manages the signals to read out and control the modules, biases the sensors with high voltage and powers the ASICs

Signal type	Signal name	No. of wires	Comments
HV	1 kV max.	1	Clearance
POWER	1x Vdda, 1x Vddd, 1.2 V	2	2 planes, R < 2.7 mΩcm^{-1}
GROUND	Analog, Digital	1 (2) plane(s)	Dedicated layer, R < 0.7mΩcm^{-1}
Slow control	Data, Ck (opt. +rst, error)	2 to 4	I^{2}C link
Input clocks	320 MHz, Fast command e-link	4 or 8	CLPS
Data out lines	Readout data (TOT, TOA, Lumi)	4 pairs	4 e-links differential CPLS
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6	DC voltage
Debugging	ASIC_debug	2	Analog

- Controlled impedance: 100 Ω diff. pairs, 50 Ω single lines (both ± 10 %)
- Nominal date rate: 1.28 Gb/s
- BER < 10^{-11}
- Width = 19 mm, thickness = 350 um, but length between 16 and 75 cm

FLEX cable prototype

75 cm

4 layers stackup: HV line and differential lines, stripline configuration

Single lines, microstrip configuration

4 prototype pieces (fully assembled and wire-bonded for testing)

A significant subset of the signals was selected to address the design requirements (signal integrity, power distribution, HV-insulation, interference and crosstalk)

The study phase by manufacturing a 75 cm length prototype investigates the technology requirements (materials, manufacturing capability, electrical and mechanical robustness)

The Flex cable prototype was manufactured by the CERN PCB service (CP)

An adapter board has been developed as plug-in for the FMC High-Speed connector on the Kintex KC705 [2].

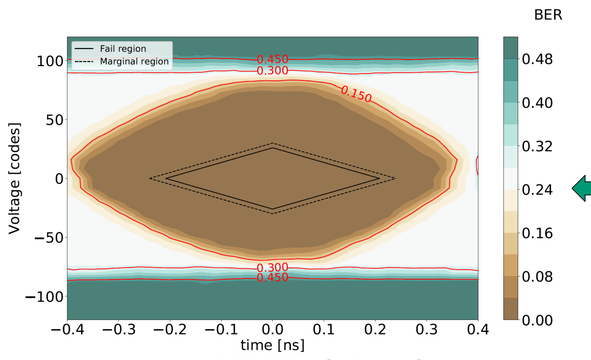
FLEX cable dimensions		
Length [cm]	Width [mm]	Thickness [μm]
75.0±0.2	17.99±0.04	300±10

Dimensions within the specifications

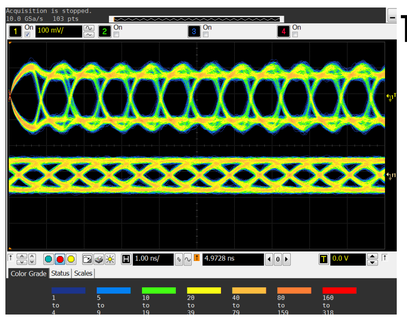
Signal Transmission Performance

Eye diagrams

Signal transmission through a differential pair line



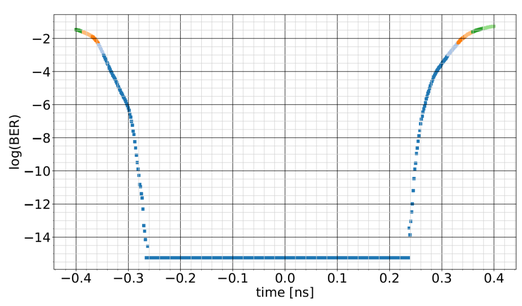
Kintex KC705 Eval. Board



Oscilloscope

Track length
75 cm
2x 75 cm
100 mV/div
1 ns/div

Bathtub



GTX drivers setttings:

TX Diff Swing 1119 mV

TX Post-cursor 6.64 dB

TX Pre-cursor 0.00 dB

RXterm 900 mV

The FPGA KC705 Eval. Board[2], compatible with the VC707[3] used by the LpGBT [4] designers, is programmed to inject test patterns at **1.25 Gb/s** and check the response with the **IBERT**. SMA connectors on the adapter board route the signals to the oscilloscope for classical eye-diagram analysis

Good performance in terms of signal transmission for 2x track length (75 cm): BER test shows no errors and for eye diagrams parameters, the opening area is larger than the evaluation mask area recommended by Kintex. Bathtub width 500 ps at BER <10^{-14}

Integrated Bit Error Rate Result

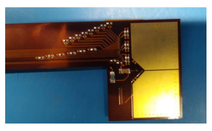
Prototype	BER	Errors
CP	10^{-15}	0

Power Integrity Simulations and Measurements

Post-layout simulations with Cadence "Sigrity" and "PowerSI" [1] (signal integrity and power distribution over long lines)

Additional ground areas reduces significantly the resistance of the analog planes

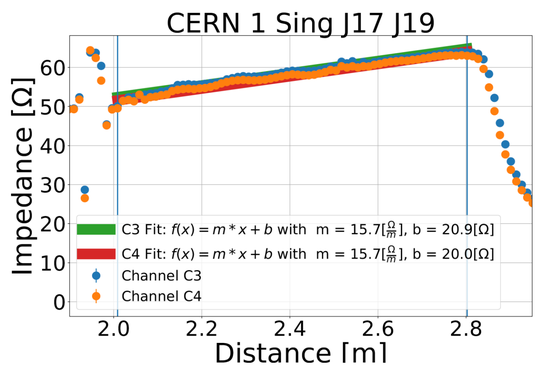
Measurements with Keithley 2100 multimeter [5]



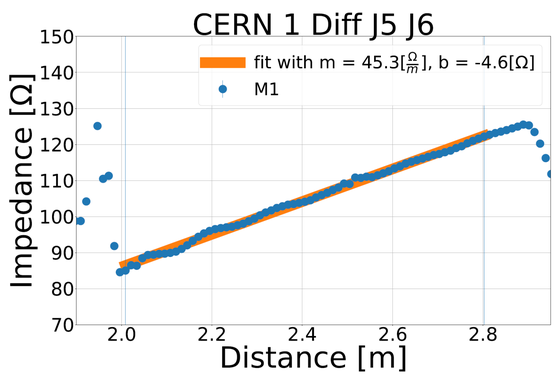
Plane	Resistance sim (mΩ)	Resistance mea. (mΩ)
CP analog	97	191
CP digital	440	428

Time Domain Reflectrometry Measurements

2 Single lines impedance



Diff. Line impedance



TDR technique to evaluate the characteristic impedance of both the single and differential pair lines (module 80E08, Tektronix)

As expected, the impedance slightly increases with the distance. The manufacturing process should be improved to reduce the tolerance from ± 20 % to ± 10 %

[1] Cadence Sigrity and PowerSI Cadence Desgn Systems Inc, https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/pcb-design-analysis/sigrity-powersi-ds.pdf
[2] K7C05 Evaluation Board. Xilink Inc. https://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf
[3] VC707 Evaluation Board. Xilink Inc. https://www.xilinx.com/support/documentation/boards_and_kits/vc707/ug885_VC707_Eval_Bd.pdf
[4] LpGBT project. GBT project "Radiation Hard Optical Link Project". https://espace.cern.ch/GBT-Project/default.aspx
[5] Keithley 2100 6 ½ Digit Multimiter

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