Contribution ID: **144** Type: **Poster**

Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

Tuesday, 3 September 2019 17:20 (20 minutes)

The compact structure of the HGTD proposed for the High Luminosity ATLAS detector upgrade at the CERN LHC requires a design to match the tight mechanical and electrical constraints. Our solution with a flexible printed circuit manages the signals to read out and control the modules, to bias the sensors with high voltage and to power the ASIC. It is crucial to match the characteristic impedance of the lines. The high voltage bias requires clearance and shielding to limit the interference with the digital logic. We present the results of several geometrical and electrical tests performed on the first prototype.

Summary

The High Granularity Timing Detector (HGTD) proposed for the High Luminosity upgrade of the ATLAS detector at the LHC at CERN has the purpose to provide a very precise time information for each track (30 ps resolution) to assign them correctly to the hard scatter vertex or to the additional collisions taking place at the same bunch crossing (pile-up).

The HGTD consists of 8000 modules that are the basic unit of the detector. A bare module comprises a Low Gain Avalanche Detector (LGAD), which requires biasing, up to 1000 V, bump-bonded to two ASICs. A module has a surface of 2x4 cm2 . The signal transmission from each elementary unit to the electronics boards that surround (peripheral electronics) the detection region requires customized electronics. High Voltage (HV), slow control, high-speed differential signals (1.28 Gb/s) and clock at different protocols should be transferred. All these signals must be contained in an independent cable to be fitted in the very limited available space. Considering all the relevant specifications, a flexible printed circuit (FLEX cable) is the most appropriate choice to fulfill the requirements. A module consists of a bare module wire-bonded and glued to the FLEX cable.

The cable thickness should not exceed 350 µm (up to 10 FLEX cables max. will be stacked) and the width should be less than 18 mm outside of the bare module surface. The length is defined by the different positions of the modules on the active area and of the corresponding connector on the peripheral electronics. The FLEX cables length ranges from 160 to 750 mm.

The study phase and the analysis of the constraints lead to the design of a prototype with the maximum expected length, but only a few lines of each type to address the potential limitations of the technology. To distinguish between design and production effects, the approach to the same design by two different manufacturers was studied.

The prototype consists of a stack-up of four layer of polyimide with a total thickness of 350 µm.

The electrical requirements for the ASIC are two voltage supplies at 1.2 ± 0.2 V and the impedance of the lines to be 80-100 Ω for differential and 45-55 Ω for single-ended lines. The high-voltage to bias the sensor is expected to be in the range 600 –1000 V.

Several electrical and geometrical tests on the prototype show that a behavior within or close to the specifications. The comparison of the discrepancies between two different manufacturer processes gives an overview of the technological limitations.

An exhaustive characterization with static and dynamic tests will be presented. We discuss the details of the Time Domain Reflectometer (TDR) measurements for the transmission lines. We estimate the performance of the data-link in terms of Bit Error Rate (BER) for the longest cable as well as the influence of the HV bias on

the high-speed digital logic. Therefore, a small test setup based on a Kintex FPGA evaluation board emulates the realistic conditions of the cable in normal operations.

Primary authors: ROBLES MANZANO, Maria (Johannes Gutenberg Universitaet Mainz (DE)); MASETTI, Lucia (Johannes Gutenberg Universitaet Mainz (DE)); Dr WEITZEL, Quirin; BROGNA, Andrea Salvatore (Johannes-Gutenberg-Universitaet Mainz (DE)); KURT, Atila Eyüp (Mainz University); BERNHARD, Peter; PLATTNER, Paul (Mainz University); GREINER, Fabian

Presenter: ROBLES MANZANO, Maria (Johannes Gutenberg Universitaet Mainz (DE))

Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience