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Back-end firmware for the LHCb VELO upgrade phase I

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LHCb detector is a general purpose experiment instrumented in the forward region at the LHC, specialized in b- and c- physics, new physics and CP violation. The Vertex Locator (VELO) detector is being upgraded along with the rest of the tracking system and readout architecture during 2019-2020. The aim of this poster is to present the architecture of the control and readout firmware on the VELO specific back-end boards. Latest progress towards the installation and commissioning will be shown.

Summary

The upgrade of the LHCb experiment is being installed during the long shut down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the front-end ASIC (VeloPix). The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s/ASIC and produce an output data rate of over 15
Gbits/s, adding up to 2.85 Tbit/s of data for the 40 Mpixels of the whole VELO.
The VeloPix transmits zero suppressed, time-stamped, non sorted packets with binary hit information over 5.13 Gbits/s links with a custom data protocol (GWT) to the back-end boards in the LHCb surface. Back-end readout boards (FPGA based) recover, synchronize, sort, clusterize the data and send it to the LHCb CPU farm for further processing. Due to the lack of a hardware trigger at LHCb, a significant processing load is placed on the CPU farm. A campaign to reduce this processing overhead for LHCb has been initiated, and implementing more of the processing in the FPGA back-end is critical to this endeavour.
This poster will present an overview of VELO back-end firmware. This VELO firmware is comes in two variants, (control and data acquisition) derived from a LHCb common
framework. The control firmware is dedicated to the distribution of slow control and fast timing signals to the front-end electronics. Customization to the control framework for
the SLVS protocol used by VeloPix will be outlined.
The data acquisition firmware accepts the data from the twenty links of one VeloPix module with an input rate up to 100 Gbits/s. The GWT transmission protocol and its
motivating factors over the standard GBT will be described. The time-ordering of the unsorted input data will detailed and the impact of this modification to the standard LHCb firmware framework. We will present new algorithms for clustering the VeloPix hits, and the positive impact to the downstream CPU processing downstream. Methods for simulating the firmware algorithms and the monitoring tools developed for verification will also be presented.

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