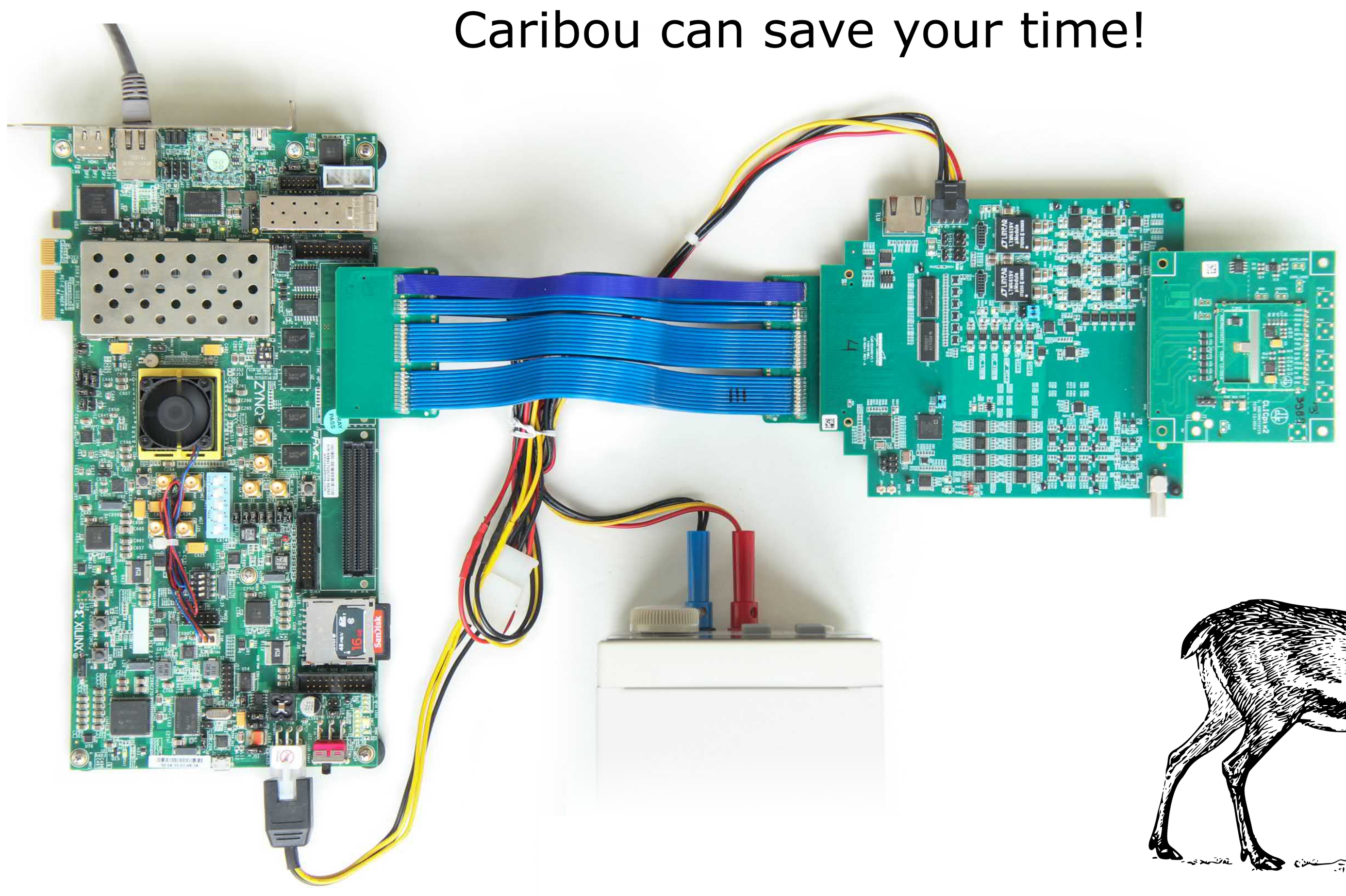
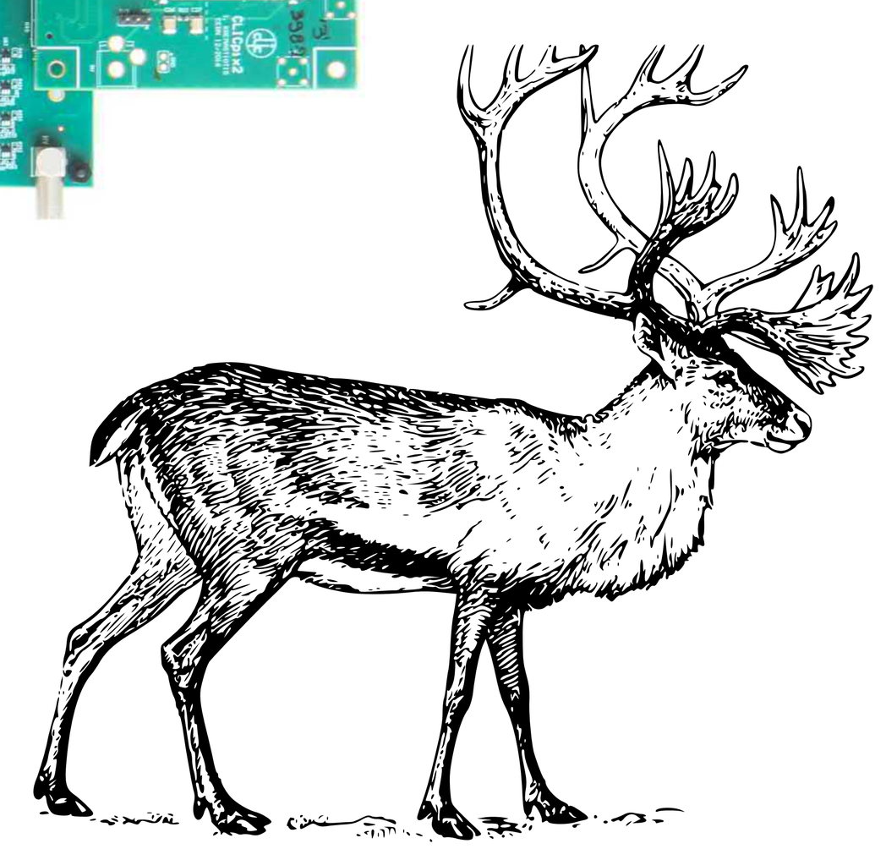
Caribou

A versatile data acquisition system based on programmable hardware

Tomas Vanat on behalf of the CLICdp collaboration, TWEPP 2019, 2 - 6 September 2019, Santiago de Compostela

Developing a silicon pixel detector?
Need a DAQ for your prototype?
Caribou can save your time!



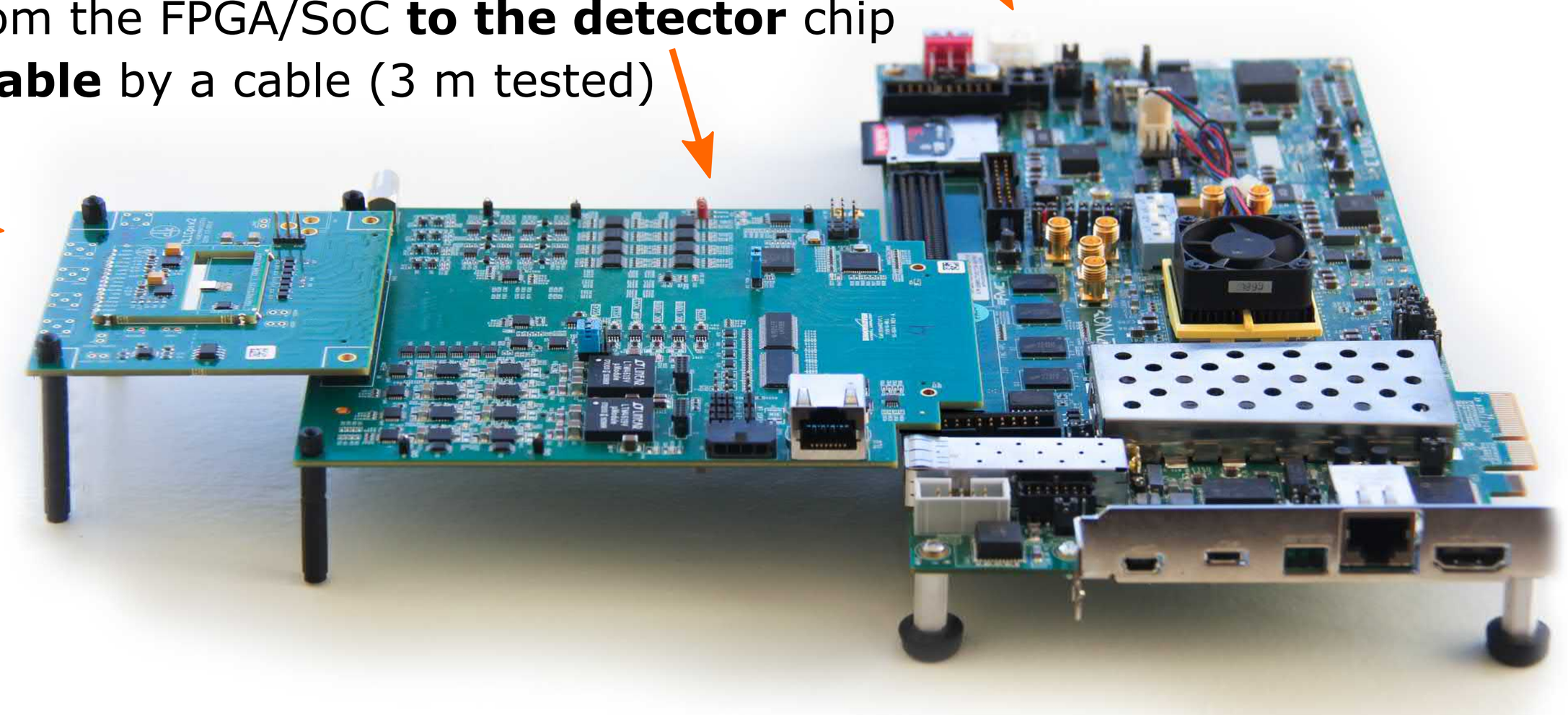


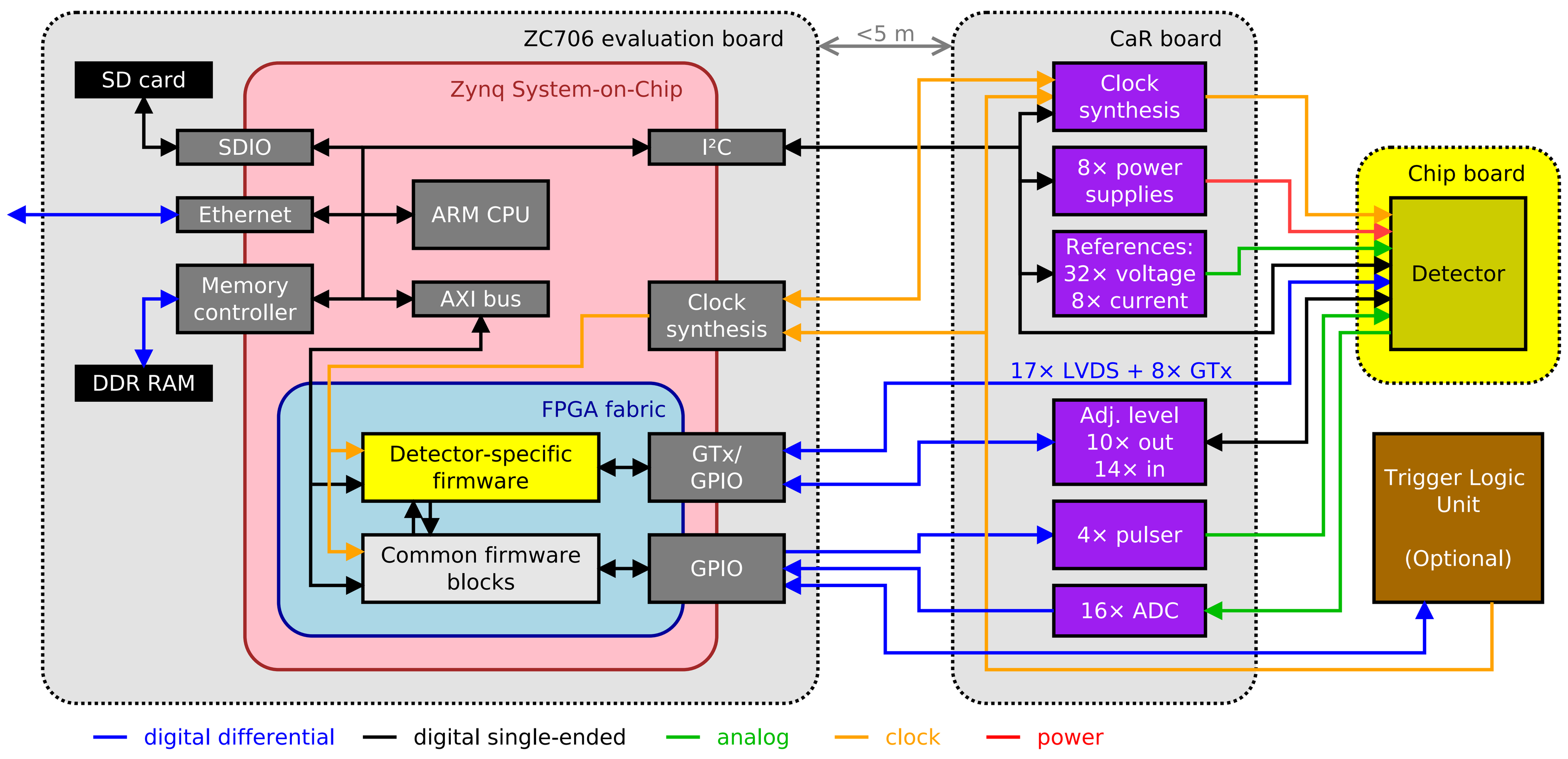
Motivation

- A **similar** concept of **readout, control** and **powering** is used in most silicon pixel detectors
  - Differs in voltage levels, number of channels or protocol
- A **new detector-specific DAQ** system is usually developed for each new detector
  - **Time-consuming** process of HW/FW/SW development brings **no innovative** functionality
- A **versatile DAQ** system for prototyping can **speed-up** the **development** process
  - Caribou, initially CaRIBOu, started as a project for ATLAS by BNL, UniGE and CERN and is an acronym for Control and Readout Inner tracker Board
  - Caribou provides **HW** and **SW cores** and **interfaces**, only detector-specific part is modified

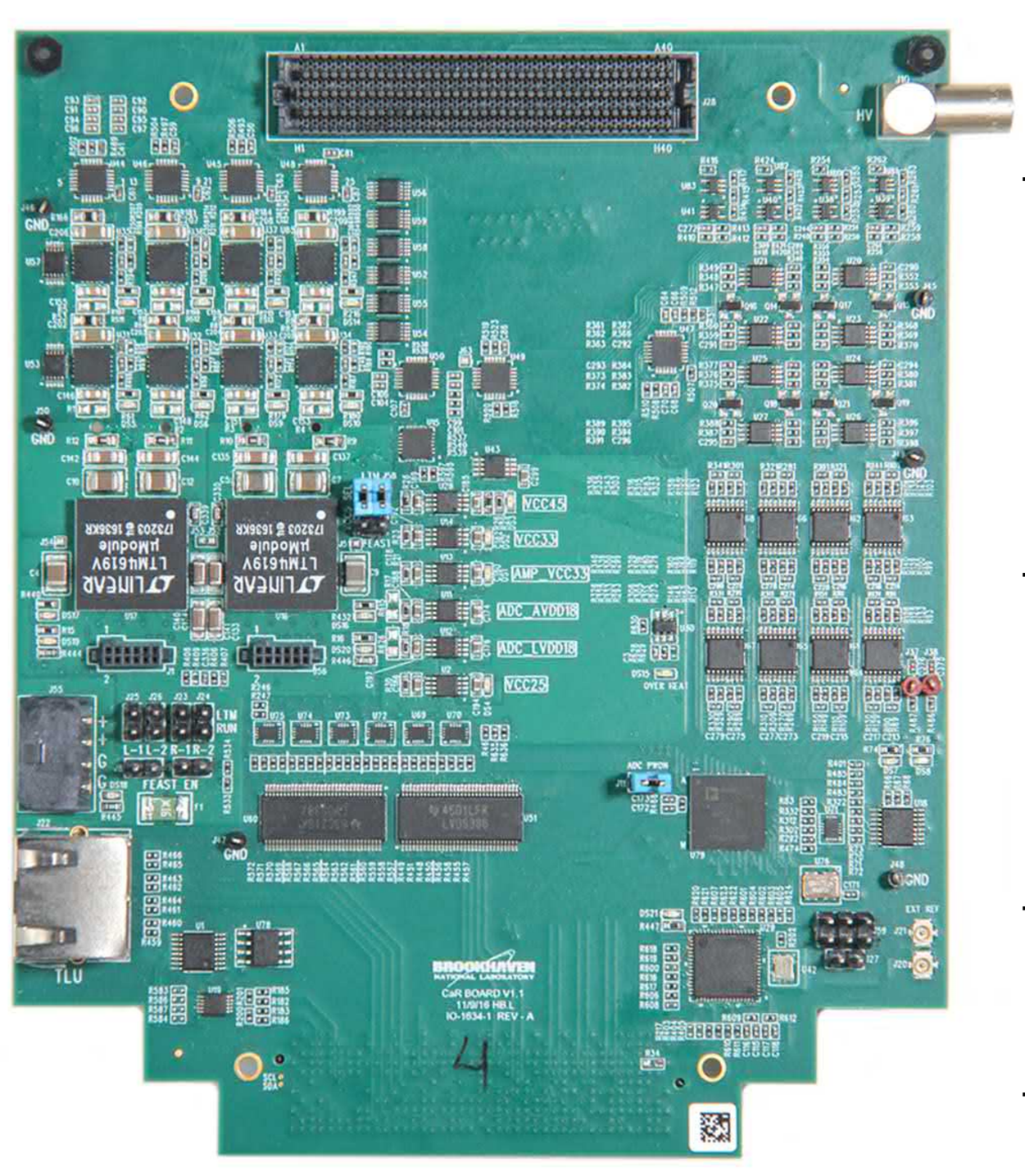
Caribou hardware architecture

- FPGA/SoC board (e.g. Xilinx ZC706)
  - An **embedded CPU** runs the operating system (**Linux**), **DAQ** and **control software** (Peary)
  - An **FPGA** runs **detector-specific hardware** blocks for data processing and detector control
- Control and Readout (CaR) interface board
  - Provides **physical interface** from the FPGA/SoC **to the detector** chip
  - CaR – FPGA connection **extendable** by a cable (3 m tested)
- **Application-specific** detector carrier board
  - **Detector** chip **and passive components** only



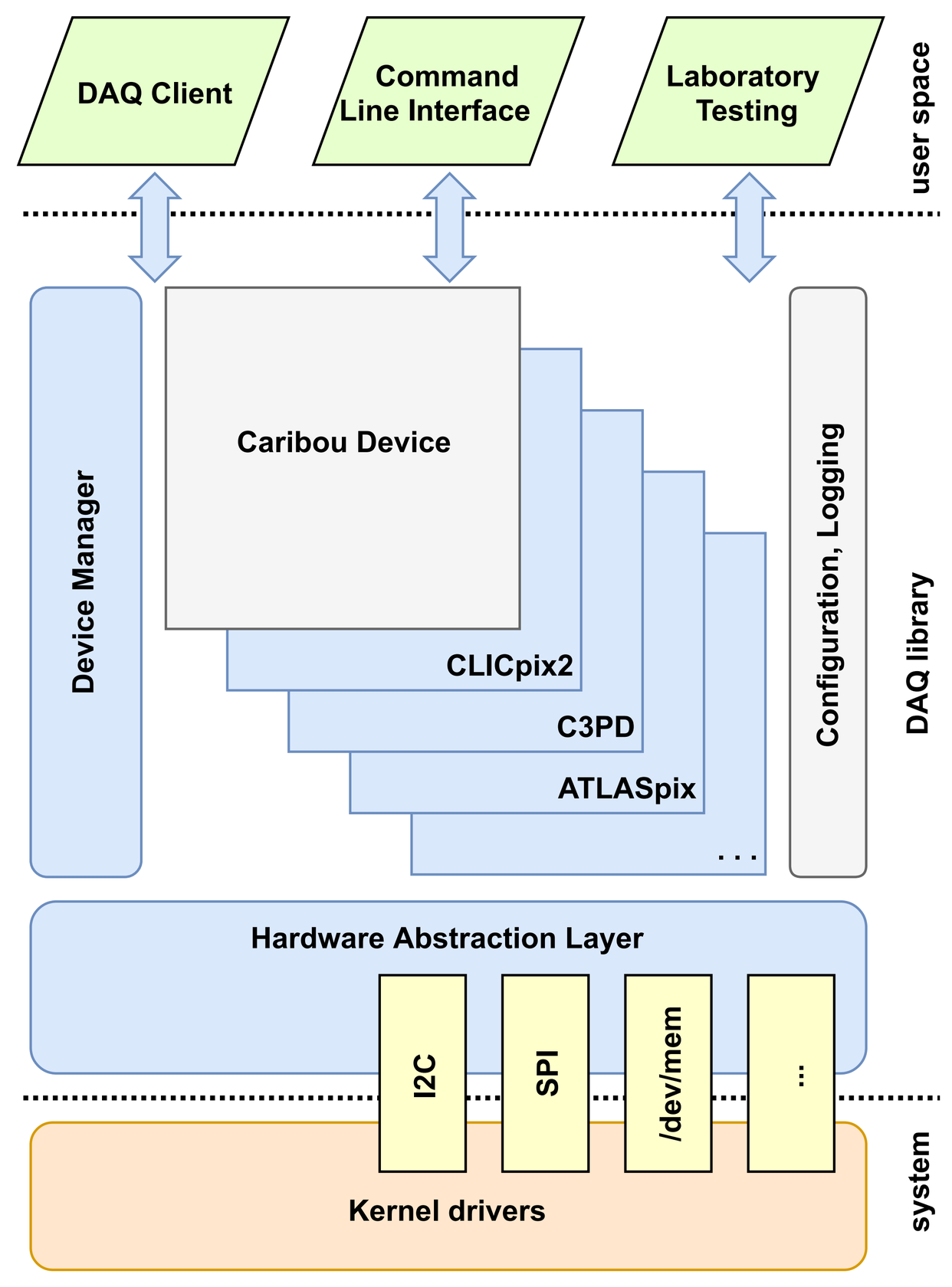


Control and Readout (CaR) board

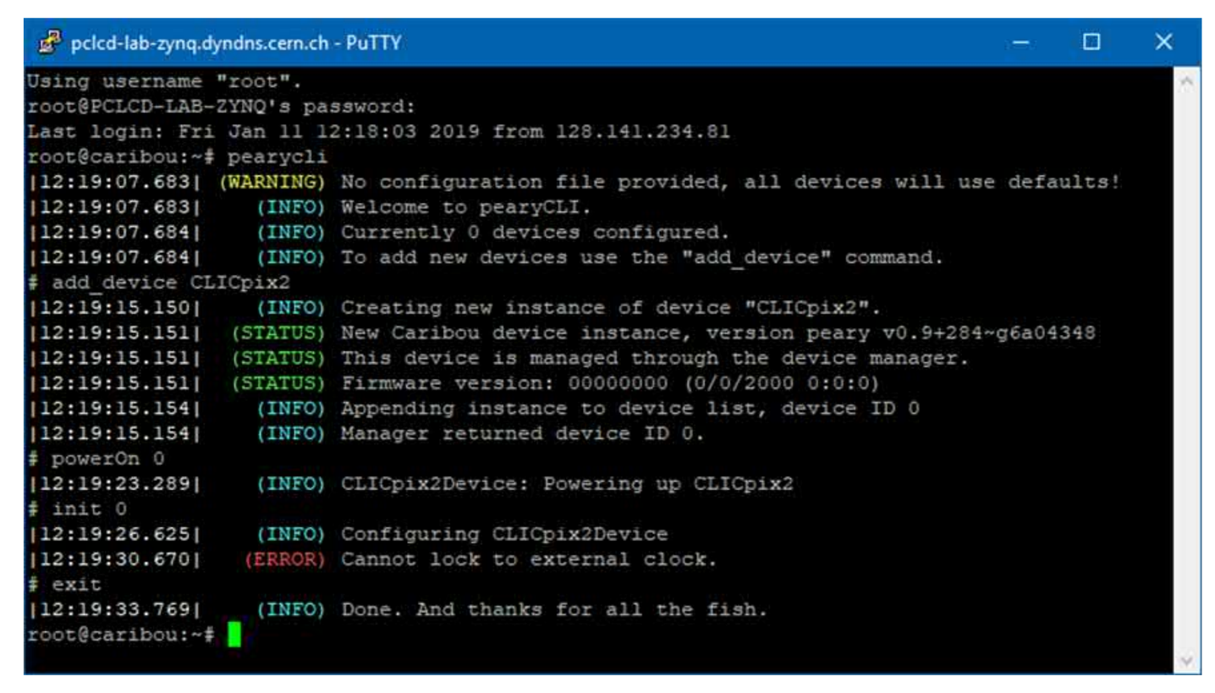


Power	• 8 adjustable **power supplies** with monitoring • external **HV input**
Analog I/O	• 8 inputs to **12-bit ADC**, 50 kSamples/s • 16 inputs to **14-bit ADC**, 65 MSamples/s • 4 programmable **injection pulsers** • 32 adjustable **voltage references** • 8 adjustable **current references**
Digital I/O	• 8 full-duplex **high-speed links** (0.8-12 Gb/s) • 17 bidirectional **LVDS links** (<1.1 Gb/s) • 10/14 **output/input links**, adjustable level • **TLU** interface
Clocking	• Programmable low-jitter **clock generator** with **external** (TLU) **reference**
Interface	• **FMC** interface to FPGA board • 320-pin SEARAY interface to detector chip

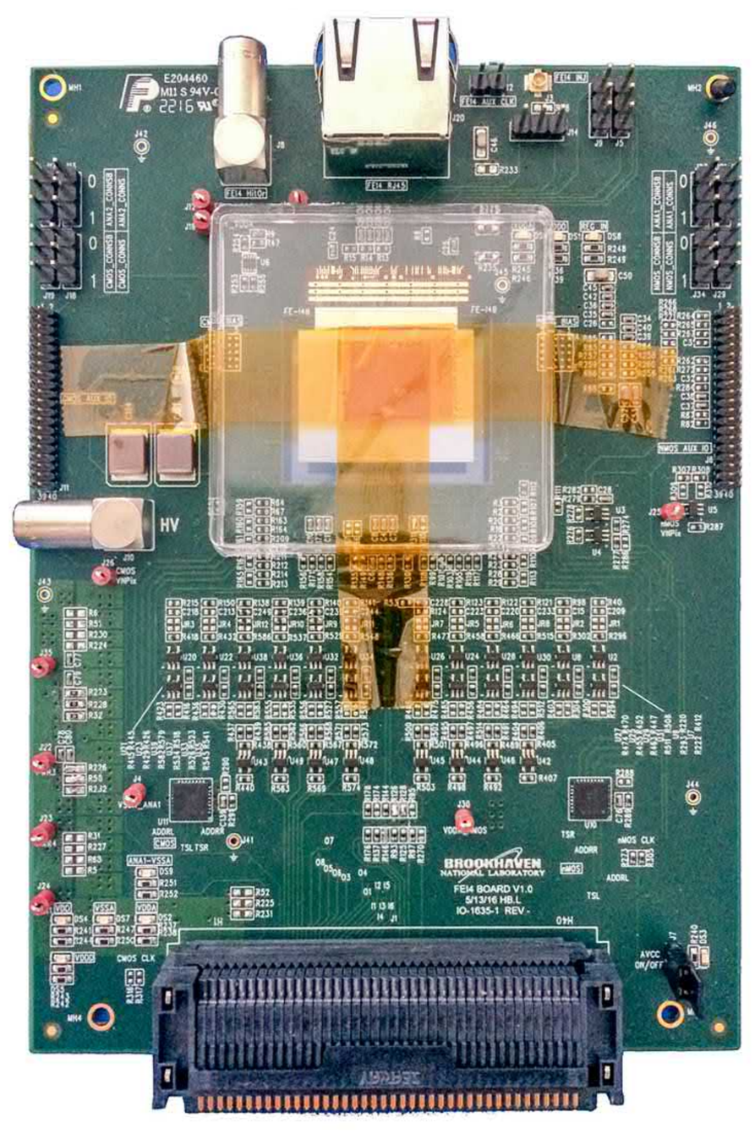
Caribou software architecture



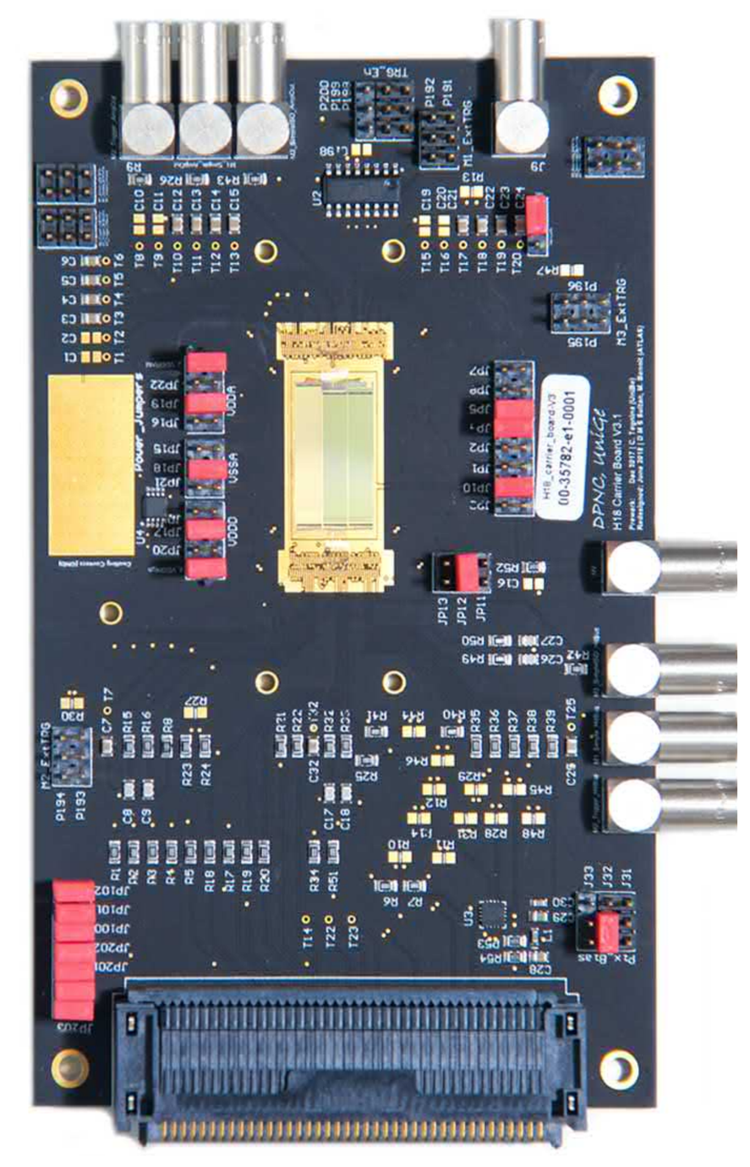
- **System:** Yocto- and OpenEmbedded-based Linux ("Poky")
- **DAQ library** ("Peary") containing:
  - Hardware **Abstraction Layer** (HAL), allowing to handle hardware peripherals as objects in C++
  - **C++ templates** for implementing a new user device
  - **Logging** with multiple verbosity levels
  - **Device manager** supports multiple devices in parallel
  - **Command line interface** for standalone operation
  - **Client interface** for integration with another DAQ



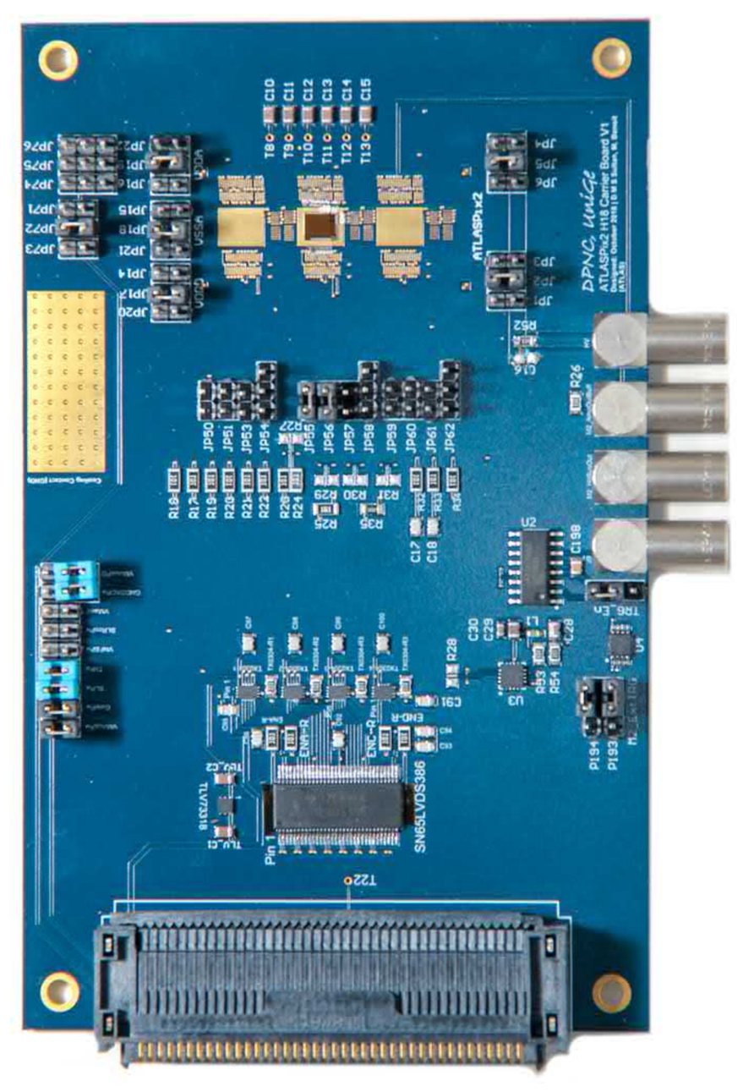
Supported detectors



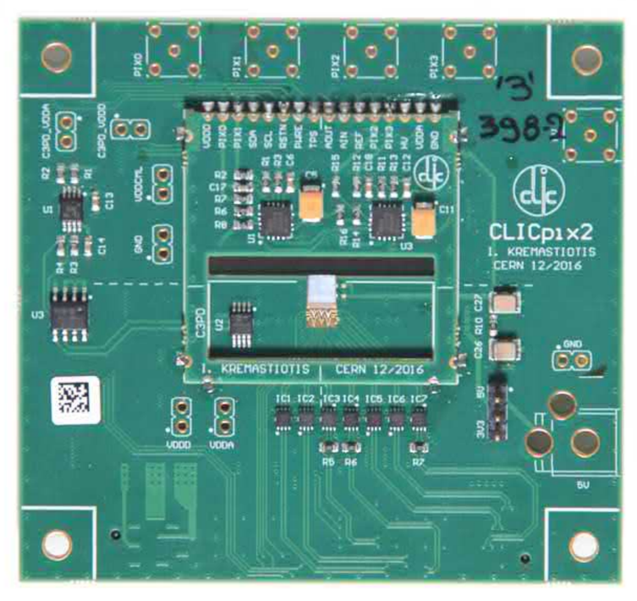
H35Demo/FEI4



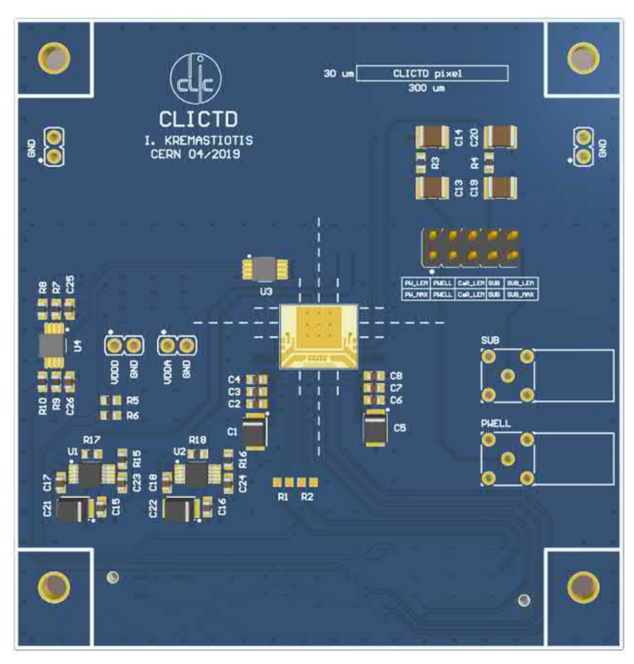
ATLASPix



ATLASPix2



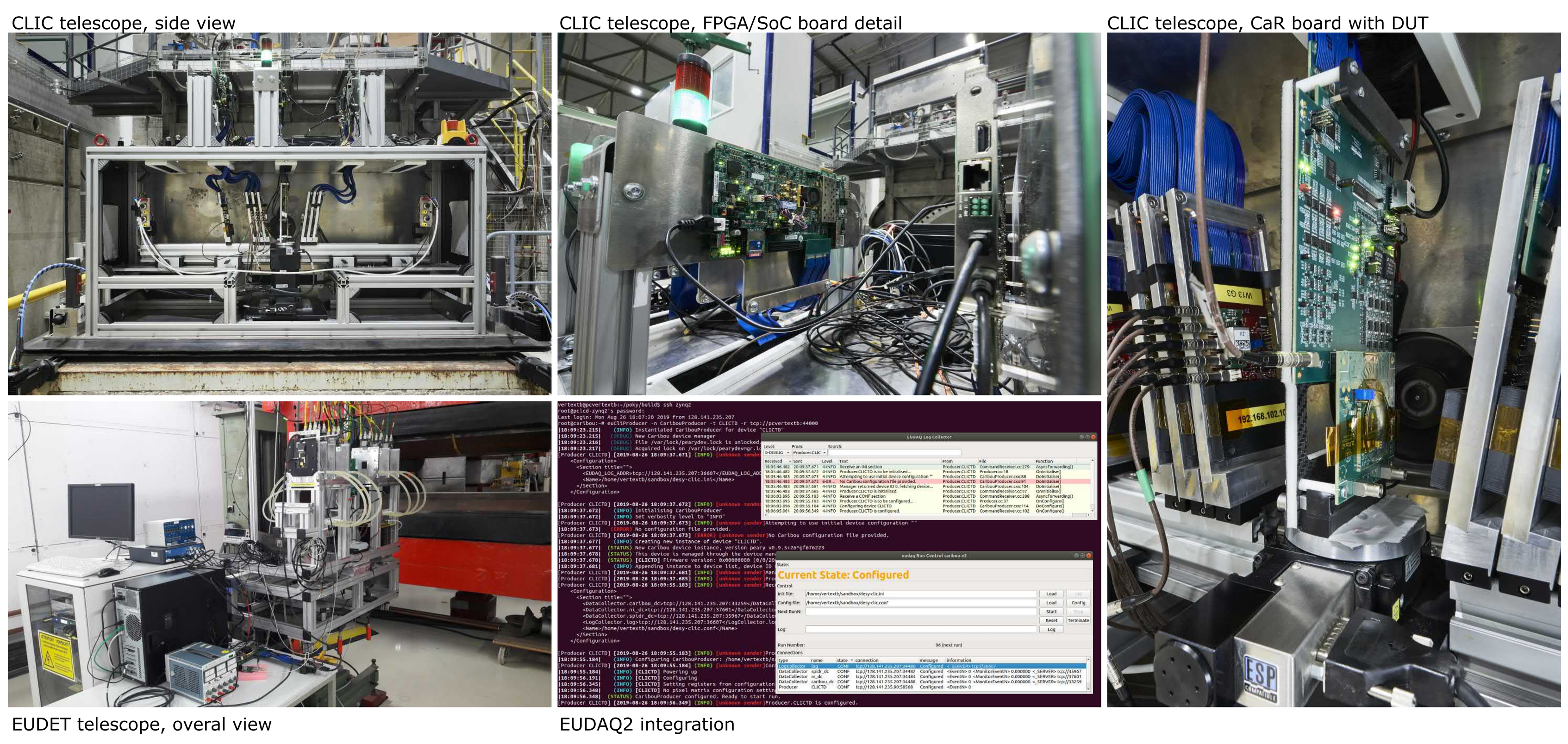
CLICpix2/C3PD



CLICTD

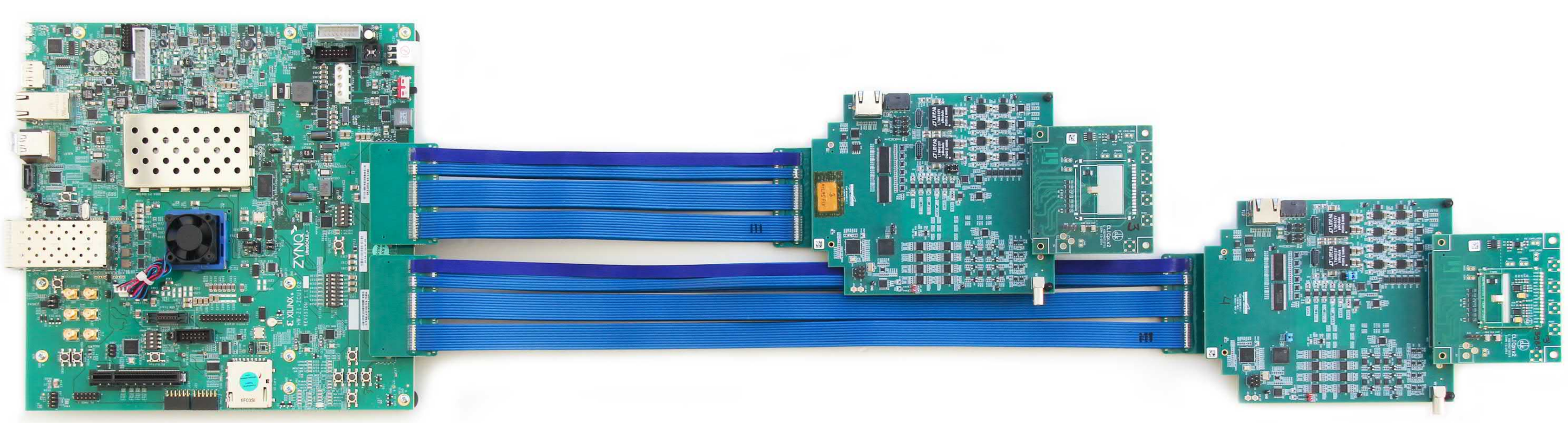
Testbeam integration

- **CLIC telescope** in SPS North Area (**CERN**)
- **EUDET telescope** (**DESY**), fully controlled from **EUDAQ2**



Work in progress and future plans

- Migrate the system to Zynq **UltraSCALE+** (ZCU102 board)
  - 64bit architecture, 4 cores, faster CPU
- **DMA** for fast data transfer
- **New detectors** support
  - ATLASPix3, RD50, CLIPS



gitlab.cern.ch/Caribou