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Overview of the HL-LHC Upgrade for the CMS Level-1 Trigger

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In view of the High-Luminosity LHC, the Compact Muon Solenoid (CMS) experiment is planning to replace entirely its trigger and data acquisition system. Novel design choices are being explored such as ATCA prototyping platforms and newly available interconnect technologies proving links up to 28 Gb/s. Higher-level trigger object reconstruction is performed through large scale FPGAs (such as Xilinx UltraScale) handling over 50Tb/s of fine granularity detector data with an event rate of 750 kHz. The system design and ongoing hardware R&D will be described.

Summary

The High-Luminosity LHC will open an unprecedented window on the weak-scale nature of the universe, providing high-precision measurements of the Standard Model as well as searches for new physics beyond the Standard Model. Such precision measurements and searches require information-rich datasets with a statistical power that matches the high-luminosity provided by the Phase-2 upgrade of the LHC. Efficiently collecting those datasets will be a challenging task, given the harsh environment of 200 proton-proton interactions per LHC bunch crossing. For this purpose, CMS is designing an efficient data-processing hardware trigger (Level-1) that will include tracking information and high-granularity calorimeter information. The current conceptual system design is expected to take full advantage of advances in FPGA and link technologies over the coming years, providing a high-performance, low-latency computing platform for large throughput and sophisticated data correlation across diverse sources

Modern technologies offer an effective solution to achieve these goals. The upgraded system makes use of newly released UltraScale Xilinx FPGAs technology implemented on the ATCA platforms. Data received from the tracker, the calorimeters and the muon systems represents a total bandwidth of 50 Tb/s, which are processed through innovative architecture designs such as Time-Multiplexed-Trigger (TMT). Higher granularity inputs, algorithms operating on a wider field of view allow for improved position and energy resolution of regional and global quantities. Optical interconnects are via 28 Gbps optical links are being studied and currently tested on various subsystems.

A dedicated Correlator Trigger will be used as central processor to compute high-level trigger objects and correlation among objects. A Time-Multiplexed approach is considered to provide enough latency for the implementation of sophisticated algorithms such as particle flow reconstruction. This approach is designed to allow for a high processing clock speed and thus efficient use of logic resources. The fully pipelined firmware approach of the TMT provides an efficient way to localize the processing, reduce the size and number of fan-outs, minimize routing delays and eliminates register duplication. The successful firmware implementation and testing of such algorithms will be discussed.

The talk will cover the technological aspects of the Phase II upgrade trigger system emphasizing on the many challenges of its implementation and in particular the innovative algorithms proposed. Results of its expected performance based on simulated data will be presented. The recent results from demonstration and hardware validation vs software emulator will also be detailed. The ATCA boards designed for this project are aiming towards a standardization of the data processing required for the future LHC electronics systems.

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