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eFEX preproduction module design and test

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The Electron Feature Extractor (eFEX) is one of the core subsystems for the Phase-I upgrade of the ATLAS Level-1 Calorimeter Trigger. In Run 3, the eFEX will identify isolated e/g and tau candidates with much higher discriminatory power than in Run 2. The eFEX subsystem consists of 24 eFEX modules housed in two ATCA shelves. Each eFEX module has up to 200 optical input/output links and more than 400 on-board electrical fan-out links, all running at 11.2Gbps. Four pre-production modules have been made and tested. We present hardware and firmware design experience and test results from the eFEX pre-production modules.

Summary

The ATLAS Level-I Calorimeter Trigger Phase-I upgrade consists of three Feature Extractor (FEX) subsystems: eFEX, jFEX and gFEX. The function of eFEX is to identify the isolated energy deposits in the electromagnetic and hadronic calorimeters indicative of electrons, photons and taus. To cope with the increased pileup in Run 3, the eFEX runs more sophisticated algorithms with higher discriminatory power using finer-granularity calorimeter data to retain the trigger sensitivity to electroweak physics processes at low energy threshold.
In Run 3, the ATLAS front-end detector electronics will remain largely unchanged and the ATLAS Level-1 Trigger latency will still be limited to 2.5 us. The latency budget for the eFEX subsystem is only 13.5 Bunch Crossings (BC). To meet this tight latency requirement, all the eFEX algorithms are implemented in firmware running in modern FPGAs. The whole eFEX subsystem is divided into 24 eFEX modules housed in two ATCA shelves, and each eFEX module holds 4 algorithm processing FPGAs (XCV550T) and one control FPGA. Each module receives data on up to 136 fibre links (11.2 Gb/s) covering a calorimeter area of up to 1.7 x 1.0 (eta x phi). As the eFEX algorithms are based on overlapping windows, the majority of input high-speed links need to be fanned out electrically on-board to multiple FPGAs for the algorithm window environment data sharing, resulting in more than 400 differential high-speed links routed on a single eFEX module. The Trigger OBjects (TOBs) calculated by eFEX algorithms are merged and sorted across the whole module, and only the most energetic TOBs are sent to the L1Topo subsystem over up to 48 fibre links (11.2Gb/s). Upon each L1A, data are collected from various processing stages on the eFEX real-time path, formatted, and sent to L1Calo RODs. This readout function is important for trigger validation and trigger performance analysis. Each eFEX module sends its readout data over 8 electrical links (6.4Gb/s) on the ATCA backplane using multi-lane AURORA protocol, which provides enough bandwidth for both Phase-I and Phase-II readout requirements. The eFEX module control and configuration is done via the IPBus firmware implemented in the control FPGA, which isolates software maintenance issues from the eFEX hardware system. Mission-critical parameters of an eFEX module are monitored by the ATLAS DCS system via an on-board IPMC, which can shut down the module power to prevent hardware damage in case of critical errors such as over-voltage or over-temperature. Non-mission-critical parameters on a eFEX module are collected via IPBus and sent to DCS system.
Following the successful Final Design Review of the eFEX project in Dec 2018, four pre-production eFEX module have been designed and constructed, comprehensive firmware has been developed, and systematic integration tests have been done. This presentation will report the experience of eFEX hardware and firmware development and the integration test results.

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