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Realization of a state machine based detection for Track Segments in the Trigger System of the Belle II Experiment

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The Belle II Experiment relies on an online level 1 trigger system to reduce the background and achieve the targeted frequency of 30 kHz. Here the basis for all trigger decisions based on data from the Central Drift Camber is the track segment finding. To improve both efficiency and maintainability we restructured the original combinatorial approach to finite state machines. The new implementation is saving about 20 % of FPGA slices. To achieve high test coverage an automated test framework was developed for design time validation. Operational correctness is achieved by integration in cosmic ray tests.

Summary

The upgraded SuperKEKB collider is designed to achieve a luminosity of L = 8*10^{(35)} cm^{-2}s^{-1}. As a result higher machine background is expected in the attached Belle II experiment compared to its predecessor Belle. The estimated event rates exceed the targeted trigger rate of 30 kHz. One of the major trigger systems employed to achieve this rate is the trigger system of the central drift chamber at the Level 1. Here the basis for all present trigger algorithms is the track segment finder. Its task is to detect regions of active wires in the detector and combine them into track segments, arrangements of neighboring wires that conform to a predefined geometrical shape. The track segment finder is implemented on XC6VHX565T Virtex 6 FPGAs and integrated close to the detector readout. It has to be efficient and operate in low latency to fullfill the requirements of the entire Level 1 trigger system. An combinatorial approach was in operation for the first phases of the experiment. To increase efficiency and maintainability we decided to restructure this implementation to use finite state machines.

The advantages of the new state machine implementation are the easier expandability as well as the lower resource consumption. By reducing resources, we are able to ease the achievement of timing closure for further iterations of the firmware. Additionally we added a mechanism to reduce transmission of redundant data and thus improve operation by employing suppression of neighboring hits. The overall design is reworked to provide a higher degree of flexibility during design time. We incorporated an approach to adjust track segment finding for predefined regions of the central drift chamber by allowing to load partial special finding configurations. This will allow to easily adjust to geometrical regions with broken wires. As this finding mechanism is based on BRAM, we developed an automated dual and single port inference to keep resource consumption to a minimum. In average the new implementation is capable of achieving a reduction of used Slice LUTs of about 20 \%. To validate the new implementation we developed a test framework that allows to generate testbenches that either support target high test coverage or dedicated detector data patterns to investigate special cases. Correctness within the trigger system is shown by cosmic ray tests.

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