**Introduction**

High Luminosity LHC (HL-LHC) is planned to start operating from 2026, for precise SM measurements and better reach to BSM physics. Its instantaneous luminosity will reach as high as $7.5 \times 10^{34}$ cm$^{-2}$s$^{-1}$ (N.B. peak luminosity is $2 \times 10^{34}$ cm$^{-2}$s$^{-1}$ for Run 2).

To cope with higher $p_T$ collision rate (pileup of as high as 200), trigger and readout systems will be replaced, including those for muon system. The baseline of the hardware trigger is a maximum rate of 1 MHz and 10 μs latency. (N.B. bunch crossing rate is 40 MHz)

Recent R&D results of Level-0 endcap muon trigger are reported.

**Level-0 endcap muon trigger for HL-LHC**

Current endcap muon trigger for LHC (Run 1-Run 3) uses simple coincidence logic in frontend boards, and performs $p_T$ evaluation in backend boards using look-up tables.

For HL-LHC, new hardware-based (Level-0) endcap muon trigger will be installed, to suppress trigger rate and keep high efficiency. Muon candidates are reconstructed with an improved momentum resolution. This is realized by exploiting the evolution of data transmission technologies; all hit data of TGCs are sent to the backend counting room after bunch identification. Also, data of inner subdetectors (inner TGC, NSW, RPC, Tile calorimeter) are sent to the backend counting room. There, muon candidates are reconstructed. Their $p_T$ are determined from the difference of positions and polar angles between track segments in TGC and data in inner subdetectors.

Further, precise determination of $p_T$ is performed using track segments in MDT.

Contribution of "fake muons" (low-$p_T$ charged particles coming from beam pipe) is removed by taking coincidence of track segments in TGC and data from inner subdetectors.

**Hardware implementation**

**Endcap Sector Logic (SL) board:**
It performs several tasks, e.g.:
- Reconstruction of muon track segments in TGC
- Coincidence with other subdetectors
- Data readout

It will be implemented in ATCA blades with a Xilinx Virtex UltraScale+ FPGA (XCVU9P), which has
- approximately hundred pairs of optical GTY transceivers for receiving detector signals
- huge memory resource suited for track reconstruction (UltraRAM)

48 boards are used for the whole system.

**Reconstruction of muon track segments in TGC:**
Important process to determine primitive muon candidates. Proceeds in 2 steps:
1. Determine “position ID” for each of the three stations (M1, M2, M3) by taking coincidence
2. From position IDs, segment $θ$ and $p_T$ are determined using predefined pattern list. (stored in the RAM of FPGA)

**Performance evaluation with software algorithm**

Level-0 single muon trigger performance is evaluated. (N.B. it excludes precise $p_T$ determination using MDT tracks)

**Trigger efficiency:**
Evaluated using Monte Carlo simulation samples of single muons for HL-LHC condition.
- Estimated efficiency > 90%, higher than current (Run 2) system (because of looser coincidence)
- Better rejection of low-$p_T$ muons (because of improved $p_T$ resolution)

**Trigger rate:**
High pileup (up to 200) condition for HL-LHC is emulated by overlaying Run 2 collision data (collected with zero-bias trigger).
For $p_T > 20$ GeV (primary threshold for single muon trigger), rate < 25 kHz. (N.B. for endcap region).

**Demonstration of data transfer**
**Communication between two boards (using GTX transceivers):**
Endcap SL board receives TGC data via optical cables and using recovery clock. This was demonstrated using Kintex-7 FPGAs. No bit error was detected ($BER < 5 \times 10^{-16}$).

**Test of GTY transceiver using loopback module:**
UltraScale+ FPGAs have GTY transceivers. No bit error was detected ($BER < 3 \times 10^{-14}$) at 10 Gbps. Power consumption of hundred pairs of GTY transceivers on a FPGA at 10 Gbps is evaluated to be about 30 W.

**Summary**

Recent R&D results of ATLAS Level-0 endcap muon trigger for HL-LHC are presented. To cope with high $p_T$ collision rate, the system reconstructs muon candidates with an improved $p_T$ resolution. The performance is estimated to have high efficiency (>90%) and rate < 25 kHz. The developments of hardware design, firmware design, and data transfer method are ongoing.