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ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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The design of the Level-0 endcap muon trigger system for the ATLAS experiment at HL-LHC and the status of the development are presented. The new system reconstructs muon candidates with an improved momentum resolution by combining signals from various subdetectors. The trigger efficiency is estimated with Monte-Carlo simulation to be >90%. The trigger rate is also estimated with proton-proton collision data overlaid with one another to account for a pileup condition at
HL-LHC. Track reconstruction hardware based on pattern matching is demonstrated with Virtex UltraScale+ FPGA. The bit error ratio of the data transmission and the power consumption are evaluated.

Summary

The design for the Level-0 endcap muon trigger of the ATLAS experiment at High-Luminosity LHC (HL-LHC) and the status of the system development are presented. HL-LHC is planned to start the operation in 2026 with an ultimate instantaneous luminosity of 7.5 x 1034 cm-2s-1. In order to cope with
the proton-proton collision rate higher than that of LHC, the trigger and readout systems need to be replaced. The new Level-0 endcap muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping the efficiency. That
can be achieved by exploiting the evolution of data transmission technologies to collect signals from various subdetectors in the counting room and form more offline-like tracks. The subdetectors include thin gap chambers, resistive plate chambers, micromesh gaseous detectors, and scintillator-steel
hadronic calorimeters. The combined muon track reconstruction is demonstrated with Monte-Carlo simulation samples produced with the condition at HL-LHC. The efficiency is estimated to be greater than 90%, which is a few percent higher than the current system. The trigger rate is evaluated with proton-proton collision data taken with random trigger overlaid with one another in order to account for a pileup of 200, which is expected at HL-LHC. The obtained value for momentum threshold of 20
GeV, the primary threshold assumed for single muon trigger, is about 30 kHz, which constitutes only about 3% of the assumed total Level-0 trigger rate of 1 MHz. The hardware implementation is planned with ATCA blades. Each blade is designed to have a Virtex UltraScale+ FPGA with approximately
hundred pairs of GTY transceivers, which can be used to receive the detector signals, and with huge memory resources suited for the track reconstruction. The track reconstruction is based on a pattern matching algorithm using the detector hits and the predefined lists of hits corresponding to tracks. A
memory resource of UltraRAM integrated in the FPGA is exploited to store the predefined lists of hits. An initial test with the evaluation kit VCU118 shows a high efficiency and angular resolution better than the requirement. The bit error ratio of the data transmission with GTY transceivers is evaluated
with transfer rates up to 25 Gbps. The power consumption of hundred pairs of transmitter and receiver of GTY running with 10 Gbps, which is an average transfer rate assumed for the system, is evaluated to be about 30 W.

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