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## The hardware demonstrator of the Phase II ATLAS Level-0 MDT Trigger processor

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The selectivity of the current L0 muon trigger is limited by the moderate spatial resolution of RPC and TGC. The MDT chambers currently used for precision tracking will be therefore included to improve the momentum resolution and the redundancy.

A hardware demonstrator of the MDT trigger processor is presented. It consists of an ATCA blade, constructed of two separate modules, and based on FPGA technology. An overview of the explored algorithms for the track finding task will also be shown.

### Summary

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In the Phase-II scheme, the MDT trigger processors will receive MDT hits from the detectors and match them to the trigger candidates (seeds) from the RPC and TGC+NSW trigger chambers. These seeds provide a region of interest (RoI) and the identification of the bunch crossing from which the muon originated. This is the  $t_0$  for computing the MDT drift time from the arrival time of the hit. MDT hits matched to the RoI are then used by the MDT trigger algorithm to improve the momentum resolution, by forming track segments and joining them together for momentum determination.

A hardware demonstrator of the MDT trigger processor is presented. It consists of an ATCA blade, constructed of two separate modules called the “Command Module” and “Service Module”, and based on FPGA technology. An overview of the explored algorithms for the track finding task will also be shown.

**Author:** COLLABORATION, ATLAS

**Presenter:** Dr CIERI, Davide (Max-Planck-Institut für Physik (DE))

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