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EureKA-Maru: an ATCA board for the CMS Phase 2 Tracker Upgrade with centralized slow control and board management solution based on a Zynq Ultrascale+ System-on-Chip

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The Phase-2 CMS tracker back-end processing system is composed by two types of Detector, Trigger, and Control (DTC) boards interfacing the inner and outer tracker, and by the Track Finding Processor (TFP) board performing level-1 track reconstruction from the outer tracker data. Several groups are building hardware to prove key and novel technologies needed in the back-end processing system. EureKA-Maru is designed to contribute to the pool of alternatives a design with an improved thermal performance of the optical transceivers as well as an integrated management solution based on a Zynq Ultrascale+ (US+) System-on-Chip (SoC) device.

Summary

The Phase-2 CMS tracker back-end processing system is composed by two types of "Detector, Trigger and Control" (DTC) boards interfacing the inner and outer tracker, and by the "Track Finding Processor" (TFP) board performing level-1 track reconstruction from the outer tracker data. Several groups are building ATCA hardware to prove key and novel technologies needed in the back-end processing system. EureKA-Maru is designed to contribute to the pool of alternatives. The design improves the thermal performance of the optical transceivers as well as integrates a centralized management solution based on a Zynq Ultrascale+ (US+) System-on-Chip (SoC) device.

EureKA-Maru is designed around a single Virtex US+ FPGA with up to 128 high-speed transceivers, each with a line rate of up to 25 Gb/s. 120 high-speed lanes are connected to Samtec Firefly optical transceivers; four are used for the DAQ path and the remaining four for slow-control and management tasks. The placement of components has been done with the primary purpose of keeping the thermally sensitive optical transceivers with the best cooling possible. The placement also allows a single cable length for all transceivers, therefore, minimizing the bulk cost of Firefly components thereby also reducing the number of spare variants.

The design explores the idea of using an integrated solution for board management and slow control having a plug-in module with a Zynq US+ SoC. The management module provides FPGA logic, high-performance ARM-A53 multi-core processors and two ARM-R5 real-time capable processors. The ARM-R5 cores are used to implement the IPMI/IPMC functionality and communicate via backplane with the shelf manager at power-up. The ARM-R5 are also connected to the power supply (via PMBus), to voltage and current monitors, to clock generators and jitter cleaners (via I2C, SPI). Once full power is enabled from the crate, a Linux starts on the ARM-A53 cores. The FPGA on the management module is used to implement the low-level interfaces including IPBus, or glue-logic. The SoC is the central entry point to the Virtex Ultrascale+ FPGA on the motherboard via IPMB and TCP/IP based network interfaces. The communication between the Zynq US+ SoC and the Virtex Ultrascale+ uses the AXI chip-to-chip protocol via MGT pairs keeping infrastructure requirements in the main FPGA to a minimum.

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