Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade

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ABSTRACT

The pixel-strip modules for the CMS Tracker Phase-2 Upgrade for the HL-LHC integrate a readout hybrid (PS-ROH) for the control and data acquisition link. This hybrid is based on the new, low power and compact gigabit transceiver (LPGBT) and the Versatile Transceiver (VTRx+) specifically designed for the upgrade. A characterization board was first designed to qualify the design rules and the achievable timing performance of the gigabit block. This design enabled the development of the PS-ROH hybrid for the CMS Tracker PS modules. A testing setup was also developed to verify the PS-ROH performance before its integration to the PS modules.

INTRODUCTION

The PS modules contain a strip sensor, a macro pixelated strip sensor of 5×10 cm^2 [3] and two front-end hybrids [2] interconnected with a power hybrid [4] and with an optical readout hybrid [1]. The readout hybrid enables the optical transmission of clock, control and data at transmission speeds up to 10.24 Gbps in the cold and radiation environment of the tracker.

The optical readout hybrid interfaces the two front-end hybrids with the new low power gigabit transceiver LPGBT. This new ball grid array chip provides different transmission modes, high-speed differential ports (e-links), digital input and output control ports and eight analog to digital converter inputs. It provides enhanced clock distribution and phase alignment features.

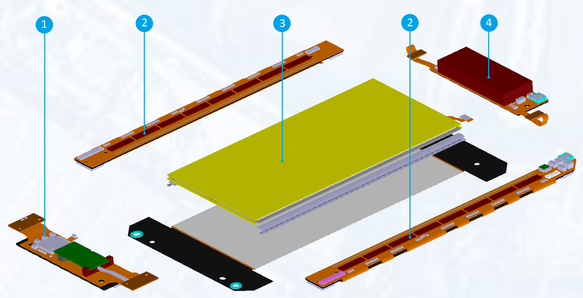


Fig. 1 : PS module - exploded view.

CHARACTERIZATION BOARD

To be able to test all the LpGBT features that are implemented in the PS-ROH, we developed a test board, which represents the reference design for the future LpGBT applications. It is a 6-layer rigid board which gives access to all E-Link groups, data and clocks, the high speed serial data link and contains two different options for decoupling capacitor placement.

[1] Low Power Gigabit Transmitter ASIC
[2] Electrical gigabit link
[3] E-Link input, output and clock divided in four channels
[4] Reference Clock 40 MHz
[5] Phase-Shift Clocks
[6] I2C M/S control connectors
[7] VTRX+ control connector
[8] Configuration switches
[9] Power connector—1.2V

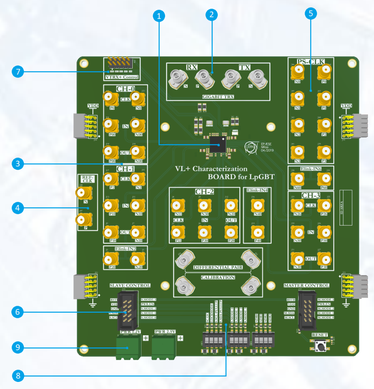


Fig. 4 : Characterization board PCB overview

PS-ROH BLOCK DIAGRAM

Following figure represents the block diagram for all connections of the PS Read Out Hybrid. There are seven high speed differential data lines, two control lines, two clock lines connected to each front-end hybrid, operating at speeds from 320 Mbps to 640 Mbps. A 10.24 Gbps line connects the serial data from LpGBT to VTRx+.

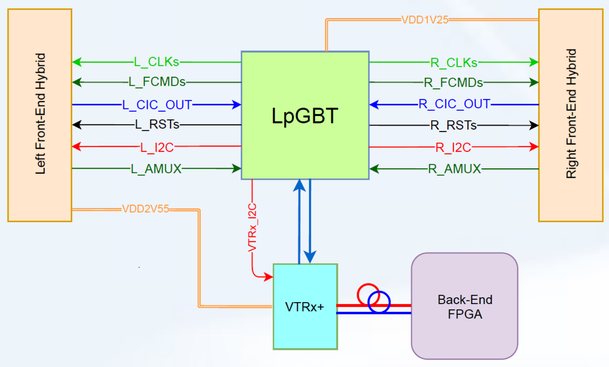


Fig. 2 : PS-ROH block diagram

POWER INTEGRITY

The simulation results for different decoupling options on the Characterization board and on the PS-ROH are shown on the figures bellow. Each figure shows the frequency response of a different decoupling capacitor arrangement with respect to the ASIC.

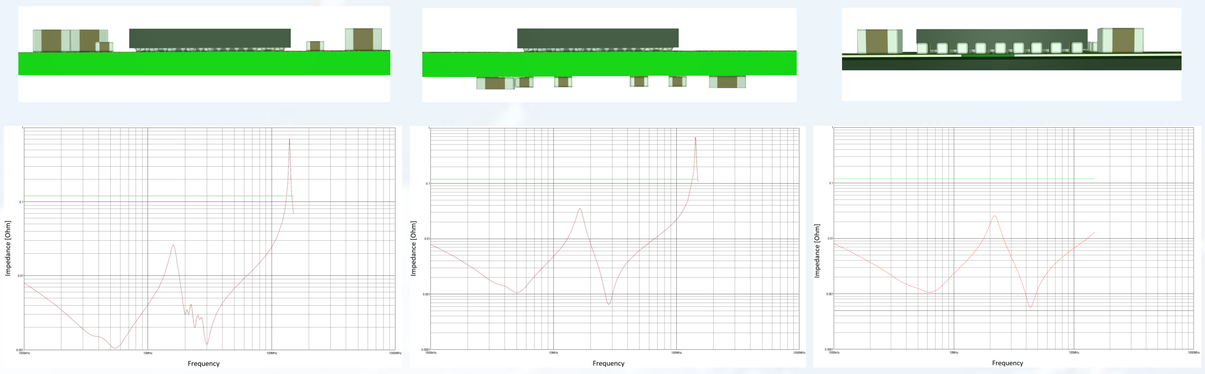


Fig. 5 : Characterization board, capacitors on the same side with the chip

Fig. 6 : Characterization board, capacitors on the opposite side of the chip

Fig. 7 : PS-ROH, capacitors on the same side with the chip

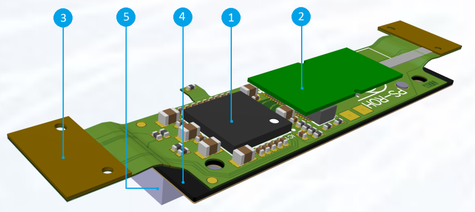
PCB OVERVIEW

The PS Read Out Hybrid board is a 4-layer flex, which is reinforced by a Carbon Fiber stiffener in the central part and FR4 stiffener mounted above the connectors [3]. PS sensor module requires three different thicknesses (1.6 mm, 2.6 mm and 4.0 mm) to be achieved using special shape spacers (Aluminum-Nitride or Aluminum-Carbon Fiber) [5].

The board has controlled differential impedance with two different values, 90Ω on the bottom layer and 100Ω on the top layer.

The board design is finished and sent for fabrication.

[1] Low Power Gigabit Transmitter ASIC
[2] VTRx+ Optical Transceiver
[3] FR4 side stiffener
[4] Carbon Fiber stiffener
[5] AL-CF or Al-N Spacer
[6] Compensator
[7] Fine pitch connector to front-end hybrid
[8] Grounding plugs



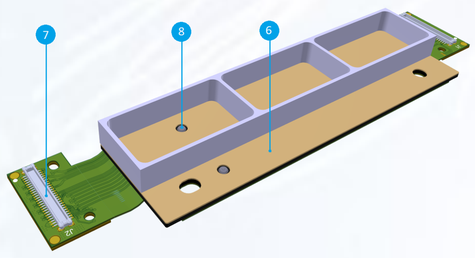


Fig. 3 : PS-ROH board overview

SIGNAL INTEGRITY

The eye diagrams measured on the transmission (TX) line of the Characterization board for both operating speeds with two decoupling configurations are shown in the table bellow. The difference between different decoupling schemes is only visible at the speed of 10.24 Gbps, but signal quality remains good.

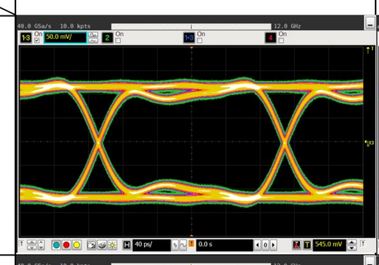
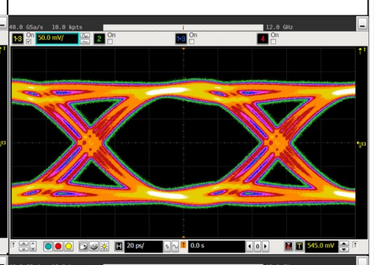
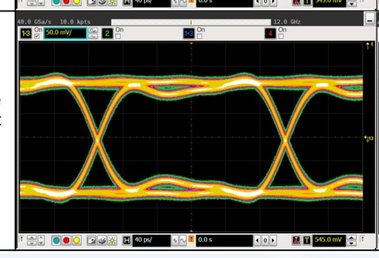
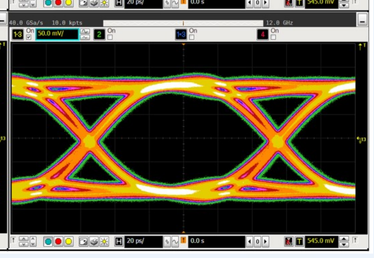
Decoupling \ Speed	5.12 Gbps	10.24 Gbps
Same side as the ASIC chip (TOP)		
Opposite side from the ASIC chip (BOTTOM)		

Fig. 8 : Eye-diagrams of the TX line on the Characterization board

Conclusion

The computer simulation and measurement of S-parameters and eye-diagrams for different configurations on the Characterization board shows that the topology applied in the PS-ROH design has good performance. There are slight differences between the different decoupling schemes, which can be seen on the frequency response graphs and on the eye-diagrams, at higher frequencies. Testing of the features and characterization of the LpGBT chip is successfully done, with the Characterization board. Based on these results, the design was implemented in the PS-ROH.

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