Contribution ID: **80** Type: **Poster**

CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade

Tuesday, 3 September 2019 17:20 (20 minutes)

The CMS electromagnetic calorimeter (ECAL) will be upgraded to maintain detector performance in the challenging environment of the High Luminosity LHC. The front-end readout electronics of the ECAL barrel will be replaced, while maintaining the existing crystals and avalanche photodiodes (APDs). Moreover, the upgrade will optimize the timing resolution of the system. The new front-end electronics consists of two cascading ASICs: a fast, dual gain trans-impedance amplifier (CATIA) and a dual ADC, designed in 130 nm and 65 nm CMOS, respectively. The latest test beam and laboratory test results of CATIA coupled with an ADC will be presented.

Summary

CATIA : APD readout ASIC for CMS phase 2 ECAL electronics upgrade.
The High Luminosity Large Hadron Collider (HL-LHC) program will provide about one order of magnitude of additional integrated luminosity than the current LHC program did after ten years. The impact of the increased luminosity has been carefully taken into account for the current Compact Muon Solenoid (CMS) Electromagnetic Calorimeter (ECAL) barrel detector. Although the legacy crystals and avalanche photo-diodes (APD) will survive the challenging environment of the HL-LHC with acceptable performance, the ECAL readout electronics must be upgraded to accommodate the higher data rates. In addition, to deal with the increase in hit density, CMS is adopting a new strategy for the selection of data by the Level 1 trigger by extending the data retention latency and increasing the granularity by using single crystal information.
The ECAL barrel readout electronics are being completely redesigned to deal with the bandwidth limitation and increase of Level 1 trigger latency. The new ECAL electronics topology is designed for a continuous readout of the detector, displacing to the back-end electronics the Level 1 trigger generation and buffering. Fitting the continuous readout system, the proposed solution for the front-end electronics is a cascade of two custom Application Specific Integrated Circuits (ASICs) : a fast, dual gain trans-impedance amplifier (TIA) —named CATIA—designed in a 130 nm CMOS process and a 12-bit, 160 MSPS dual analog to digital converter (ADC) implementing gain selection and data compression, designed in a 65 nm CMOS process.
Between legacy APD and a new ADC, CATIA has to fulfill the constrains of both old and new electronics system. On one hand, the readout ASIC has to achieve an integral non-linearity (INL) better than ± 0.1 % over 2 TeV of dynamic range. The noise level of the new front-end has to cope with the expected increase of APD leakage current and the loss of transparency of the crystals due to aging. On the other hand, the continuous readout requires the new front end to deliver to the back end electronics a signal shape resolute enough in time to discriminate the anomalous signals due to direct interaction of particles in the APD silicon from the scintillation signals. These requirements are achieved in CATIA by using the high bandwidth provided by a Regulated Common-Gate TIA and a dual gain channel with their differential outputs designed to drive the input stages of the foreseen ADC.
After a first successful prototype in 2017, a full features CATIA (V1) ASIC came back from foundry

in September 2018 implementing the TIA, the two gains, the two ADC driver amplifiers, a 12-bit calibration system, an internal temperature sensor and a triplicated I2C slow control. The latest tests from the former prototype in test-beam and CATIA V1 in laboratory, in both cases driving an ADC as in the final setup, has shown results within expectation.

Primary author: CMS COLLABORATION, CMS collaboration

Presenters: CMS COLLABORATION, CMS collaboration; GEVIN, Olivier (Université Paris-Saclay (FR))

Session Classification: Posters

Track Classification: ASIC