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High-speed design : how to successfully address the high speed challenges : 25Gbps and over

Wednesday, 4 September 2019 10:45 (45 minutes)

Today communication protocols (32Gbps PCIE Gen5, 112Gbs PAM4, ...) and FPGAs transceivers speeds are pushing
designer to hardware designs constraints, PCB material choice and layout constraints that where almost never considered years ago.
This presentation is an extract of a CCES technical training, and its purpose is to cover some of the theorical aspects of “high speed”,
as well as some tricks and traps to be successfull in those coming designs.

Summary

Presenter: CAPITAN, Jean-Michel (Hardware Expert, CCES)

Session Classification: Invited