Contribution ID: **166** Type: **Oral**

Using advanced SoCs at the CERN experiments and accelerator

Tuesday, 3 September 2019 15:45 (45 minutes)

Recent hardware developments in the experiments and the accelerators, especially for the detector readout electronics for the High-Luminosity LHC, are using FPGAs with embedded processors (SoCs).
This is very popular with HW developers due to the close integration between the computing element running a unix operating system and the programmable logic part of the FPGA. For the HL-LHC, there will be of order two to four thousand such devices across CERN experiments (mainly ATLAS and CMS), posing a number of questions about networking, security, operating system support, scalability of the infrastructures and maintainability. The use cases and the integration aspects were discussed at a workshop held at CERN mid-June 2019.
This talk gives a brief summary of the workshop, the use cases, and the thrust at CERN to find common solutions to the integration aspects and long term support for these types of devices in the experiments and more generally across CERN.

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Session Classification: Invited