



Contribution ID: 167

Type: **Oral**

Designing advanced SoCs in technologies down to 28nm CMOS: challenges and solutions.

Wednesday, 4 September 2019 15:45 (45 minutes)

Sub 65-nm technologies can offer to engineers huge advantages for the design of high-density and low power circuits and for the integration of high complexity System-on-Chips. Transistors and gates are almost free for the creative designer, but yet their correct integration requires an exponentially increasing investment in tools and training, and a totally new approach to verification, all the way from the high level system validation to the low-level physical and manufacturing verification. New challenges appear along the design process and have to be consistently addressed by designers and project managers.

First the direct challenges, strongly linked to the technology itself, which are mainly affecting both analog and digital backend flows in multiple aspects: floor-planning, routing, sign-off, power estimation and area reduction. To further complicate this picture, many of these aspects are also subtly intertwined and require often difficult system level decision.

In addition, there are indirect challenges induced by “more than Moore” technologies (e.g. mixed-signal integration and verification), and higher SoC complexity requiring novel functional verification and prototyping methodologies.

This talk will cover in more detail these challenges, focusing mainly around a 28nm technology and will present some of the solutions available to the IC design community. We will also suggest the adoption of some of the most robust design methodology based on existing CAE tools.

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Session Classification: Invited