



Microelectronics User Group Meeting

TWEPP 2019

2-6, September 2019

Santiago de Compostela, Spain

WELCOME!



Agenda

- “Welcome”
by Dr. Kostas Kloukinas (CERN) (5')
- “CHIPS: **CERN-HEP IC design Platform and Services**”
by Dr. Kostas Kloukinas (CERN) (15')
- “Europractice EDA tools for the HEP community”
by Dr. John McLean (Europractice STFC, UK) (15')
- “ASIC support News & Radiation Tolerant device models for 65nm technology”
by Dr. Alessandro Caratelli (CERN) (20')
- “Digital Library Characterization techniques”
by Maxime Barbe (CADENCE VCAD design services) (25')
- “Discussion”

CHIPS:

CERN-HEP IC design Platform & Services

Michael Campbell, Kostas Kloukinas, Francois Vasey
ESE Group, EP Department, CERN

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ASIC design support for HEP

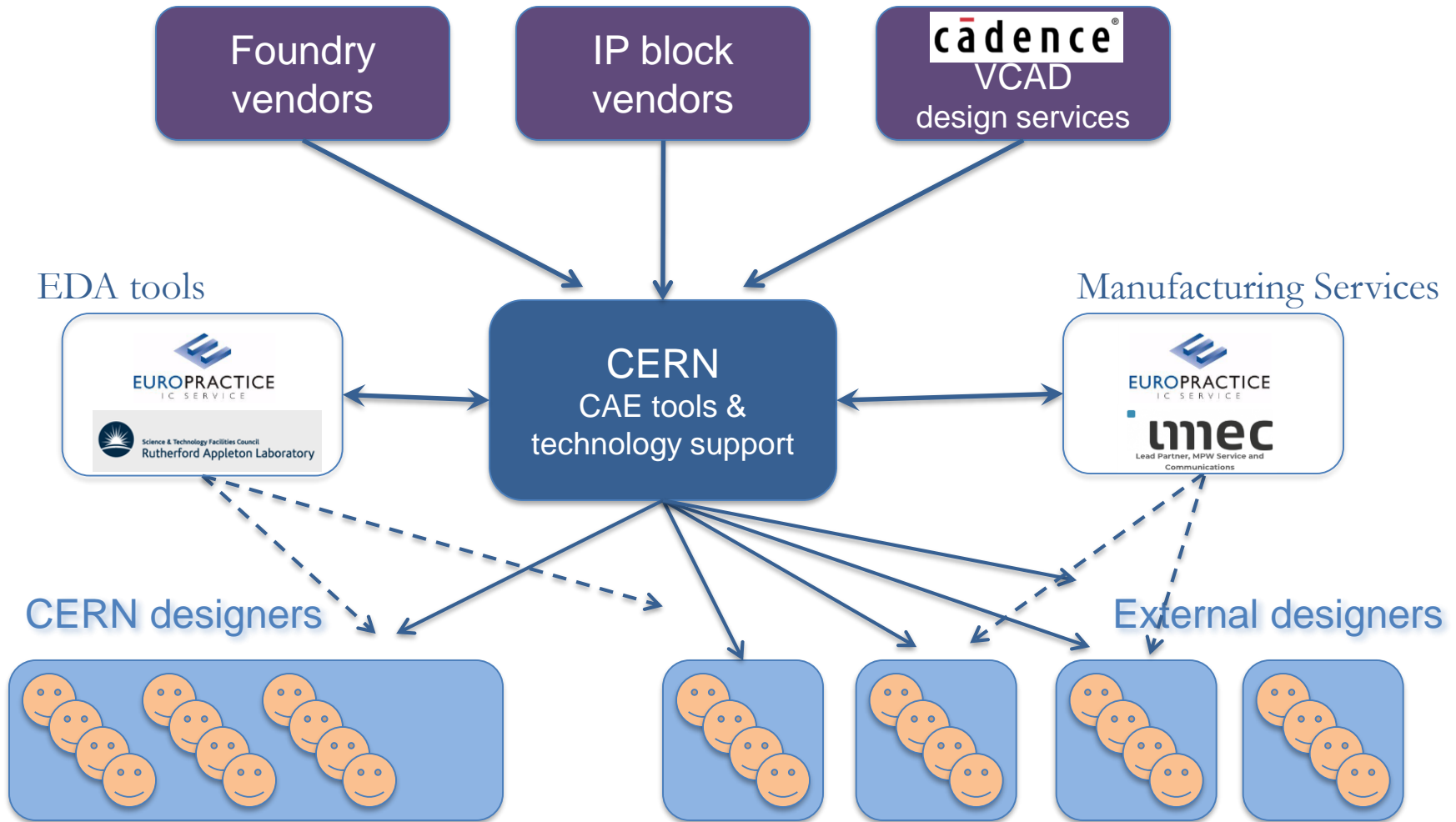
- CERN evaluates and qualifies silicon technology processes

- Provide support to HEP community for selected technologies
 - Technology Support
 - Develop ASIC design platforms for common use
 - Develop specific macro blocks of general use
 - Organize distribution and maintenance
 - Provide technology support to designers

 - Foundry Access Services
 - Establish Commercial Contracts with silicon vendors
 - Develop productive working relationships
 - Establish NDAs that allows for collaborative work
 - Organize & coordinate silicon fabrication



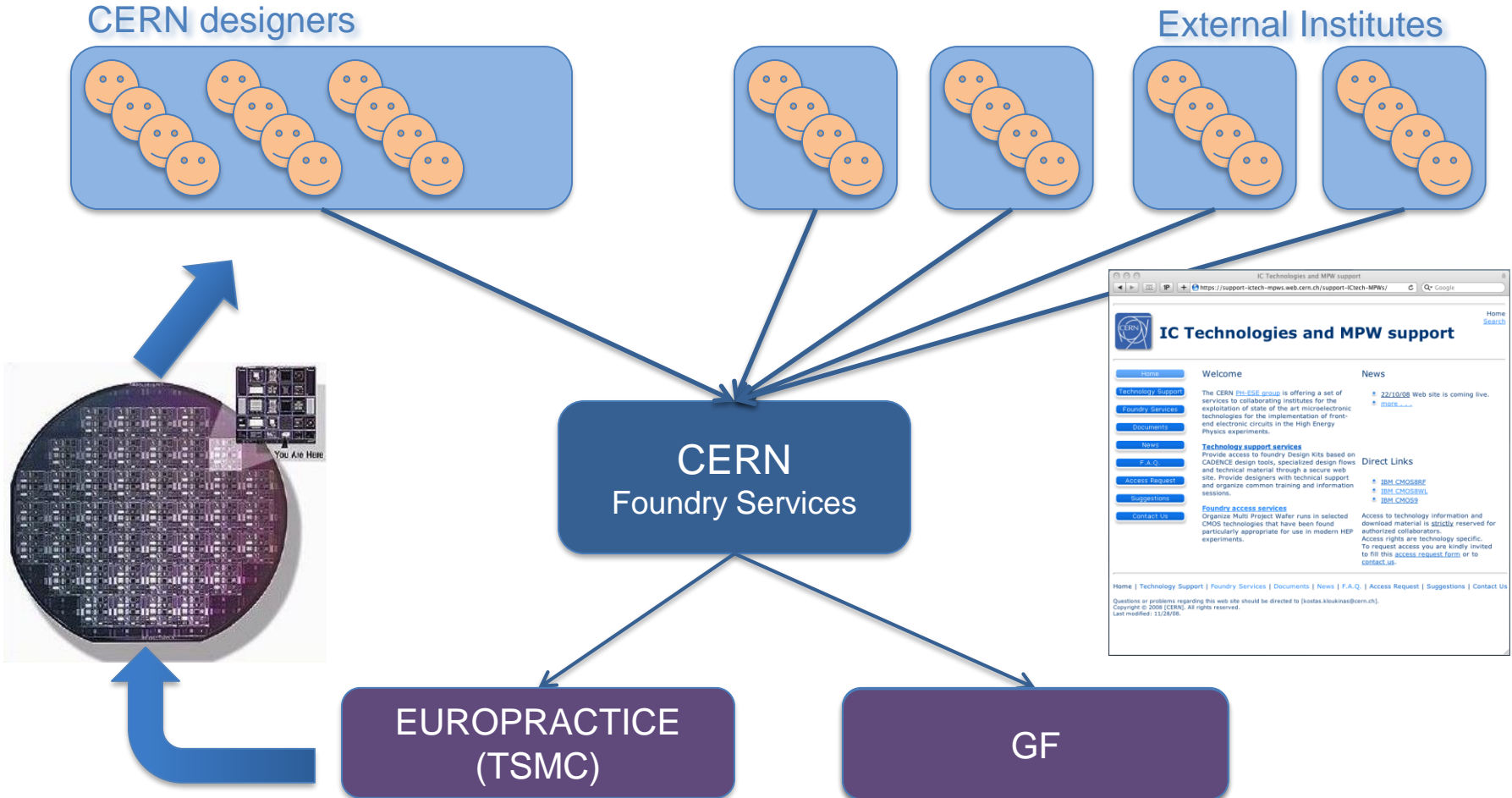
Technology Support





Foundry Access Services

- Organize prototyping Multi Project Wafer runs, for sharing fabrication costs
- Coordinate Engineering & Production runs



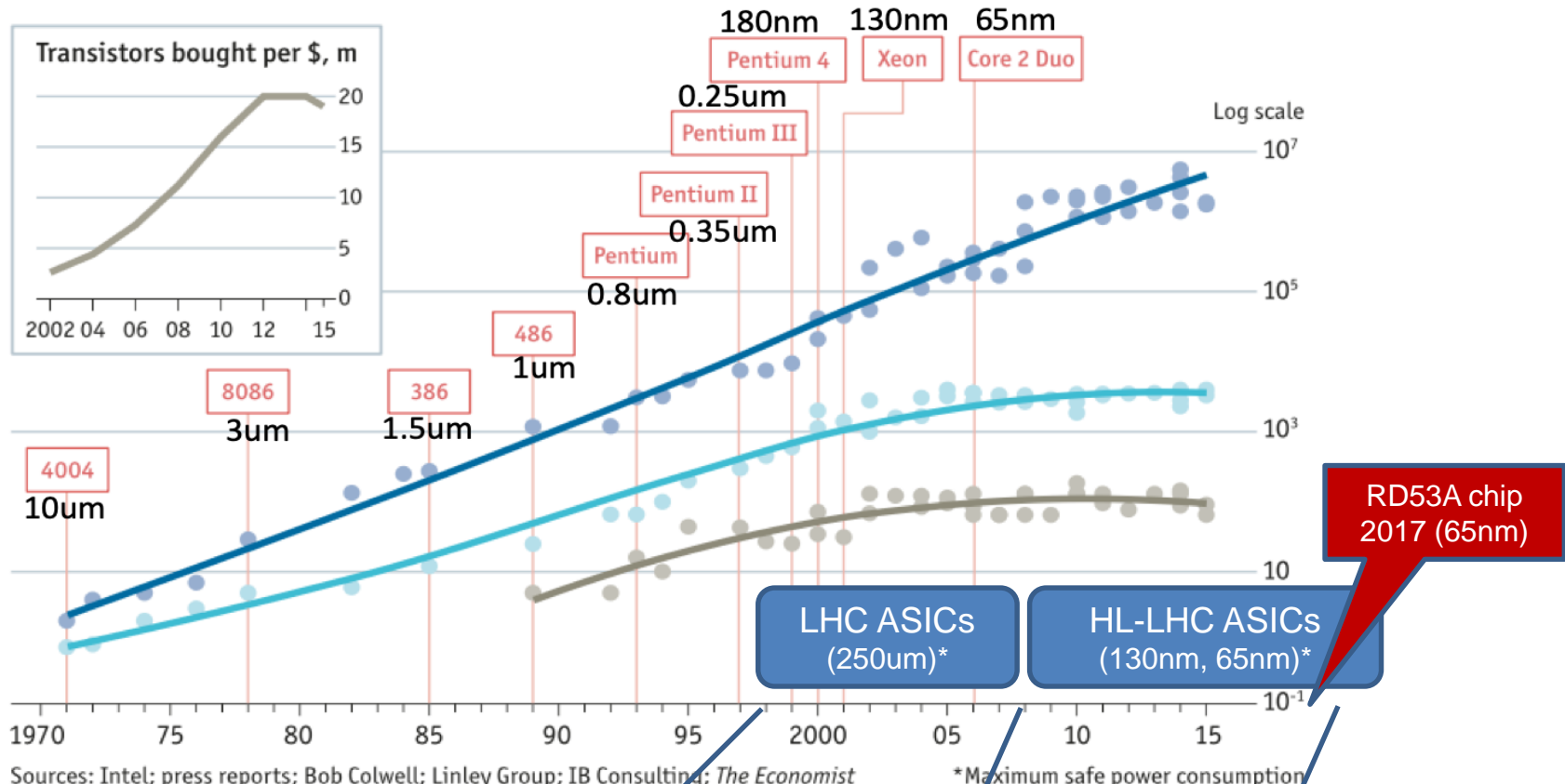


Technology evolution and HEP

Stuttering

● Transistors per chip, '000 ● Clock speed (max), MHz ● Thermal design power*, w

□ Chip introduction dates, selected



Sources: Intel; press reports; Bob Colwell; Linley Group; IB Consulting; *The Economist*

*Maximum safe power consumption

CERN-HEP
Centralized services

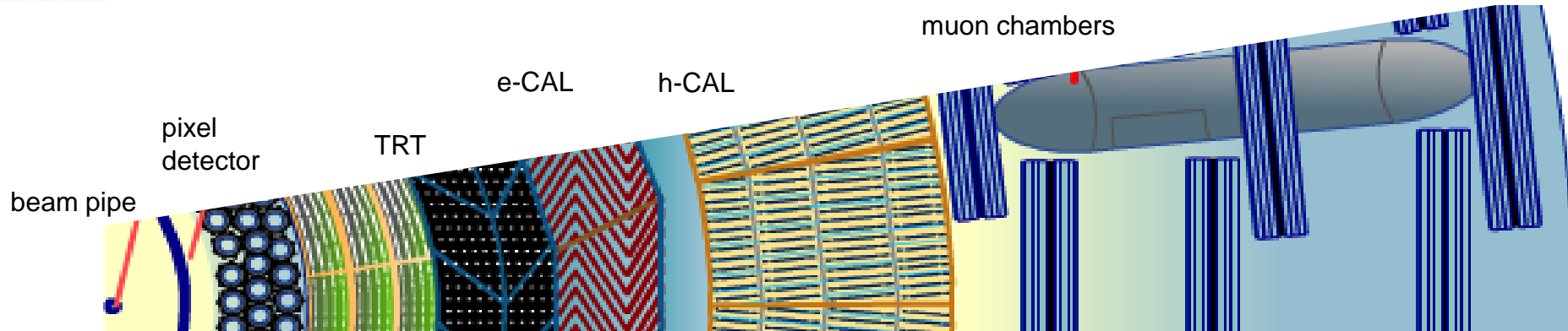
Foundry
Service

Technology
Support

CHIPS



ASICs in ATLAS at LHC



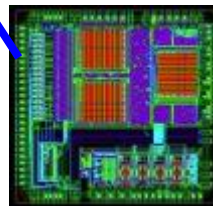
FE-13 pixel det.
28 000 chips
80 M segments
1.7 m² Si sensor



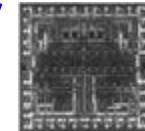
ABCD Si det
50 000 chips
6 M segments
60 m² Si sensor



ASDBLR TRT det
38 000 chips



DTMROC TRT det
19 000 chips



ASD muon det
148 000 chips

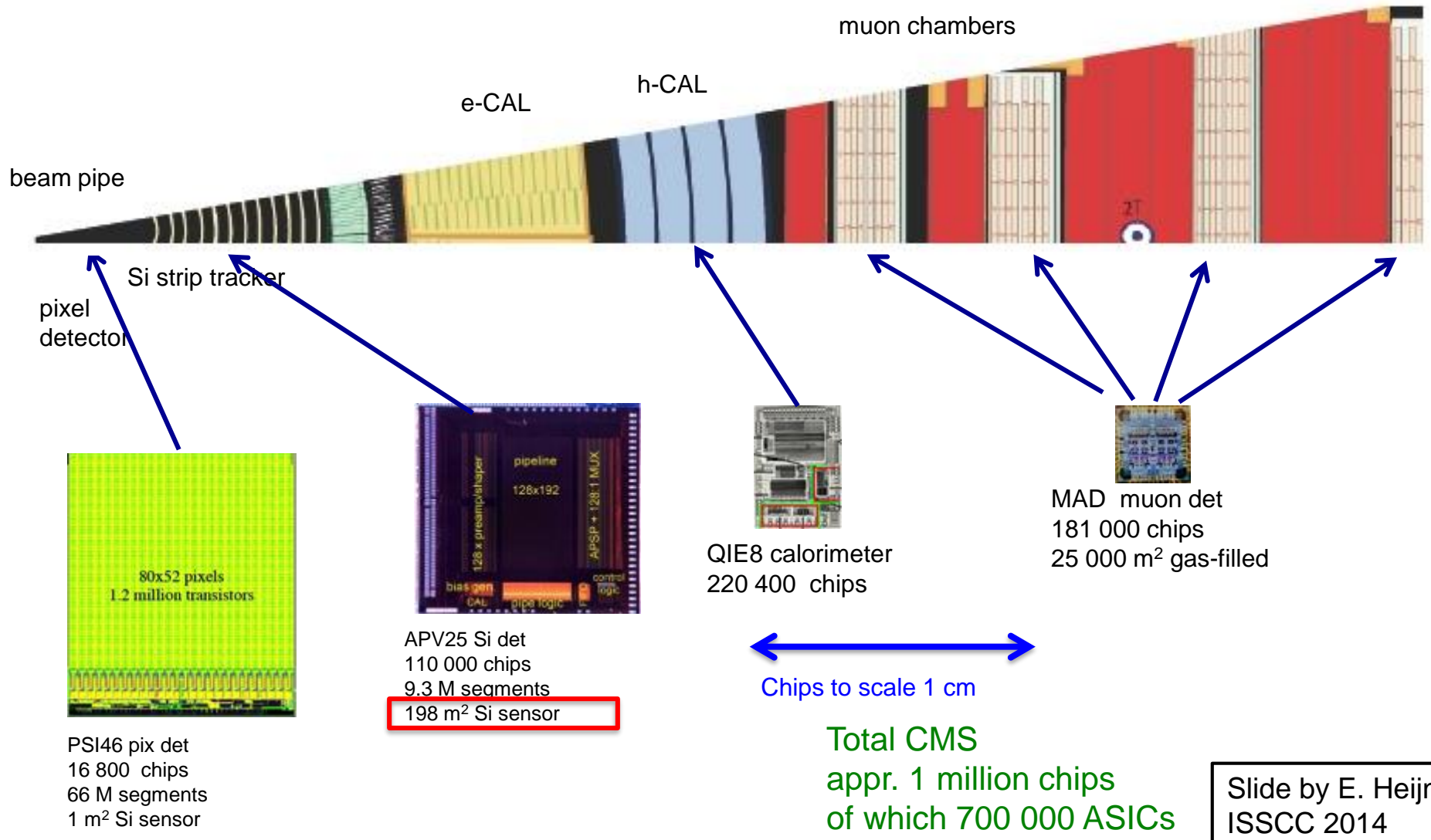
Chips to scale 1 cm

Total ATLAS
100 million sensor cells
appr. 800 000 chips
majority ASICs

Slide by E. Heijne
ISSCC 2014



ASICs in CMS at LHC



Slide by E. Heijne
ISSCC 2014



ASICs for HL-LHC Upgrades

List of ASICs for the upgrade programmes

ALICE (and NA62)
SAMPA, ALPIDE, FEERIC, Non-LHC, TDCpix (NA62)
LHCb
VELO – VeloPix, Upstream Tracker – SALT, RICH – CLARO, SciFi – PACIFIC, CALO – ICECAL, MUON - nSYNC
ATLAS
ITK Pixel, Monolithic Pixel, ITK strips, Lar Calorimeter, HGTD, Muon NSW, Muon MDT, Muon TGC, Muon RPC, Trigger-DAQ
CMS
GEM VFAT3, OT CBC, OT CIC, OT MPA, OT SSA, EB CATIA, EB LITE-DTU, IT ROC, EC Si ROC (HGCROC, H2GCROC), EC TCON, ECON, DCON, EC LDO, BTL TOFHIR, BTL ALDO2, ETL ETROC, CMS CFO
CERN common ASICs
lpGBT, LDQ10, lpGBTIA, GBTX, GBT-SCA, GBLD, GBTIA, FEAST2, bPOL12V, bPOL2V5, linPOL12V, RD53



ASIC design Challenges

- 67 ASICs are being developed
 - Most of them comply with development schedules
 - Many were delayed or required multiple prototyping iterations
 - Few are problematic and might have serious repercussions on the physics programs of the experiments
- The CERN SPC¹ highlighted at its December 2018 meeting (among other things) the challenges associated with ASIC developments in the HEP community and *asked for a coherent plan for dealing with these problems*
- What primarily emerged, is that the complexity of the CMOS processes being used is high and will increase in the future and along with that the complexity of our designs

¹SPC: Scientific Policy Committee
an advisory body to CERN council
<https://council.web.cern.ch/en/content/welcome-scientific-policy-committee>

■ Technology Challenges

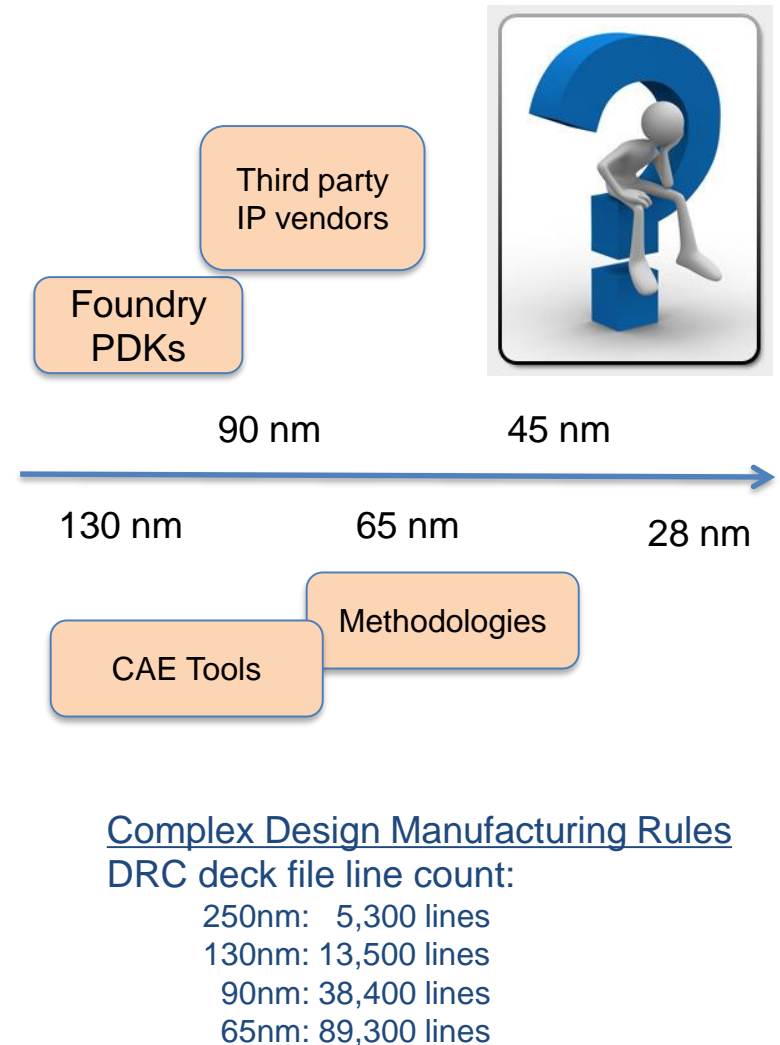
- ❑ Complex deep-submicron technologies
- ❑ Powerful and Flexible CAE Tools but complicated to use

■ Design Challenges

- ❑ Designs of increased complexity (SOC)
- ❑ Mixed Signal designs & IP reuse
- ❑ Vendor IP libraries prepared for digital flows
- ❑ Radiation Tolerance

■ Productivity Requirements

- ❑ Large, fragmented, multinational design teams
- ❑ Designers with different levels of expertise
- ❑ Work on common design projects
- ❑ Expensive technologies
- ❑ Importance of 1st silicon success !





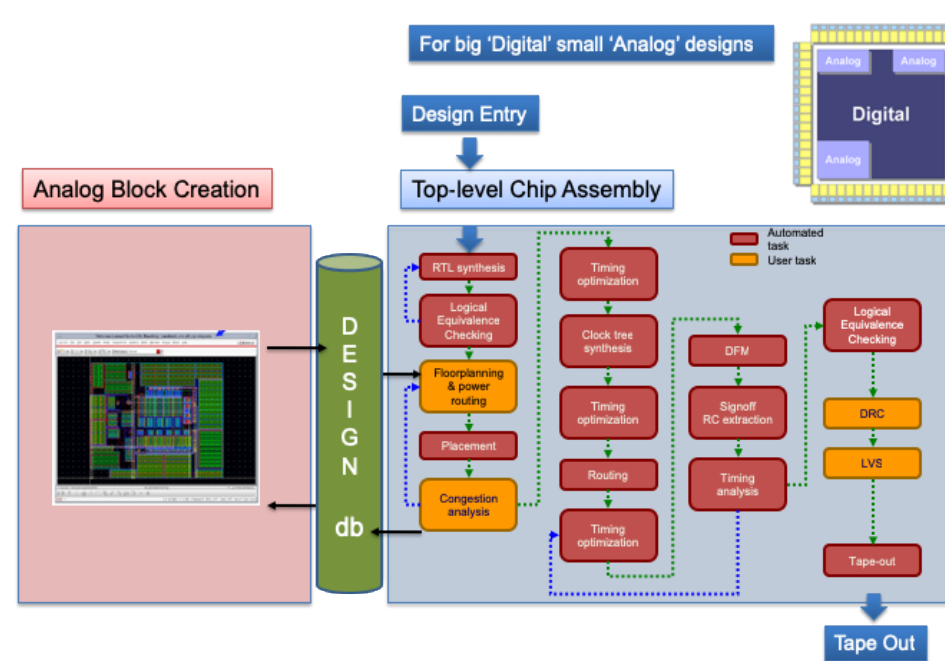
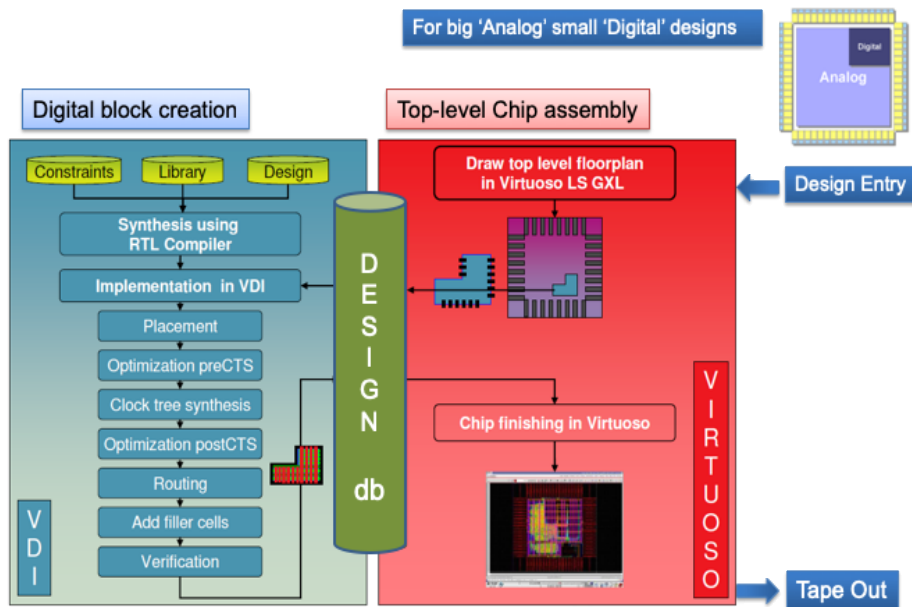
Facing the Challenges

- The *Digital on Top design implementation* and *System Level Verification methodologies* must be adopted systematically to avoid expensive and time-consuming errors even if this implies a significant increase in design time and resources
- The layout of analog blocks for radiation hardness (and Single Event Upset resilience) becomes increasingly challenging and deep expertise is required
- The monolithic integration of sensor and electronics in a single substrate holds great potential for low material budget tracking detectors. However, the added complexity of shielding the sensor from the active readout electronics adds further complexity and requires deep expertise
- As the design community remains geographically scattered and smaller groups may struggle to cope with the new design flows CERN could strengthen training and support

Analog vs. Digital on Top flows

Analog On Top workflow

Digital On Top workflow



Analog on Top - Historical design flow

Blocks are prepared separately then added one-by-one to the design
Ok for small designs but extremely risky for complex ASICs

Digital on Top – New approach for complex designs

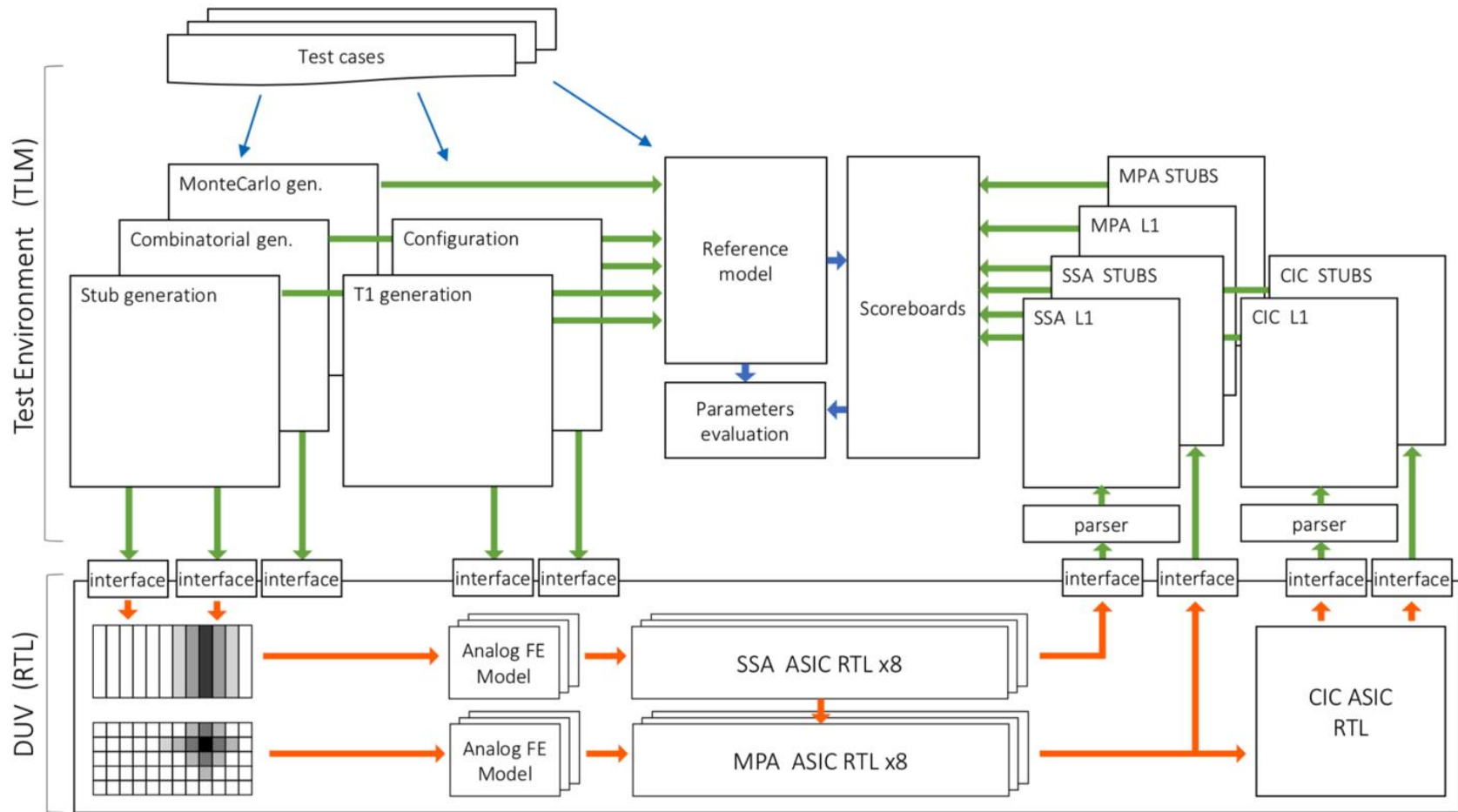
System-on-chip design
High level simulation and verification throughout design
Requires different skill set and generally more resources
Strong mitigation of risk if *all* steps are *fully* followed



System Level verification framework

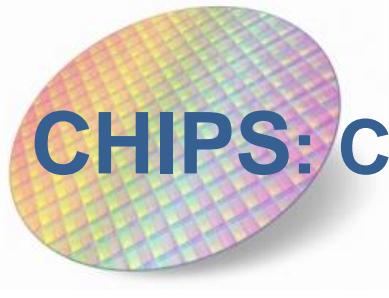
CMS Outer Tracker ASICs (MPA/SSA/CIC) verification framework

Simone Scarfi
Alessandro Caratelli





Support Services in the future



CHIPS: CERN-HEP IC design Platform & Services

- *Strengthening Foundry Services and Technical Support in CERN EP-ESE-ME*
- *Meeting the challenges of present and future CMOS designs in the HEP community and at CERN*



CHIPS Action Plan

3 elements have been identified to meet this challenge

- A. Involve a broader spectrum of experienced practitioners in design support.
- At present a small core team in EP-ESE-ME provides support. It is proposed to redistribute the technical support tasks more uniformly across the experienced designers in EP-ESE-ME. For each step in the design flow one or two specialists will be identified and these will be tasked with supporting outside groups. Such support can only be provided by experienced practitioners
- B. Subcontract specialised tasks
- Reinforce contracts with companies able to give punctual help with particular issues related to the tools and design flow. These facilities should be available both to CERN engineers and to members of the community. As with all such external contracts there should be one person responsible (of course with a back-up) to act as intermediary between the company and the designers
- c. Train and coach
- ❑ Continue to organize formal training sessions to expose designers to the latest tools and, in particular, to educate them in the use of the common design platform.
 - ❑ Furthermore, host designers from the HEP community at CERN in each case for some months per year. Some 'hot desks' could be allocated for such activities



CHIPS Implementation Workplan

- The CHIPS implementation workplan is currently being drafted and will become available towards the end of 2019
- The workplan will cover a five year period: 2020-2024
- The ramping up of the new service and the level of support is a function of the additional resources that will be made available
 - First positions will start in January 2020



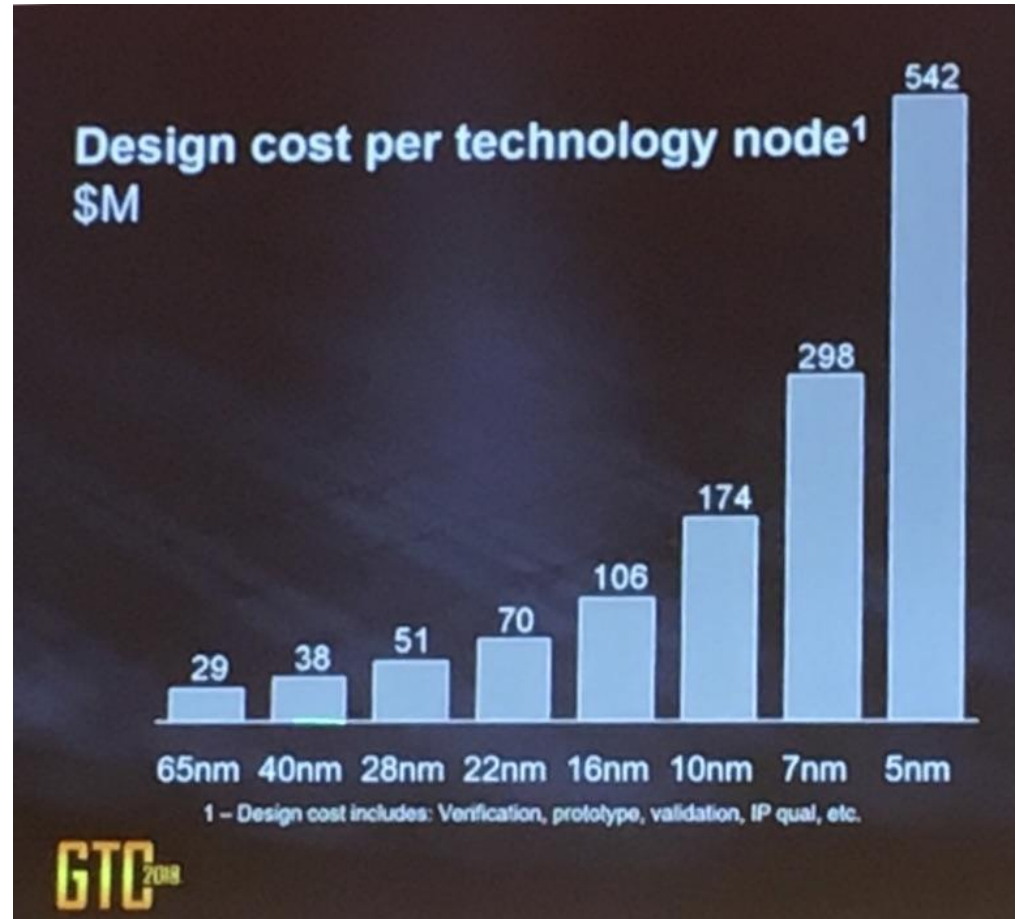
Involving the HEP ASIC community

- ❑ It is important that we continue to benefit from the synergy of efforts within the community
- ❑ The Microelectronics Users Group meetings (which take place annually at the Topical Workshop on Electronics for Particle Physics *TWEPP*) serve as a forum for discussion between designers and design groups. However time constraints limit the depth of discussions
- ❑ It is proposed to reinforce this activity by organizing dedicated MUG meetings where we invite experts from industry to participate and where HEP designers can present their latest work. The format should leave ample time for discussion of strategy and exchanges of technical experience between ASIC designers



IC development costs in industry

Designing ICs is becoming increasingly expensive at the leading edge





**Thank you
for your attention**