TWEPP 2019 – Topical Workshop on Electronics for Particle Physics
2-6 September 2019 – Santiago De Compostela, Spain

CERN ASIC support News and Radiation Tolerant device models for 65nm technology

Alessandro Caratelli, Kostas Kloukinas, Alessandra Fioriti

ALESSANDRO.CARATELLI@CERN.CH

Outline

- Supported Mixed-Signal Design Kits
  - Recent PDKs updates
  - 28nm design kit status
  - Available macro cells
- CERN Design flow
  - Supported design tools for 2019-2020 CERN Design Flow
  - Digital design flow updates
- Useful information
  - ASIC Design Support and Foundry Service webpage
  - Access to the ASIC Support community forum
  - A common UVM verification components library
  - Upcoming tutorial and workshops
- Total Ionizing Dose model for TSMC 65nm technology
  - Project description
  - TID model validation
  - Limitations and usage of the TID models

ASIC Design Support News

Supported Mixed-Signal Design Kits

TSMC

130nm CMOS

Cost efficient technology for Analog & RF designs

PDK UPDATED

130 nm

65nm CMOS

High performance technology for dense designs

65 nm

28nm CMOS

High performance, high density, low power technology

UNDER EVALUATION

28 nm

Global Foundries

250nm CMOS 6SF

END OF SUPPORT

Last tape-out in May 2019

250 nm

130nm CMOS 8RF-DM

Low cost technology for Analog & RF designs

130 nm

28nm CMOS

High performance, high density, low power technology

UNDER EVALUATION

28 nm

TSMC 130nm CERN Mixed-Signal Design Kit update

Update of the TSMC 130nm CERN Design Kit (v2019)

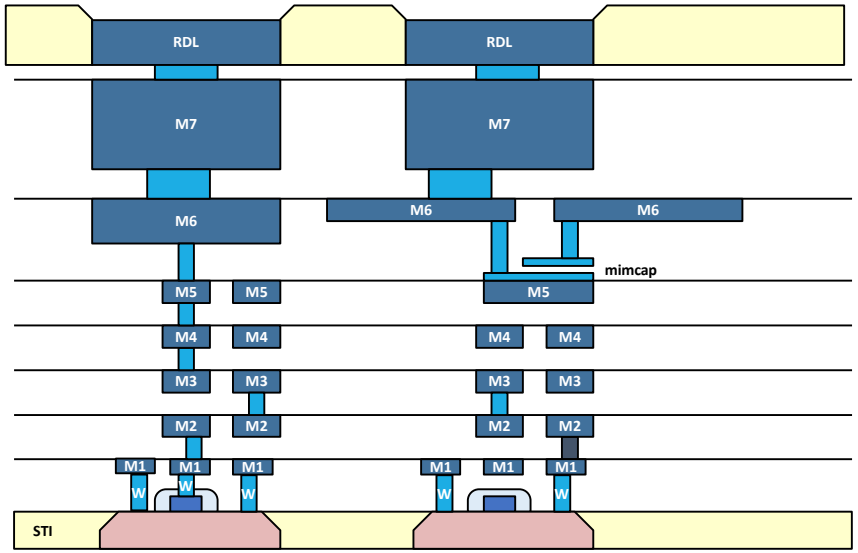
- Technology file update
- Cumulative foundry PDK patches
- Wirebond and flip-chip DRC rules
- Update of the QRC Techfiles
  Signoff extraction was leading to errors in multiple corners analysis mode regarding different VIAs area definition for RV
- Update of the open-access distributed standard cell libraries:
  - Revision of multi-fingers devices in standard cells OA schematic view
  - Solved LVS issues in a subset of digital cells
  - Open access digital library sanity checks and eventual fixes

Work in progress in collaboration with Cadence VCAD
New CERN MS Design Kit availability: **October 2019.**

Users will be notified when the download will be available **via IMEC**

Metal stacks supported:

- **7+1** metal stack
  5 thin – 1 thick – 1 UltraThick – Aluminum RDL



Standard cell libraries available:

- 9 tracks Std-V_T **tcb130ghp**
- 9 tracks Low-V_T **tcb130ghplvt**
- 9 tracks High-V_T **tcb130ghphvt**

TSMC 65nm CERN Mixed-Signal Design Kit update

Update of the TSMC 65nm CERN Design Kit (v2019)

- Technology file update (minor modifications)
- Calibre DRC rules update

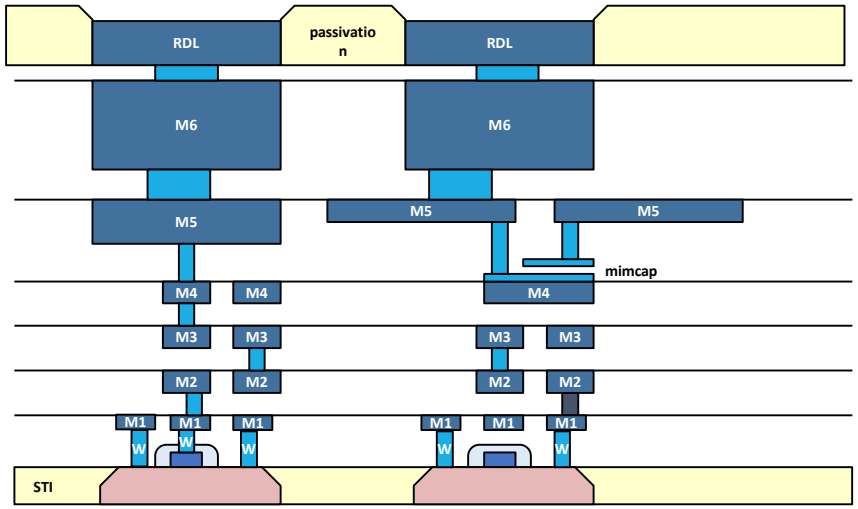
Users **will be notified very soon** and will receive the instructions for downloading the patch from the ASIC support website and for the installation.

Standard cell libraries available:

- 7 tracks Std-V_T / Low-VT / High-Vt
- 9 tracks Std-V_T / Low-VT / High-Vt
- 12 tracks Std-V_T / Low-VT / High-Vt

Metal stacks supported:

- **6+1** metal stack
  4 thin – 1 thick – 1 UltraThick – RDL
- **7+1** metal stack
  5 thin – 1 thick – 1 UltraThick - RDL
- **9+1** metal stack
  7 thin – 1 thick – 1 UltraThick - RDL



28nm technologies

The 28nm technologies are currently under evaluation:

Global Foundry 28nm **TSMC 28nm**

- Exclusive CERN access to the technology information
  - At the moment, CERN is not allowed to distribute the design kits to institutes part of the collaboration
- Radiation performance evaluation ongoing
  - G. Borghello, F. Faccio, A. Marchioro, CERN
  - First results are very promising.
  - A report on the TID performance will be distributed

TSMC 28nm CERN Mixed-Signal Design Kit

- CERN is currently working together with VCAD for building the CERN mixed signal design kit distribution.
- TSMC 28nm technology variants:

HPC

High performances variant

Supported MPW runs:
- Europractice Cybershuttle
- Europractice mini@sic

HPC+

Latest technology version

Supported MPW runs:
- Europractice CyberShuttle

HPL

Low-leakage first version of the technology based on SiON gates.

No CyberShuttle MPW run

LP

Low-power technology variant

No CyberShuttle MPW run

- Digital-cell libraries integration:

Threshold voltage: **UltraLow Vt** – **Low Vt** – **Standard Vt** – **High Vt** – **UltraHigh Vt**

Libraries: **7 tracks** – **9 tracks** – **12 tracks**

Foundry services

TSMC 130nm process

- Cybershuttle MPW runs
  - 1 run/month
- 2 Fabs
  - Fab. 6 (8” wafer), preferred for HEP designs
  - Fab. 12 (12” wafer)

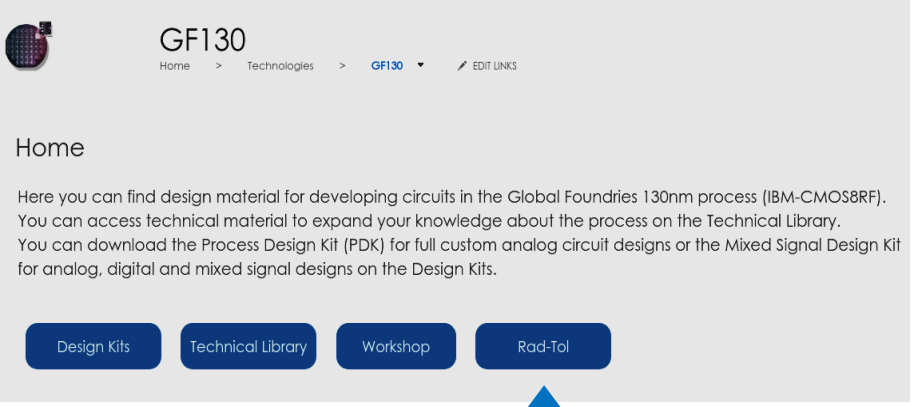
TSMC 65nm process

- Cybershuttle MPW runs
  - ~1 run/month
- mini@asic MPW runs
  - 6 runs/year
  - Cost effective solution for small designs (2mm x 2mm, 1mm x 1mm exclusively for HEP designs)
- 2 Fabs
  - Fab. 12 & Fab. 14 (12” wafer), of equal preference for HEP designs

Macro-blocks available for GF 130nm process

- RadTol ESD structures for IO pads **Silicon Proven**
- RadTol 12-bit, 32-input monitoring ADC **Silicon Proven**
- RadTol LVDS and sLVS drivers/receivers **Silicon Proven**
- SRAM generator (40MHz, dual-port synchronous)
- eFuse (1- and 8-bit; 3.3V-10mA-burn in <1ms for 8 bits) **Silicon Proven**
- RadTol Bandgap (diode based, current output 597 ± 4 mV over P,V,T) **Silicon Proven**
- RadTol DAC: 8-bit, current output, 40 nA LSB **Silicon Proven**

Full list and documentation available at:
https://espace.cern.ch/asics-support/gf130/



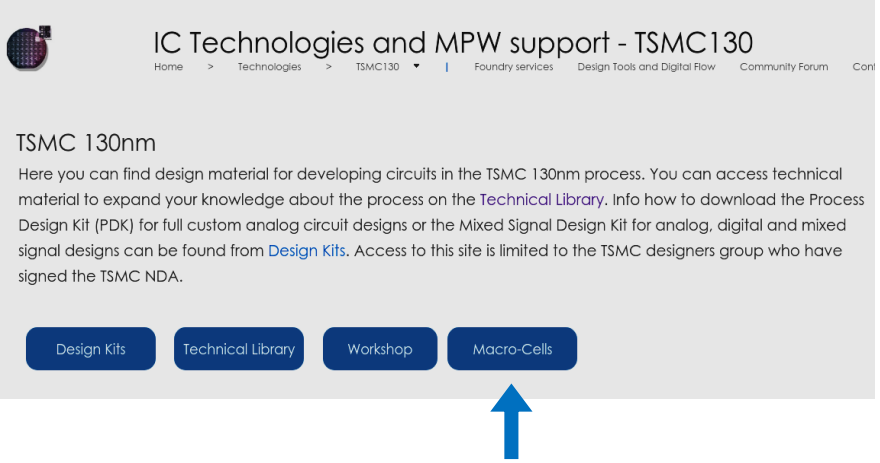
Macro-blocks available for TSMC 130nm process

- Rad-Tolerant SRAM **Silicon Proven**
  - Compiled at request
  - Only Standard-V_T and 4 metal levels used
  - Operation 80 MHz at 1.2 V
  - Dual-port
  - TID and SET tolerant

	Min	Max
Word size:	8b	256b
Mem Depth:	64w	16 kw

- E-Fuse IP block **Silicon Proven**
- Rad-Tolerant Bandgap Reference Voltage generator **Silicon Proven**
- Rad-Tolerant ESD structures for Periphery IO **Silicon Proven**
- Rad-Tolerant CERN IO pads - CMOS driver/receiver 1.2V **Silicon Proven (NEW)**
- Extraction deck files for ELT devices

Full list and documentation available at:
https://espace.cern.ch/asics-support/tsmc130/



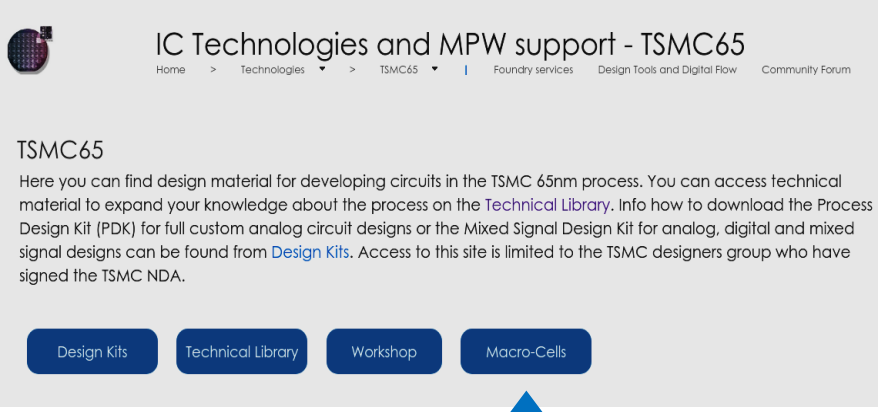
Deliverables available for TSMC 65nm process

- Rad-Tolerant SRAM **Silicon Proven**
  - Compiled at request
  - Only Standard-V_T and 4 metal levels used
  - Operation 80 MHz at 1.2 V
  - Dual-port
  - TID and SET tolerant

	Min	Max
Word size:	8b	256b
Mem Depth:	64w	16 kw

- TSMC Static RAM **Silicon Proven**
  - Compiled at request
- E-Fuse IP block **Silicon Proven**
- Rad-Tolerant Bandgap Reference Voltage Diode Based **Silicon Proven**
- Rad-Tolerant Reference Voltage generator DTNMOS Based **Silicon Proven**
- Rad-Tolerant ESD structures for Periphery IO **Silicon Proven**
- Rad-Tolerant ESD structures for Area array IO
- Rad-Tolerant CERN IO pads - CMOS driver/receiver 1.2V **Silicon Proven**
- Rad-Tolerant SLVS Drivers/Receivers **Silicon Proven**
- Extraction deck files for ELT devices

Full list and documentation available at:
https://espace.cern.ch/asics-support/tsmc65/



CERN Digital Design Flow update:

- Tools version: Cadence Genus/Innovus/Tempus/Voltus v18.10/19.10 (Europractice design tools release)
- Common flow for TSMC 130nm and TSMC 65nm PDKs
- Developed in collaboration with Cadence VCAD
- The flow will be distributed by CERN starting from next week:
  - Information available via the ASIC support website: https://espace.cern.ch/asics-support/
  - Repository link: https://gitlab.cern.ch/asic-design-support

CERN Digital design flow updates

CERN Digital Design Flow update:

- Support for Genus/Innovus **18.10/19.10** version
- Full Open-Access based flow
- Based on the new Stylus Common UI

  Common User Interface and common database access methods offering consistent commands across the whole design flow (Genus, Joules, Modus, Innovus, Tempus, and Voltus tools)
- Initialization Flow with Common MMMC settings file (coming soon)
- Hierarchical flow support
- Folder organization restructuring supporting git/cliosoft repositories
- Voltus power analysis
- C4 flip-chip flow version
- Support for Triple Module Redundancy digital cells place and CTS (SEU tolerant designs)
- Additional minor changes (CTS NDR rules, Timing optimization with QRC extraction and Tempus engine, etc..)

Supported design tools for 2019-2020 CERN Design Flow:

The supported design tool version follow the 2019 Europractice tool release:

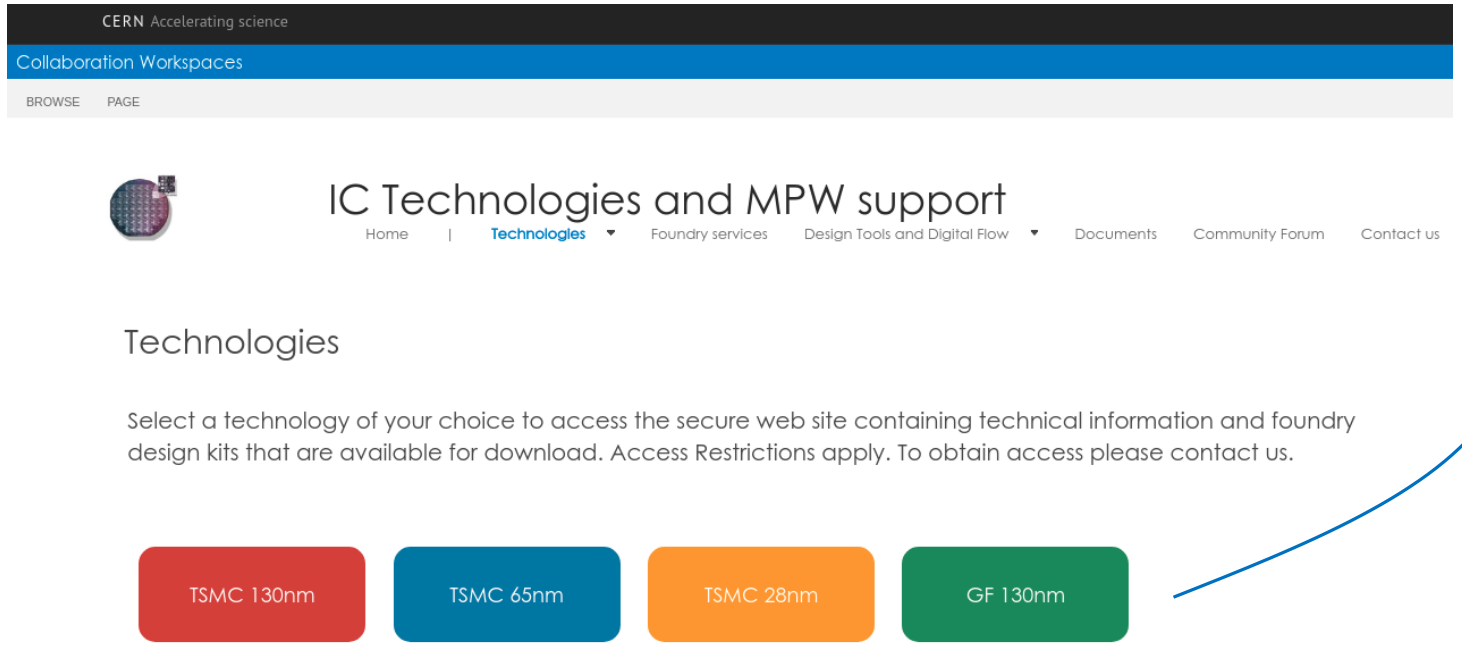
• Digital Synthesis	Genus Synthesis Solution	GENUS_18.10.000
• Digital Implementation	Innovus System	INNOVUS_18.10.000
• Analog design	IC6 Virtuoso	IC_6.1.7.722
• SDC constraints, formal equivalence	CONFRML	CONFRML_18.10.200
• DRC & LVS	PVS	PVS_16.12.000
	Calibre	CALIBRE_2018.4.17
• Parasitic Extraction	QRC/EXT	EXT_18.12.000
• Logic Simulation, Verification Planning	Incisive Verification Platform	INCISIVE_15.20.058
	UVM	VIPCAT_11.30.057_UVM
• Library characterization and validation	Liberate suit	LIBERATE_18.10.293
• Design for testability (DFT & ATPG)	Modus Test Solution	MODUS_18.10.000
• Timing sign-off	Tempus	SSV_18.10.000
• Power and IR-drop analysis	Voltus	SSV_18.10.000

If you need support in the usage of those tools or of the implementation flow, please do not hesitate to contact us!

ASIC Design Support and Foundry Service webpage

- Technical documentation about the TSMC 130nm, 65nm and 28nm design kits
- Distribution of the Global Foundries 130nm design kit
- Training material for digital design tools
- Distribution of CERN digital flows **Updated**
- Distribution and documentation of the available macro cells **Updated**
- Distribution of radiation models for TSMC 65nm technology **Updated**

Link: https://espace.cern.ch/asics-support/



ASIC Support forum

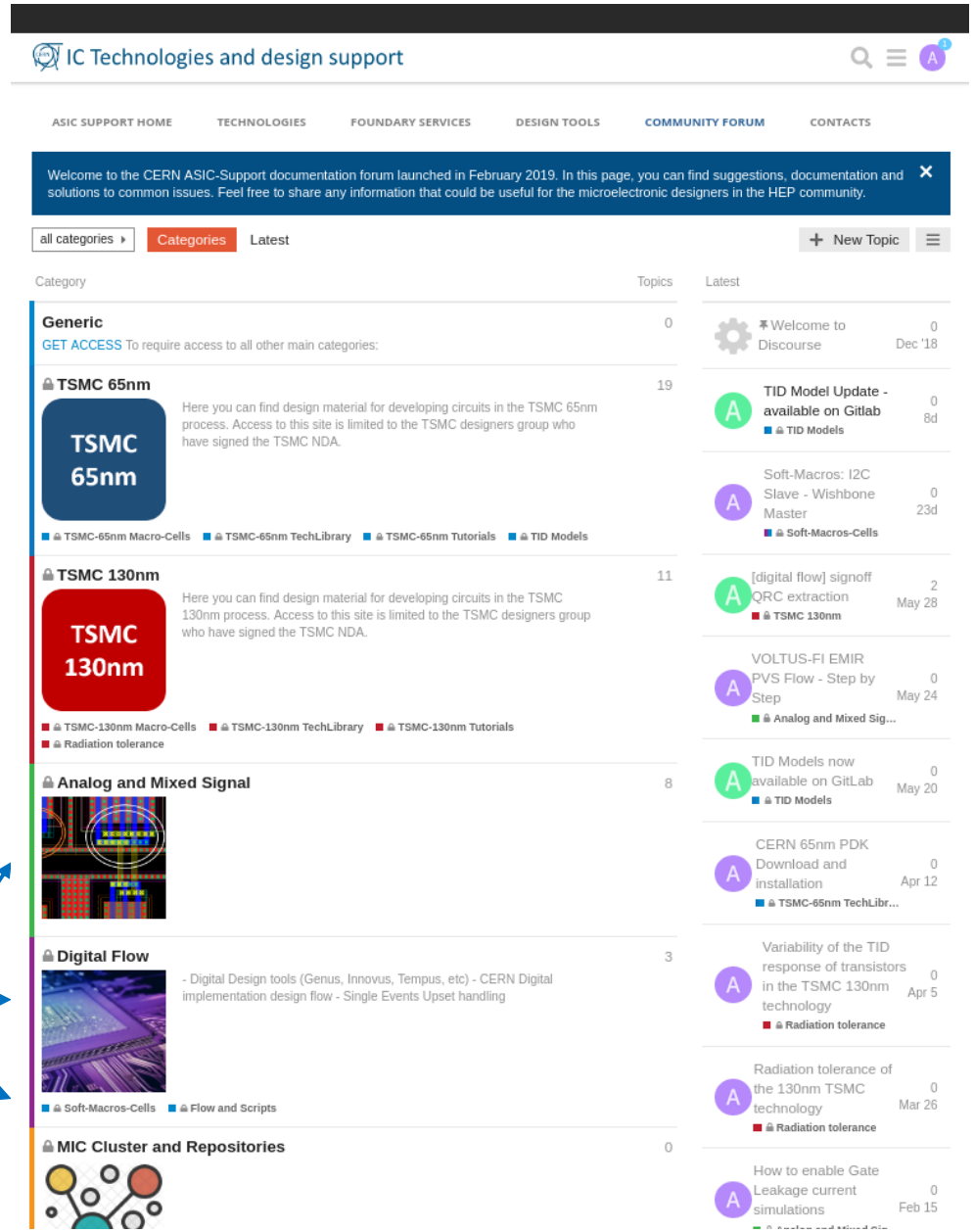
Open on March 2019, the ASIC support community forum is a place where to:

- Find suggestions
- Download documentation
- Search for solutions to common issues to avoid duplicating efforts

You are very welcome to contribute with any information or suggestion could be useful for the community!

Link: **https://asicsupport-community.web.cern.ch**

Access request: **asic.support@cern.ch**



Categories

Sub-categories

A common UVM verification components library

ASIC designers in the HEP community invests significant efforts (as much as on design itself or more) on verification.

↓

Complexity of digital-on-top ASICs have increased strongly in the latest years and, therefore, the verification needs:

- Multi chip systems with critical chip interfaces,
- Functional or gate-level simulation of complex circuits
- Complex stimuli generation depending on physics statistics
- Needs of automatization
- Randomized tests
- Dedicated of very specific/special functions (e.g. handling errors and error recovery)
- Functional coverage
- Exceptional cases/conditions
- In-side design/block assertions (localized intelligent checking: interfaces, busses, etc.)
- Single event radiation effects (SEU/SET) tolerance verification
- Continuous integration

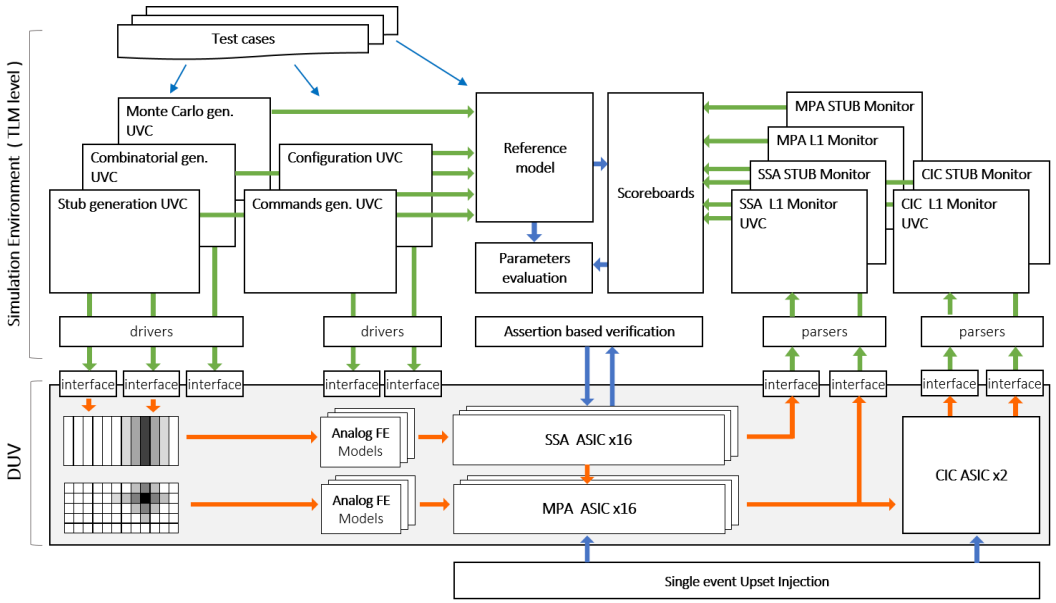
↓

Many recent complex HEP chips verification are based on System Verilog / UVM verification frameworks

A common UVM verification components library

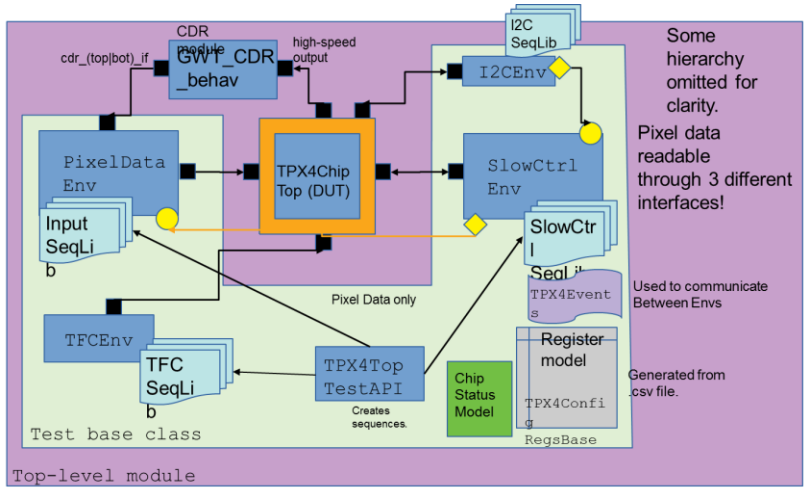
MPA-SSA-CIC Verification environment (CMS Outer Tracker)

Alessandro Caratelli, Simone Scarfi



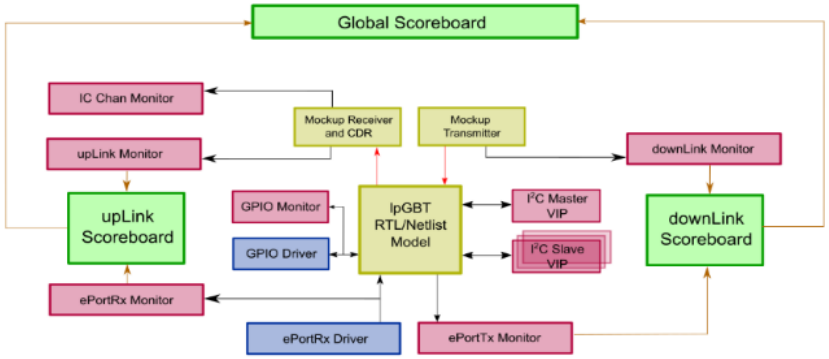
Timepix4 verification environment

Tuomas Poikela



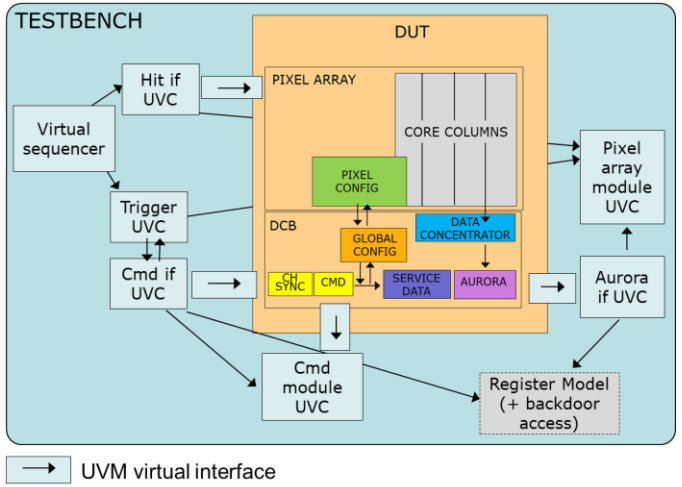
LpGBT ASIC (10Gbps tranceiver)

Szymon Kulis



VEPIX53, Verification Environment for RD53 PIXel chips

Sara Marconi, Elia Conti



A common UVM verification components library

Common HEP microelectronic user library :

Verilog/SystemVerilog modules library

UVM verification components library

- The design of blocks implementing common functionalities as transmission protocols, encoders, and others may require significant amount of design and verification time.
- A Common library of soft-IP blocks including SEU tolerant components can be beneficial for the whole community.
- Re-usable adaptable blocks to do not start from scratch.
- Standardized verification blocks/interfaces
- Common guidelines for integration and reusability.

Upcoming events

- **Digital IC implementation flow and sign-off workshop**

  CERN, October 2019 – CERN EP-ESE in collaboration with Cadence VCAD

Workshop program:

Day 1:

- Digital IC intro
- Timing constraints
- Synthesis and optimization
- Scan test synthesis
- Floorplanning

Day 2:

- Placement
- Timing/Power analysis
- Optimizations
- Routing
- Signal Integrity

Day 3:

- Back-annotated simulations
- Block models generation
- Top level analysis
- Signoff STA with Tempus
- Signoff IR-Drop with Voltus
- Signoff DRC/LVS with PVS
- DRC/LVS with Calibre

Upcoming events

- **SystemVerilog accelerated verification with UVM workshop**

  CERN, January 2020 – CERN EP-ESE in collaboration with Cadence VCAD

  Workshop program:

- Introduction to UVM Methodology and UVC struct.
- Stimulus Modeling
- Simulation Phases
- Test and Testbench Classes
- UVM component classes
- Structure of a simple environment
- Configuration database
- Type Overrides and the Factory
- Constraint layering and behavior modification
- Factories
- UVM Sequences
- Nested sequences and sequence properties
- Objection mechanism
- Virtual SystemVerilog interfaces
- Assigning interfaces using the configuration database
- Integrating multiple UVCs
- UVCs with multiple agents
- Configuration objects
- Multichannel Sequences (virtual sequences)
- Virtual sequencers
- Defining virtual sequences
- Building a Scoreboard
- Connecting components with TLM analysis interfaces
- Hierarchical connections with export
- Transaction-Level Modeling (TLM)
- Scoreboards with TLM analysis FIFO
- Coverage-driven verification overview
- Coverage considerations in a UVC

Design kits and design flow access

CERN → Development of Mixed Signal PDK and digital on-top design flow

IMEC → Distribution of the CERN Mixed Signal PDK and support of the native foundry PDK

For **support** for Design Kits, Workflow, tools, IPs and access requests,
or to get access to the **Digital design flow** scripts and the **Macro-Blocks**::

- Design and PDK support → Contact asic.support@cern.ch (Kostas Kloukinas, Alessandro Caratelli, Alessandra Fioriti)

For **Foundry service requests**:

- Foundry services: → Contact foundry.services@cern.ch (Kostas Kloukinas, Gert Olesen)

To get access to the **Design Kits and PDK**:

- For already inscribed institutes → Contact epsec@imec.be
- For new users → Contact foundry.services@cern.ch

Radiation Tolerant device models for TSMC 65nm technology

TID Models for the TSMC 65nm PDK

Standard CMOS Process Design Kits (PDKs) do not address degradation the technology incurs when exposed to high Total Ionizing Dose (TID). Front-end electronics for HEP experiments is often expected to be exposed up to very high doses.

↓

The development of TID models meant to extends the foundry PDK **to cover high TID effects** and provide an **additional simulation corner** for digital and analog designs and provide an estimation of the device parameters **degradation with TID** while **avoiding to over-constrain** the design.

Aristeidis Nikolaou, Matthias Bucher, Nikos Makris, Alexia Papadopoulou, Loukas Chevas,
Technical University of Crete (TUC), Chania, Greece

Giulio Borghello, Federico Faccio, Alessandra Fioriti, Alessandro Caratelli, Kostas Kloukinas,
CERN

TID Models for the TSMC 65nm PDK

TID models generation steps:

- A test chip was designed and TID measurements have been carried out up to 500 Mrad
  G. Borghello, H. Koch, F. Faccio
  CERN EP-ESE-ME

- Based on the measured data, the TID effects have been fit and modelled (BSIM4, BSIM6)
  M. Bucher, A. Nikolaou, A. Papadopoulou, L. Chevas
  Technical University of Crete (TUC)

- Benchmarks and qualification analysis was performed to evaluate consistency with measured data and operability in a sample design.
  Integration into the 65nm PDK
  A. Fioriti, A. Caratelli, G. Borghello
  CERN EP-ESE-ME

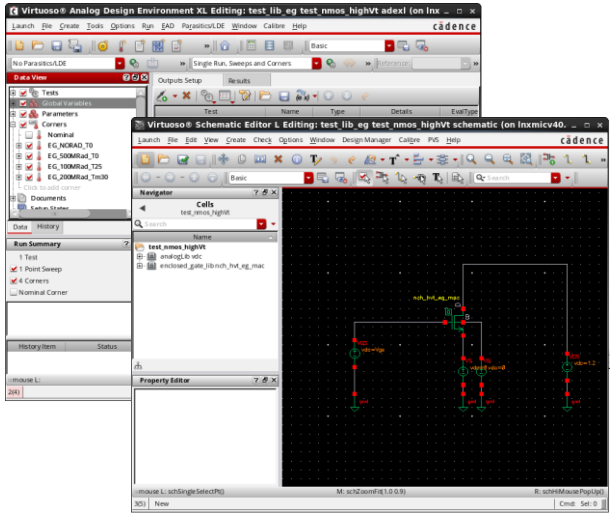
TID Models for the TSMC 65nm PDK

The models are based on:

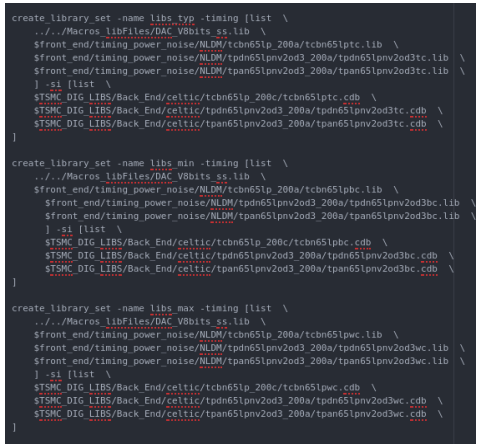
- A test chip designed at CERN including ~100 device sizes per type for linear and enclosed gate transistors
- DC current measurements (V_G swipe - V_D swipe) for multiple V_B
- Irradiated at CERN using an X-Ray radiation source
- TID up to 500 Mrad, at -30°C, 0°C and 25°C
- Annealing effects not taken into account

The models can be used for:

- Analog simulation



- Digital Flow Corner Analysis



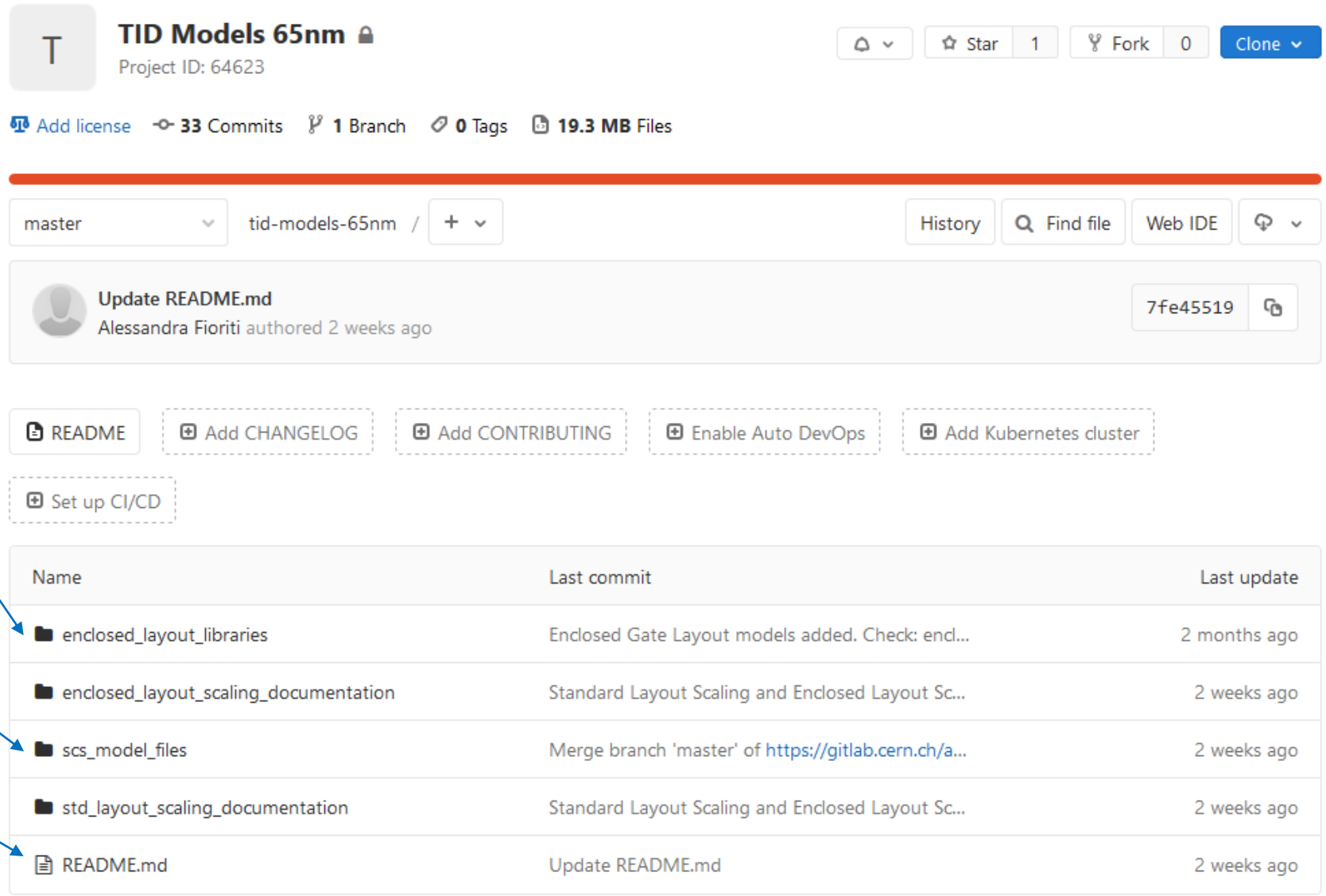
```
create_library_set -name libs_typ -timing [list \
    ../../Macros_libFiles/DAC_V8bits_ss.lib \
    $front_end/timing_power_noise/NLDM/tcbn65lp_200a/tcbn65lptc.lib \
    $front_end/timing_power_noise/NLDM/tpdn65lpnv2od3_200a/tpdn65lpnv2od3tc.lib \
    $front_end/timing_power_noise/NLDM/tpan65lpnv2od3_200a/tpan65lpnv2od3tc.lib \
    ] -si [list \
    $TSMC_DIG_LIBS/Back_End/celtic/tcbn65lp_200c/tcbn65lptc.cdb \
    $TSMC_DIG_LIBS/Back_End/celtic/tpdn65lpnv2od3_200a/tpdn65lpnv2od3tc.cdb \
    $TSMC_DIG_LIBS/Back_End/celtic/tpan65lpnv2od3_200a/tpan65lpnv2od3tc.cdb \
]

create_library_set -name libs_min -timing [list \
    ../../Macros_libFiles/DAC_V8bits_ss.lib \
    $front_end/timing_power_noise/NLDM/tcbn65lp_200a/tcbn65lpbc.lib \
      $front_end/timing_power_noise/NLDM/tpdn65lpnv2od3_200a/tpdn65lpnv2od3bc.lib \
      $front_end/timing_power_noise/NLDM/tpan65lpnv2od3_200a/tpan65lpnv2od3bc.lib \
      ] -si [list \
      $TSMC_DIG_LIBS/Back_End/celtic/tcbn65lp_200c/tcbn65lpbc.cdb \
      $TSMC_DIG_LIBS/Back_End/celtic/tpdn65lpnv2od3_200a/tpdn65lpnv2od3bc.cdb \
      $TSMC_DIG_LIBS/Back_End/celtic/tpan65lpnv2od3_200a/tpan65lpnv2od3bc.cdb \
]

create_library_set -name libs_max -timing [list \
    ../../Macros_libFiles/DAC_V8bits_ss.lib \
    $front_end/timing_power_noise/NLDM/tcbn65lp_200a/tcbn65lpwc.lib \
    $front_end/timing_power_noise/NLDM/tpdn65lpnv2od3_200a/tpdn65lpnv2od3wc.lib \
    $front_end/timing_power_noise/NLDM/tpan65lpnv2od3_200a/tpan65lpnv2od3wc.lib \
    ] -si [list \
    $TSMC_DIG_LIBS/Back_End/celtic/tcbn65lp_200c/tcbn65lpwc.cdb \
    $TSMC_DIG_LIBS/Back_End/celtic/tpdn65lpnv2od3_200a/tpdn65lpnv2od3wc.cdb \
    $TSMC_DIG_LIBS/Back_End/celtic/tpan65lpnv2od3_200a/tpan65lpnv2od3wc.cdb \
]
```

The models includes all combinations of:

- Transistor Type:
  - pMOS
  - nMOS
- Layout:
  - Enclosed Gate
  - Standard layout
- Dose:
  - 100Mrad
  - 200Mrad
  - 500Mrad
- Temperature:
  - -30°C
  - 0°C
  - +25°C
- Threshold voltage:
  - Low Vt
  - Std Vt
  - High Vt
- Process Corner:
  - Typical
  - Fast
  - Slow

TID Models access

link: https://gitlab.cern.ch/asic-design-support/tid-models-65nm



Enclosed Gate Layout Virtuoso Library

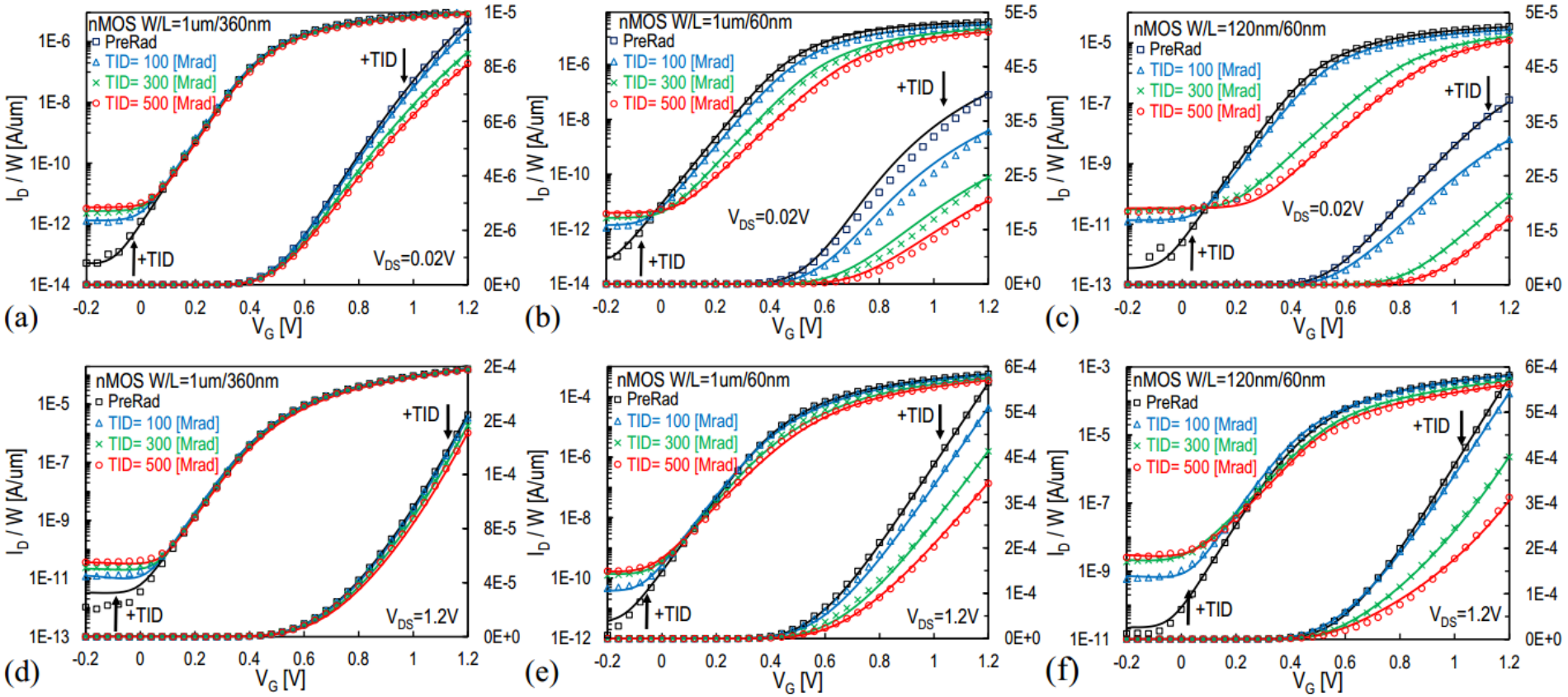
TID transistor models (.scs)

Documentation

TID measurements

Example of experimental data:

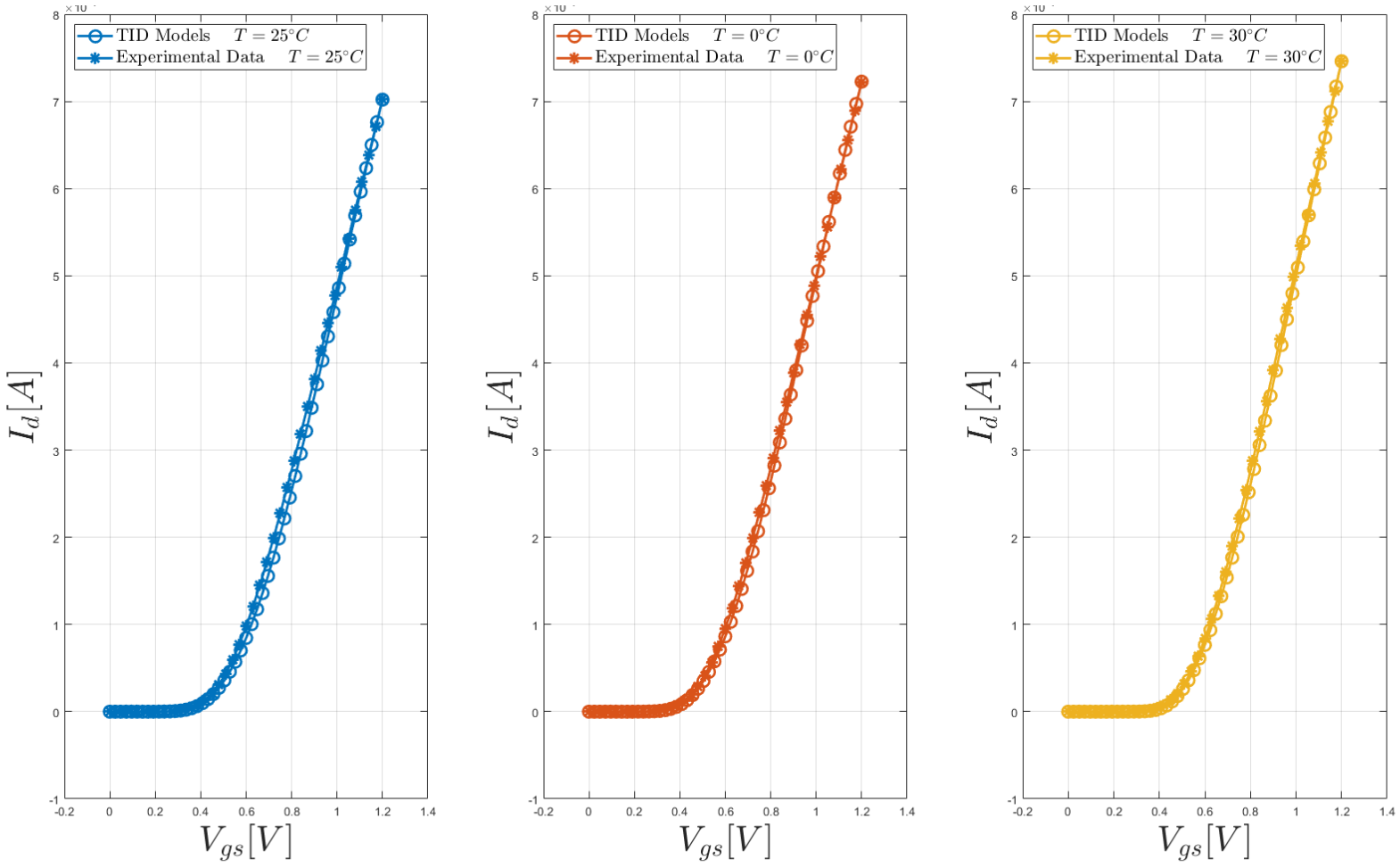
- Transfer characteristics of nMOSTs in linear (a), (b), (c) (VDS=20mV) and saturation (d), (e), (f) (VDS=1.2V) modes for pre-rad and TID of 100, 200 and 500 Mrad, at 25°C
- Threshold variation (narrow channel effects)
- Transconductance variation (short channeleffects)



TID models comparison with experimental data

Analog simulation results comparison with experimental measurements:

- For nMOS | Standard-Vt | V_{DS}=1.2V | Process = Typical | TID=100 Mrad | BSIM4 model

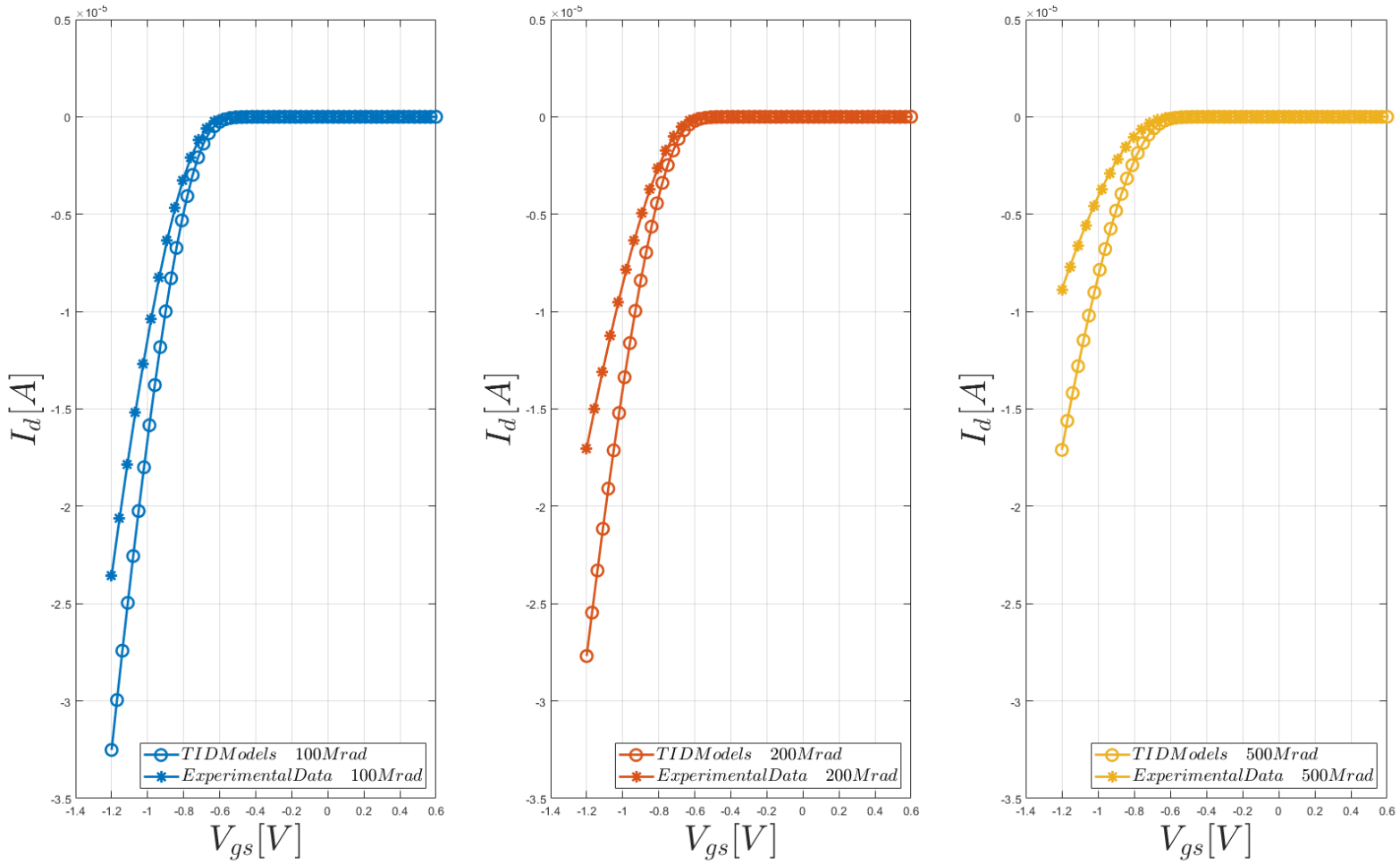


Standard-Vt devices models show in general a very good matching with experimental data for all temperatures and ionizing doses.

TID models comparison with experimental data

Analog simulation results comparison with experimental measurements:

- For pMOS | High-Vt | V_{DS}=1.2V | Process = Typical | T = 0ºC | EKV (BSIM6) model

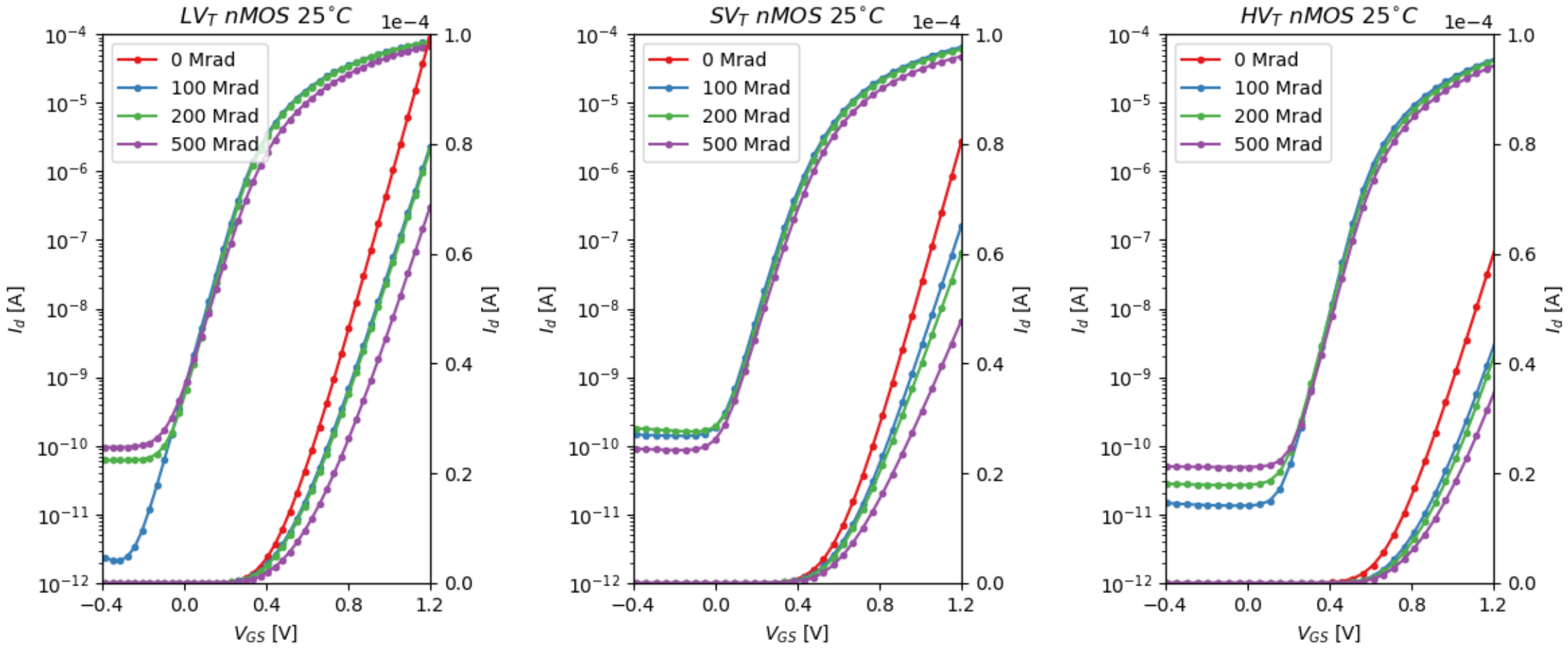


High-Vt devices models show in general a worst case analysis behavior compared to the experimental data.
At lower doses, the matching is more accurate.

TID models self consistency analysis

Analog simulation of Id current variation due to TID:

- For nMOS | V_{DS}=1.2V | Process = Typical | T = 25ºC | LVt-SVt-HVt | BSIM4-BSIM6 models

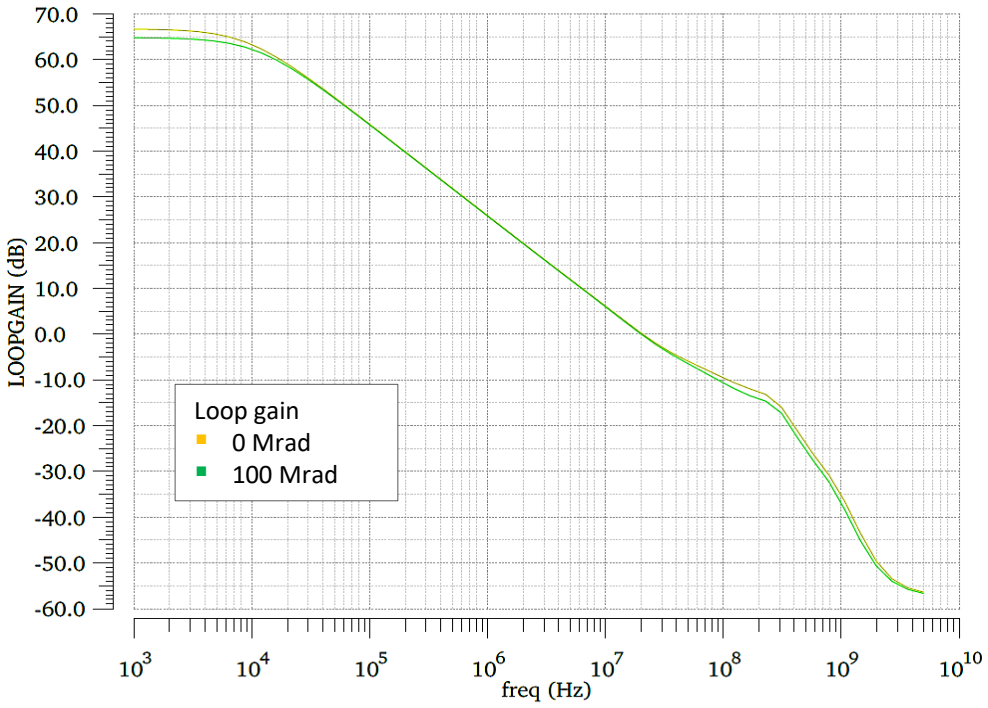


TSMC 65nm TID Models: usage example in Virtuoso

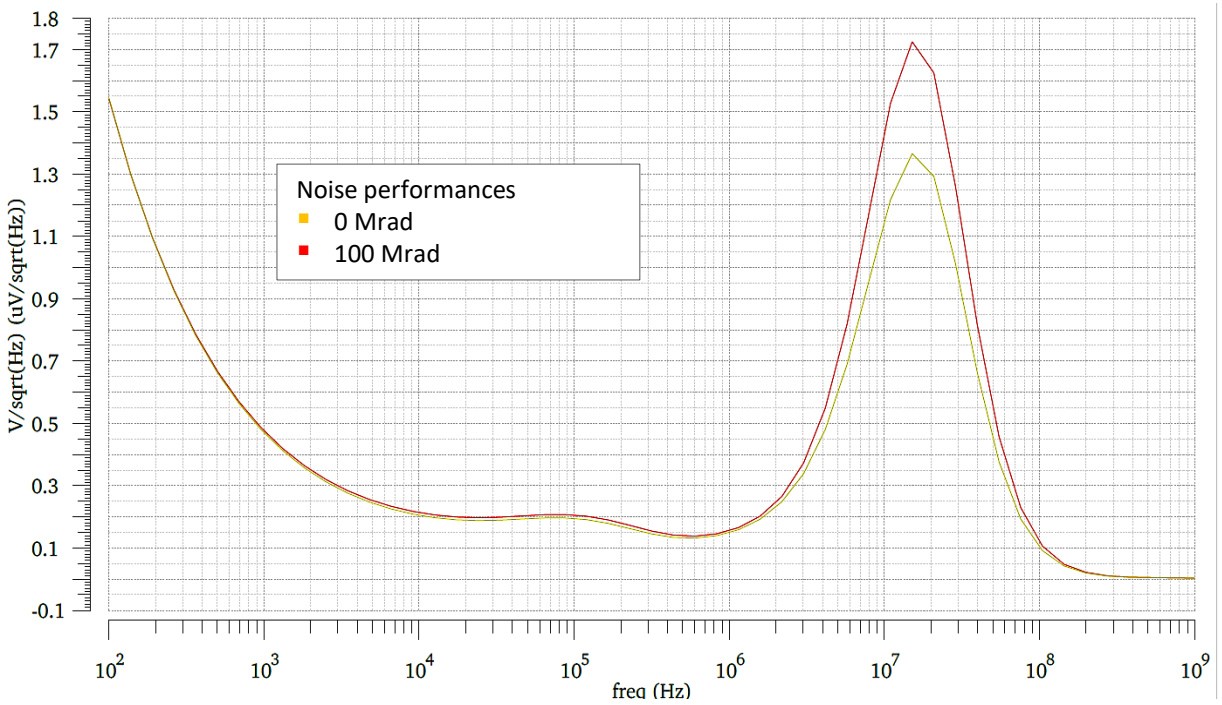
Test-case: the SSA front-end (the readout ASIC for the CMS Outer Tracker HL-LHC upgrade)

- TID effects on the noise are not directly taken into account in the models and in the measurements
- The models allow anyway to perform AC and noise simulations providing consistent results

Loop-gain



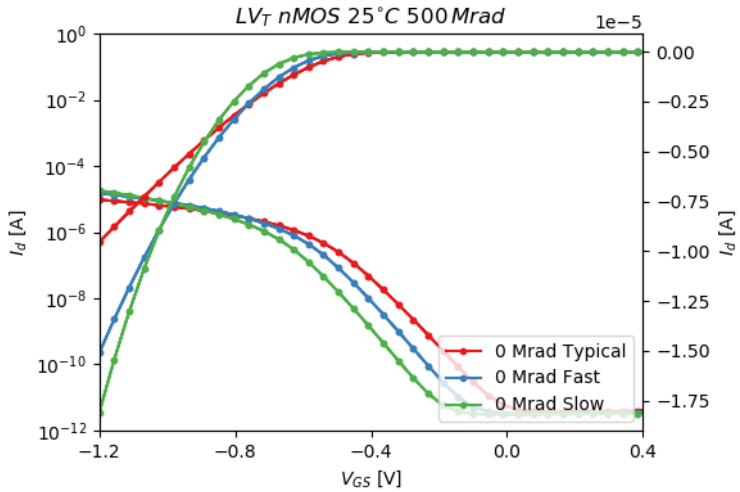
Noise performances



TID Models limitations

Main limitations:

- The models are based on a single measurement per transistor dimension, type and nominal Vt.
- Due to the limited statistics the TID models should not be used as design corners.
  The TID models should be used exclusively as an additional simulation corner to the standard TSMC ones.
- The models are based on worst bias condition measurements, representing therefore a pessimistic case analysis.
- Experimental measurements are assumed as typical corner.
- Corner variability is consistent with the TSMC models for devices modeled as BSIM4 (Std-Vt linear-gate devices) but it requires improvements for the Low-Vt devices. It is not suggested therefore to combine process and TID variation in the same simulation.



Digital library characterization

- Re-characterization of the standard cell digital libraries (CERN – VCAD collaboration)
  - 100 Mrad: **9 tracks – SVt – TYP – 100 Mrad** **9 tracks – HVt – TYP – 100 Mrad** **9 tracks – LVt – TYP – 100 Mrad**
  - 200 Mrad: **9 tracks – SVt –TYP – 200 Mrad** **9 tracks – HVt – TYP – 200 Mrad** **9 tracks – LVt – TYP – 200 Mrad**
- The re-characterization of additional libraries or corners will be evaluated according request

Thank you!