Focal Plane Processing in Standard CMOS Technologies

Photodiode Modeling and Characterization

CMOS Vision Sensors

Micro-Light Energy Harvesting

Topical Workshop on Electronics for Particle Physics, TWEPP-2019
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CAMPUS VIDA CAMPUS DE EXCELENCIA INTERNACIONAL

CiTIUS Centro Singular de Investigación en Tecnoloxías Intelixentes

Outline

- **Vision –** Analog to Information Conversion (AIC) by means of focal plane processing in standard CMOS technologies.

- **Mission -** Change of paradigm from *big data* to *smart data*.

  Development of new solutions extracting *information* from the environment *rather than* simply massive amounts of raw *data*, efficiently *reducing bandwidth and power* consumption. The use of standard CMOS technologies favors the development of *low cost* solutions.

  Vertical approach: from sensing to processing to energy autonomy

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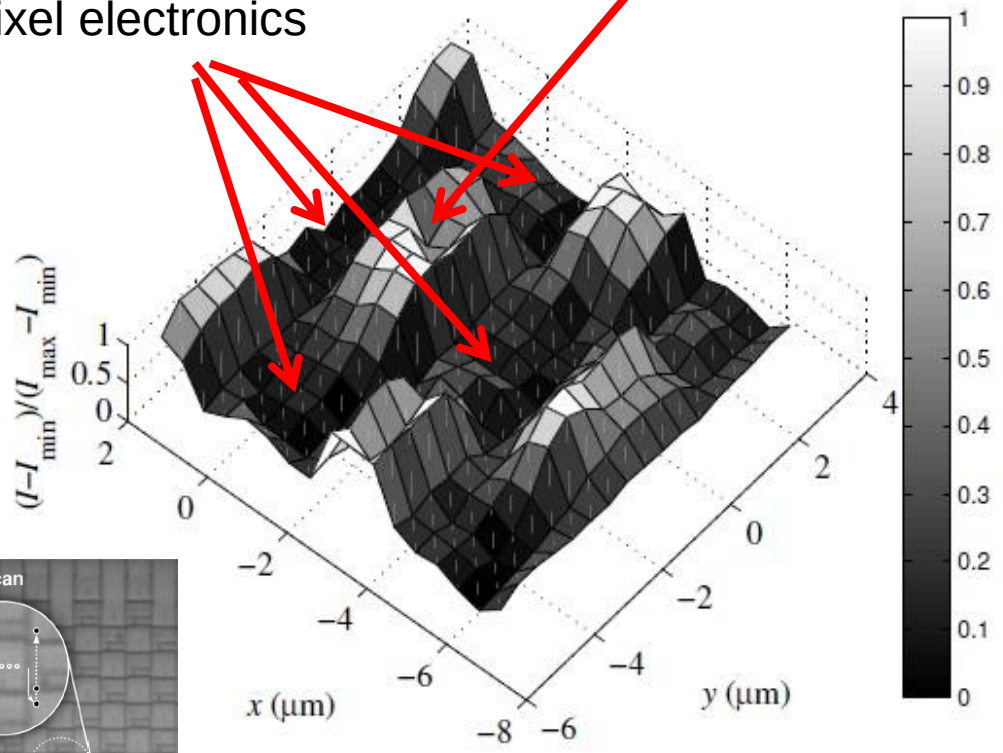
- Photodiode Modeling and Characterization

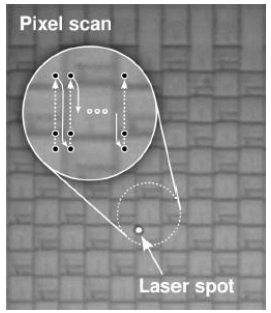
- **Goal –** Determination of the practical scaling limit of photodiodes in standard CMOS technologies
  - Modeling and experimental characterization under point source illumination → sub-pixel level study
  - Modeling and experimental characterization under uniform illumination

Point Source Illumination

North, south, east and west neighbors' pixel electronics

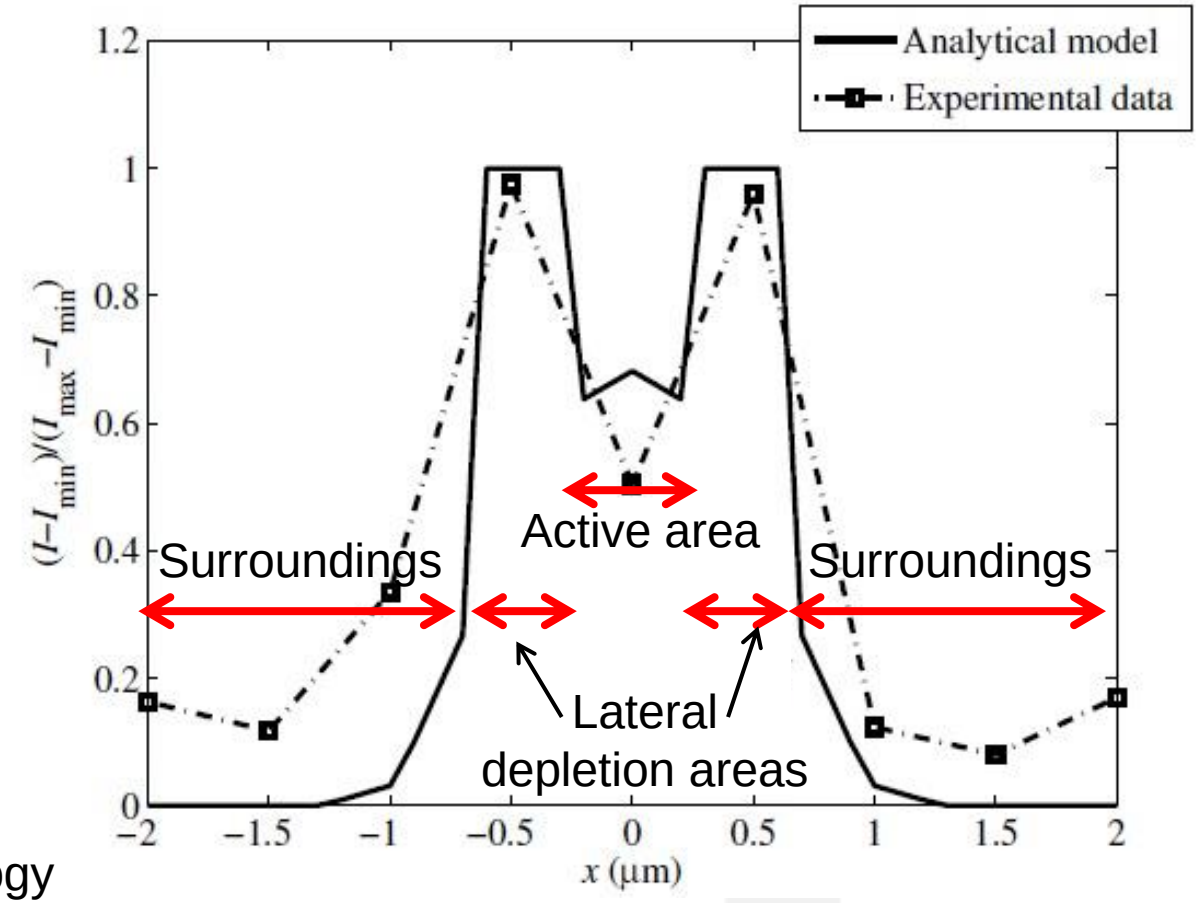
DUT





- Array of 4um x 8um 3T-APS pixels in chessboard configuration
- P-N+ and P-Nwell photodiodes
- UMC 90 nm standard CMOS technology

1D analytical model vs experimental results



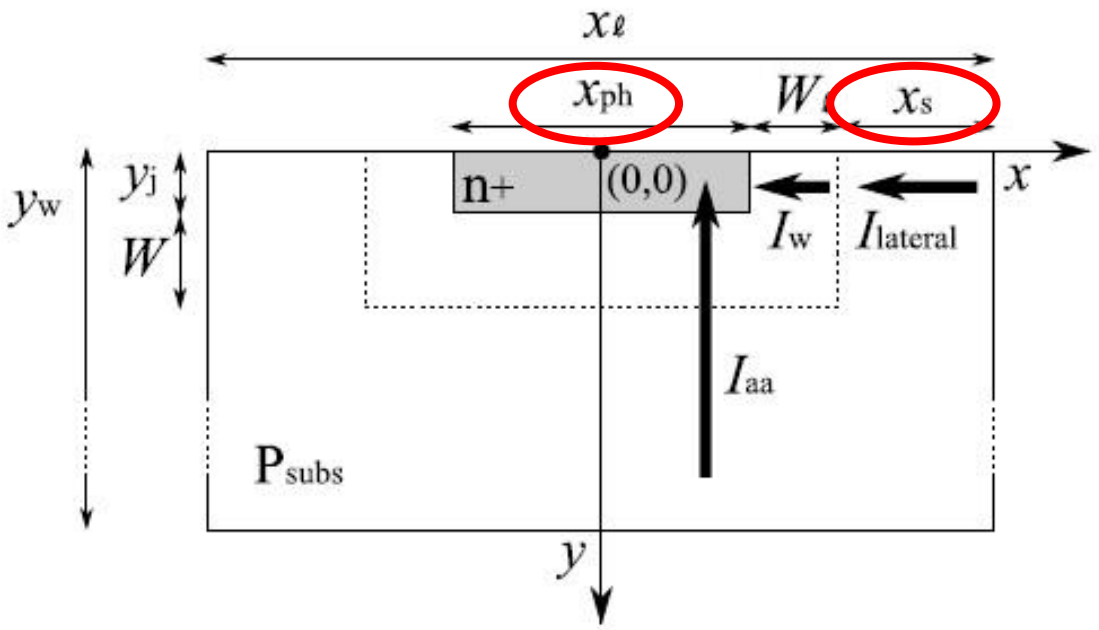
Uniform illumination

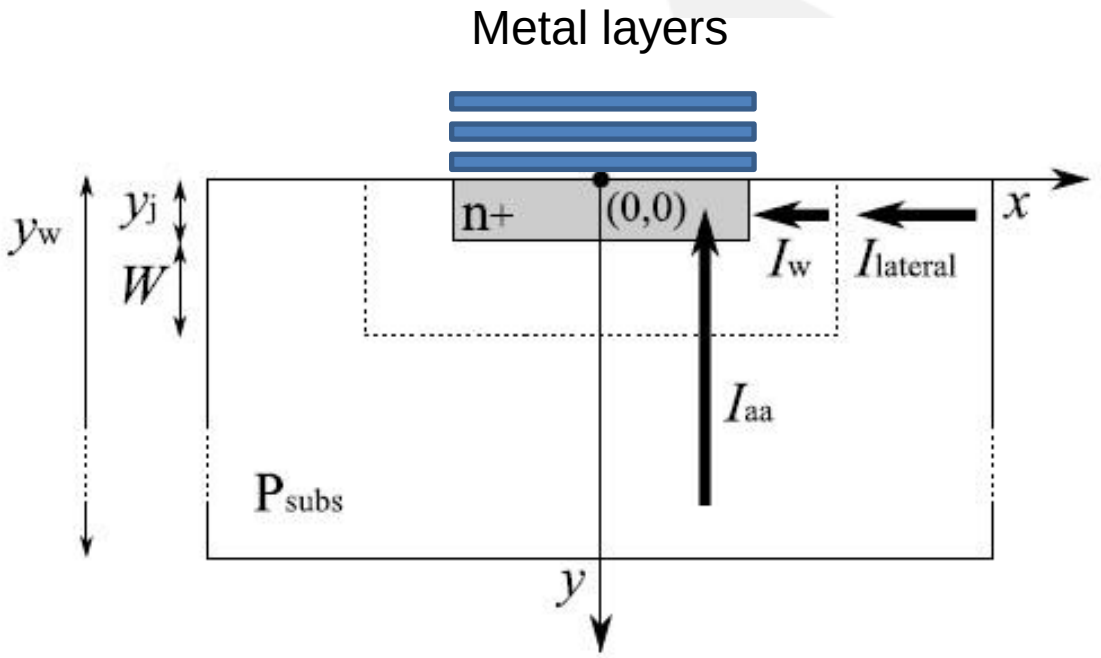
- **Goal –** Determination of the relative importance of the lateral collection with respect to the active area collection.
  - Development of a 2D, compact, general and scalable model for P-N+ [1,2] and P-Nwell [3] PDs
  - Experimental validation: square P-N+ junctions in AMS 180 nm and UMC 65 nm standard CMOS technologies [4]
  - Verilog-AMS implementation [5]

[1] Solid-State Electronics, vol. 73, pp. 15–20, Jul. 2012
[2] IEEE Transactions on electron devices, VOL. 60, NO. 10, pp. 3459-3464, 2013
[3] IEEE Transactions on electron devices, VOL. 62, NO. 2, pp. 580-586, 2015
[4] Semicond. Sci. Technol., vol. 28, no. 4, pp. 045011–045017, 2013
[5] Microelectronics Journal 43 (2012) 980–984

Uniform illumination

- Fabricated structures:





Uniform illumination

Experimental results

x_{ph} (μm)	x_s (μm)					
	0.355	0.605	0.855	1.105	1.355	1.605
0.56	68	95	102	100	89	52
1.06	172	235	244	247	228	137
1.56	304	419	435	437	405	-
2.06	468	635	663	664	605	-
2.56	505	662	664	683	635	-
3.06	769	736	-	-	-	-

Total photocurrent (nA) in UMC 65 nm standard technology.

x_{ph} (μm)	x_s (μm)					
	0.355	0.605	0.855	1.105	1.355	1.605
0.56	64	88	89	87	81	48
1.06	156	221	224	220	179	115
1.56	275	387	390	391	354	-
2.06	413	570	578	560	515	-
2.56	411	555	534	537	465	-
3.06	595	577	-	-	-	-

Lateral photocurrent (nA) in UMC 65 nm standard technology.

Lateral component dominates the total photocurrent!!

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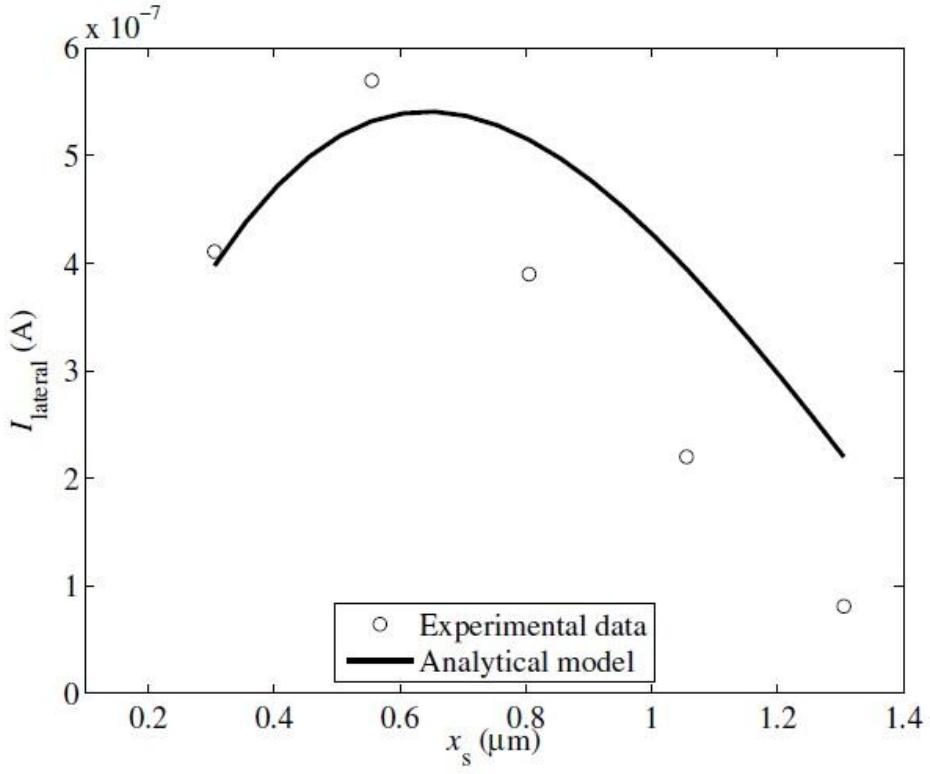
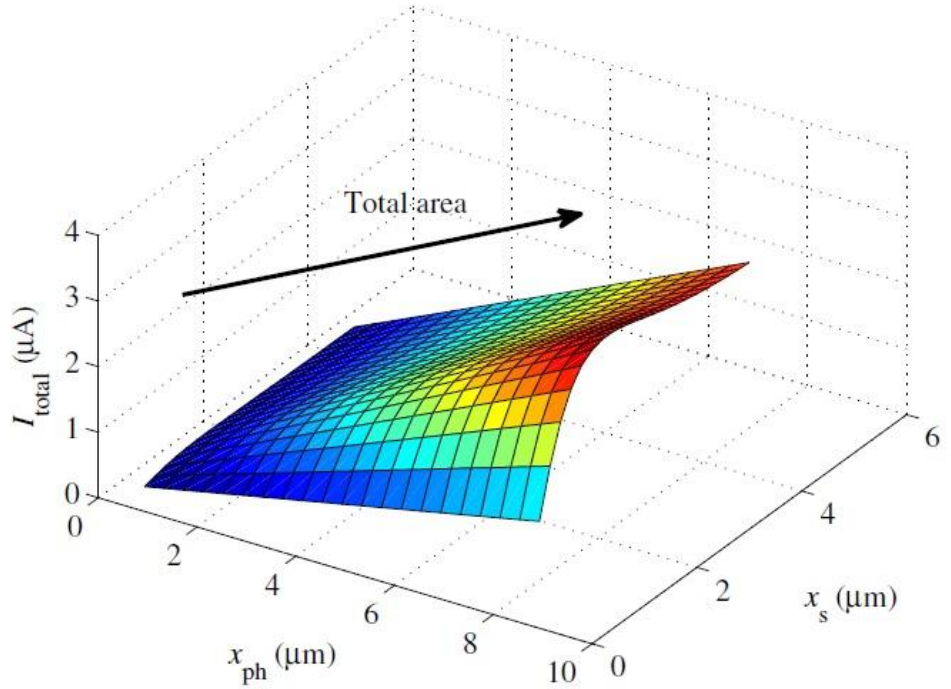
Uniform illumination

- 2D model:

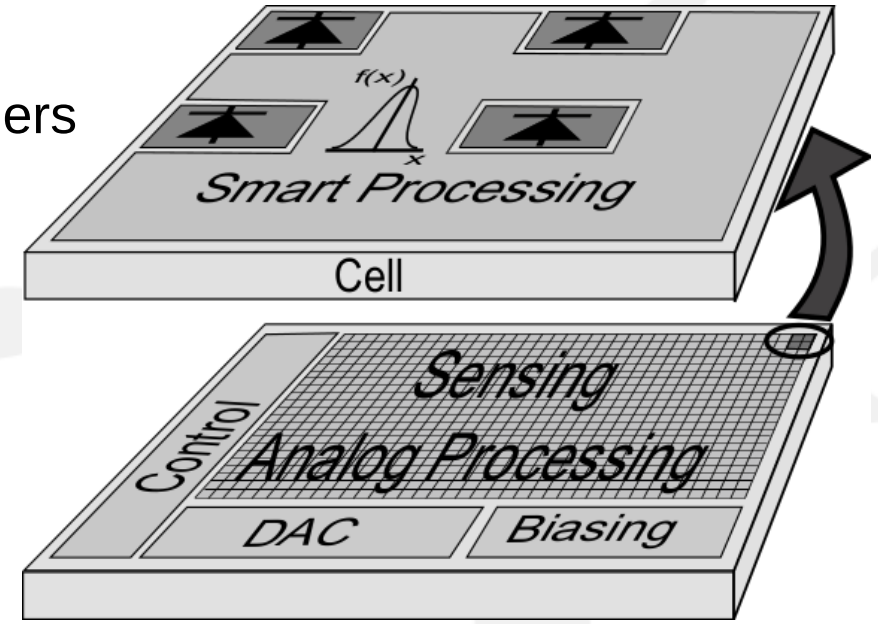




CMOS Vision Sensor for Gaussian Pyramid

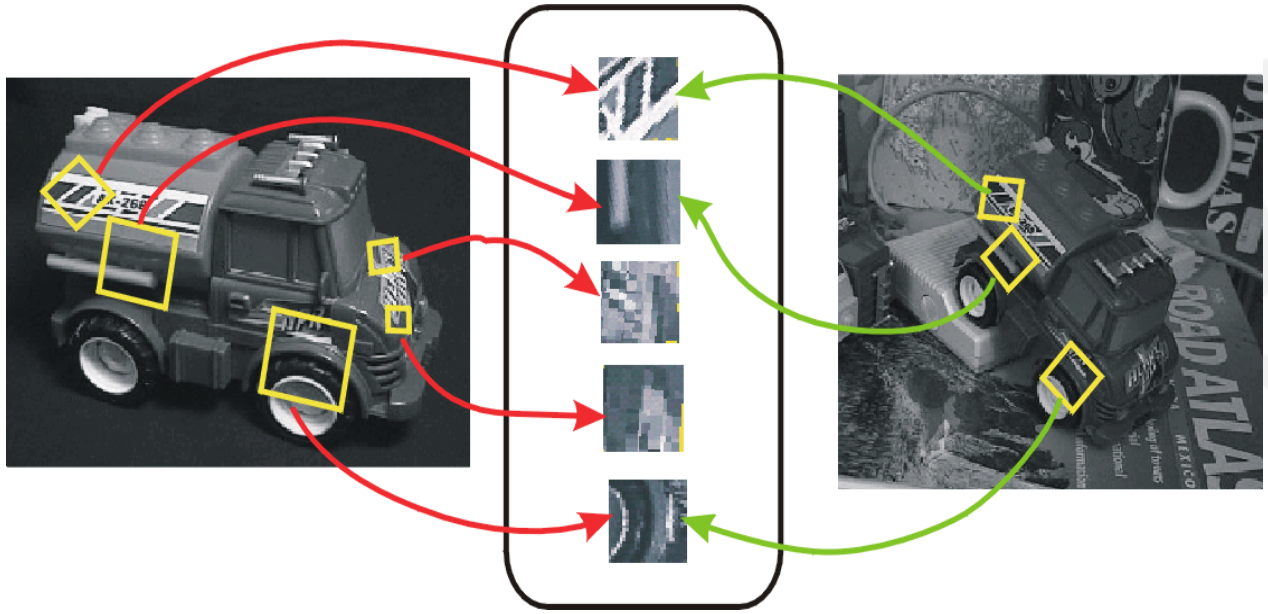
Feature Detectors on CMOS Vision Sensors

- CMOS vision sensor (CVIS) chips
- Embedded parallel processing close to the sensors
  - Per-column or per-pixel processors (or both of them combined)
    - Advantages
      - Fast and power efficient image analysis
    - Drawbacks
      - Larger pixel pitch with smaller fill-factor than imagers
      - Low resolution



CMOS Vision Sensors: Gaussian pyramid

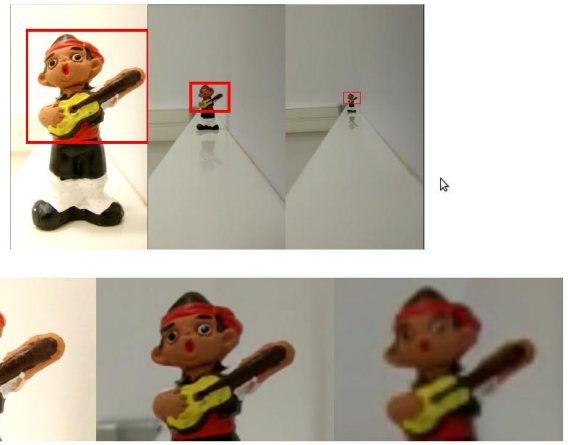
- **Goal-** design of a CMOS Vision Sensor (CVIS) chip for Gaussian pyramid extraction[1]
- **Gaussian Pyramid Extraction**- first stage of many feature detectors; it provides algorithms with scale invariance
- **Applications-** tracking, object detection, image registration, etc.



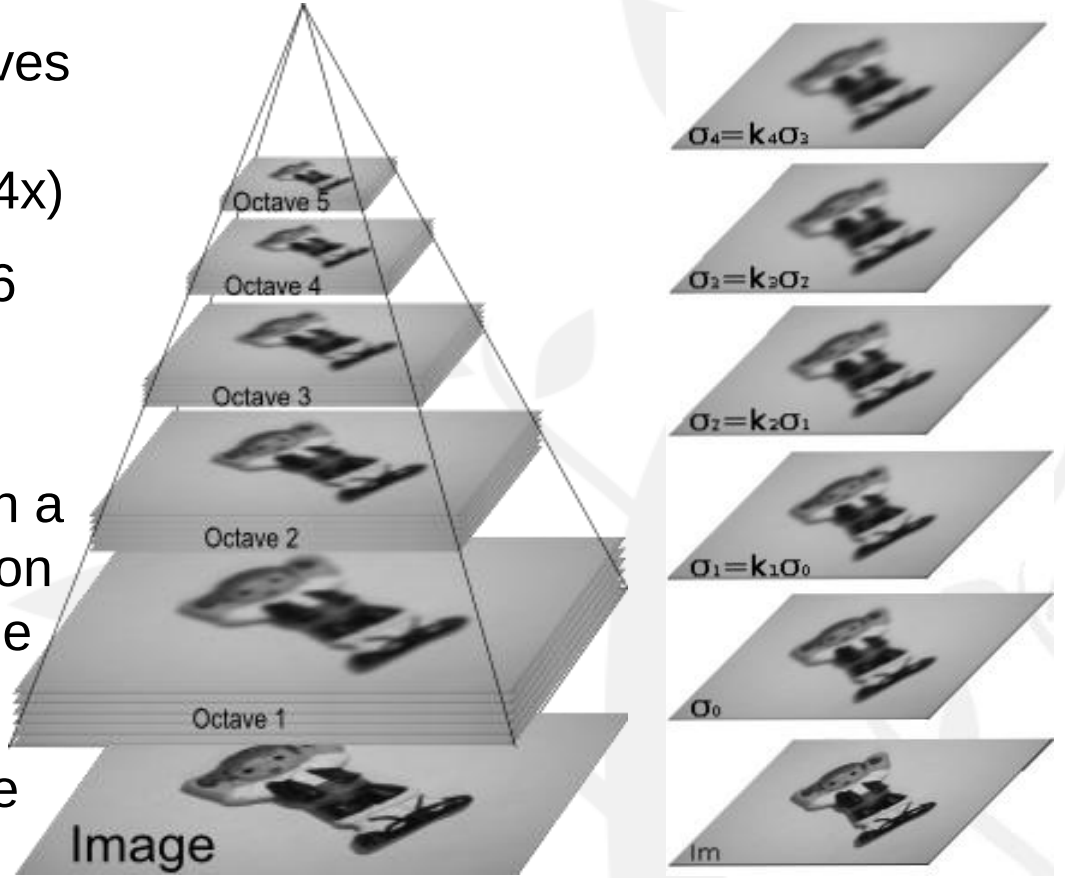
[1] IEEE J. of Solid-State Circuits, vol. 52, no. 2, pp. 483-495, 2017

CMOS Vision Sensor for Gaussian Pyramid

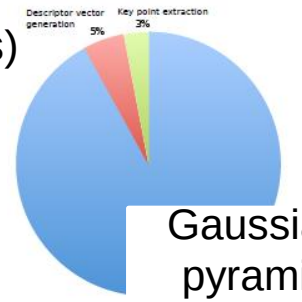
- Gaussian pyramid emulates the lost of high spatial frequency components as an object moves away from the camera



- Organized in octaves (downscaling the previous one in 1/4x)
- Each octave with 6 images or scales
- A scale is a Gaussian filter with a given sigma level on the incoming image
- 3 octaves with 6 scales each suffice



Breakdown of SIFT algorithm (@ HD, @30 fps, @ #3375 keypoints)



Gaussian pyramid 92%

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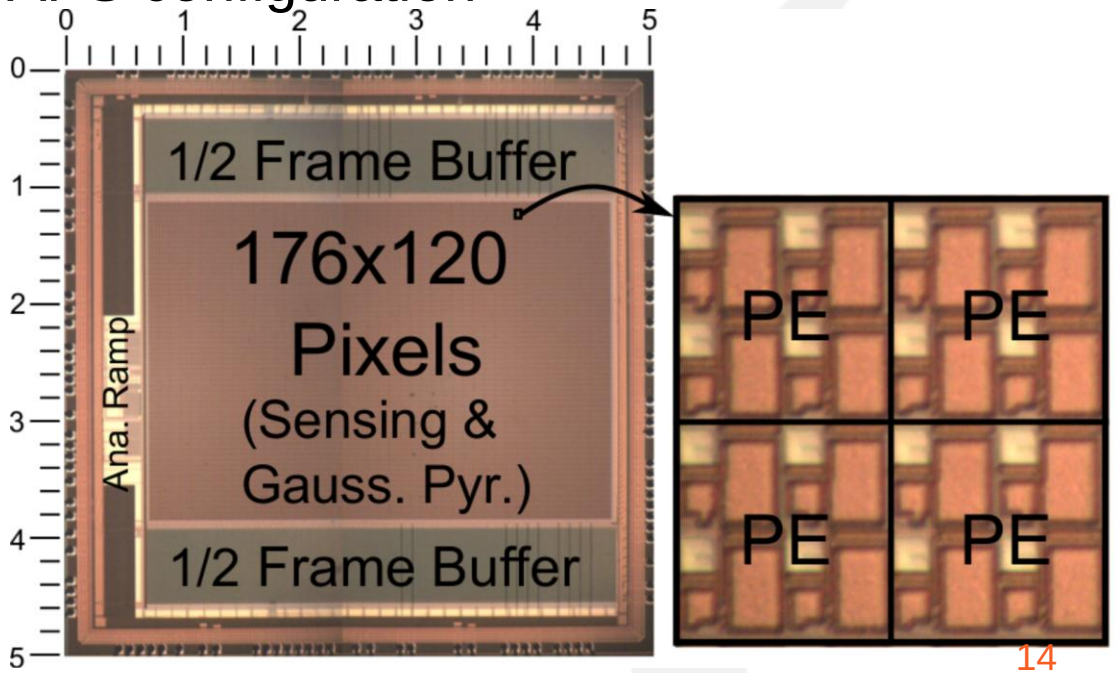
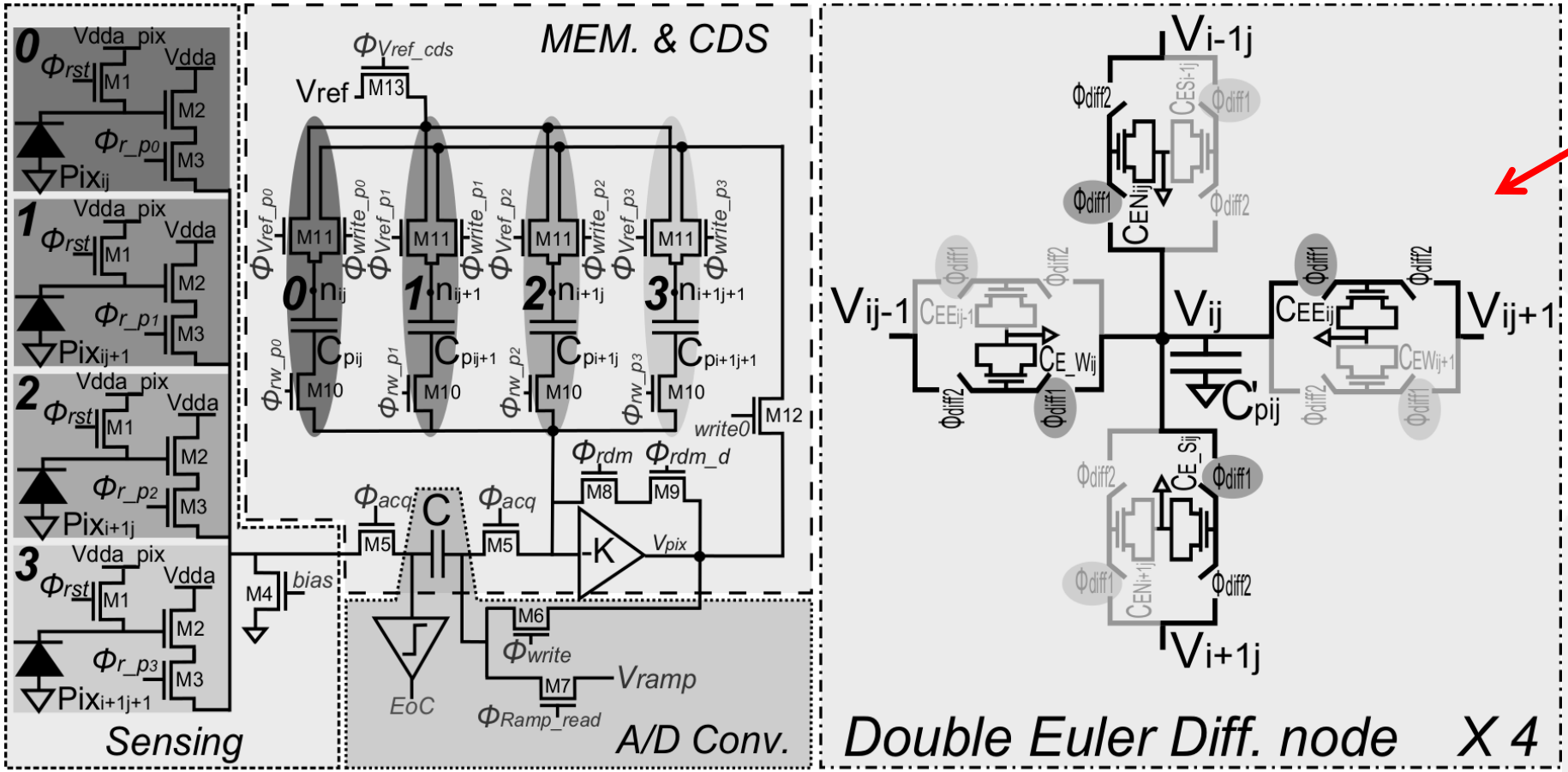
CMOS Vision Sensor for Gaussian Pyramid- chip features

- 176 x 120 pixels (5 x 5 mm^2) in standard 180 nm CMOS technology
- 88 x 60 Processing Elements (PE) for close to the sensor and concurrent processing
- Every PE occupies 44 x 44 μm^2, comprising:
  - 4 nwell/psub photodiodes of 8 x 8 μm^2 in 3T-APS configuration
  - 4 state and 4 exchange capacitors
  - Circuits for in-PE ADC and CDS
    - Hardware reuse
- Read-out with an 8-bit single-slope ADC

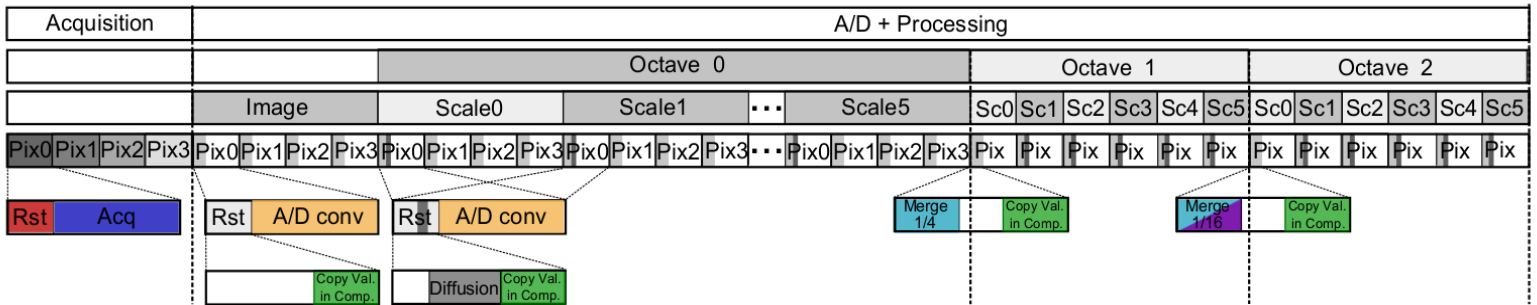


CMOS Vision Sensor for Gaussian Pyramid- chip features- pixel schematics



Switched-Capacitor Network

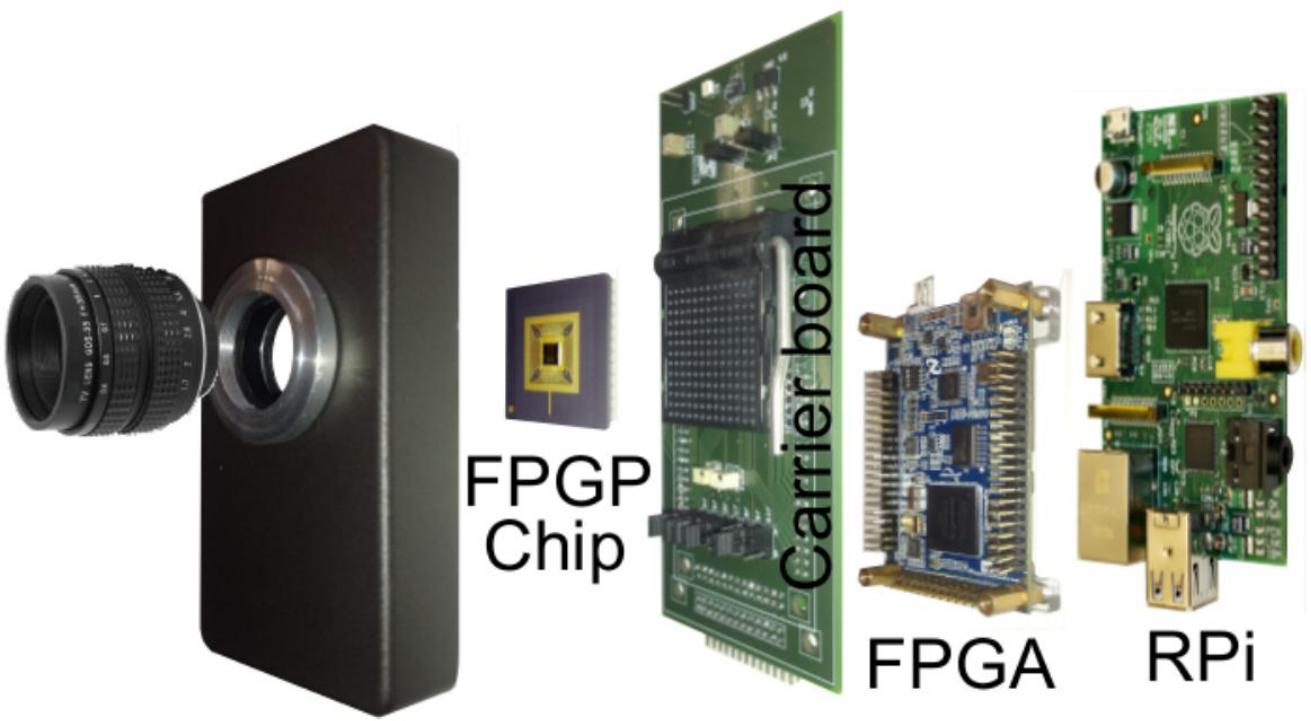
- More linear than resistor-based solutions
- Better control of σ through the number of clock cycles



CMOS Vision Sensor for Gaussian Pyramid

Experimental Results

- Test Setup



CMOS Vision Sensor for Gaussian Pyramid

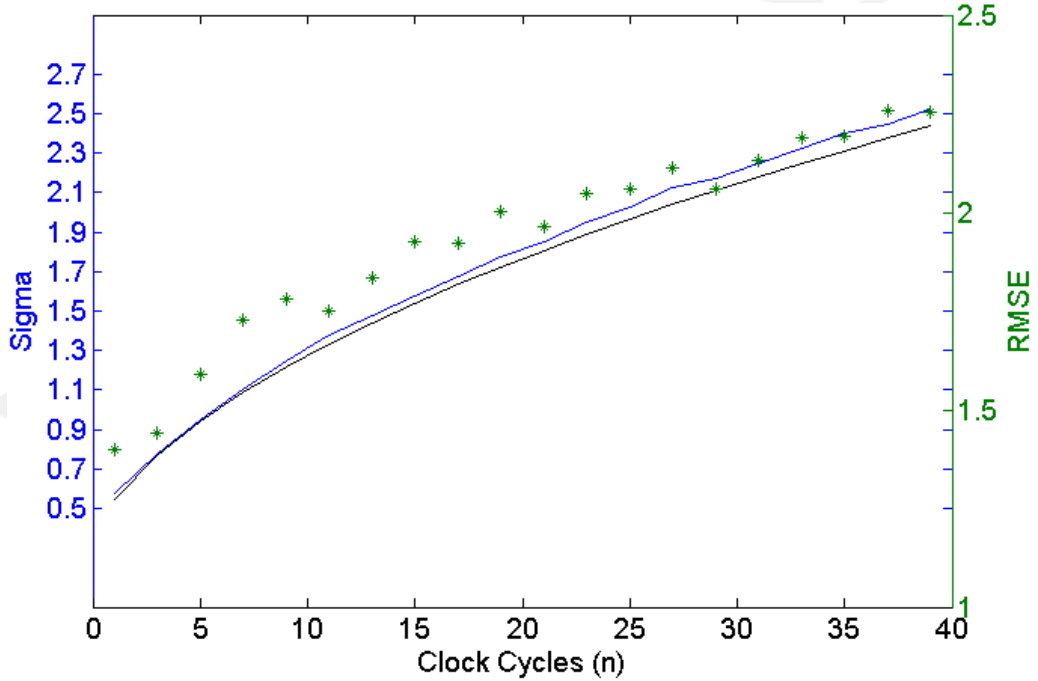
Experimental Results

- Input image and different snapshots of the on-chip Gaussian pyramid for $\sigma = 1.77$ (number of clock cycles of the double-Euler, n= 19), $\sigma = 2.17$ (n = 29), and $\sigma = 2.51$ (n = 39)

- Accuracy assessment:

  Sigma : Theoretical (black); Experimental (blue)

  RMSE- comparison with the Gaussian filter with numerical simulations (Matlab).



CMOS Vision Sensor for Gaussian Pyramid

Experimental Results: comparison with conventional solutions

HW Solution	Function	Energy/frame	Energy/px	Mpx/s
This work 180 nm CMOS	Gaussian Pyramid	176 x 120 px 70 mW @ 8 ms 0.56 mJ/frame	26.5 nJ/px	2.64
Ref. [1] OV9655 + Core-i7	Gaussian Pyramid	VGA resolution 90 mW @ 30 fps + 35 W @ 136 ms 4.8 J/frame	15.5 uJ/px	2.26
Ref. [2] OV9655 + Core-2-Duo	Gaussian Pyramid	VGA resolution 90 mW @ 30 fps + 35 W @ 2.1 s 73.7 J/frame	240 uJ/px	0.15
Ref. [3] OV9622 + Qualcomm Snapdragon S4	Gaussian Pyramid	350 x 256 px 30 mW + 4 W @ 98.5 ms 0.4 J/frame	4.4 uJ/px	0.91

[1] M. Murphy et al., “Image Feature Extraction for Mobile Processors”, IEEE IIWSC 2009

[2] Feng-Cheng Huang et al., “High-Performance SIFT Hardware Accelerator for Real-Time Image Feature Extraction”, IEEE TCAS-VT, vol. 22, no. 2, March 2012

[3] G. Wang et al., “Workload Analysis and Efficient OpenCL-based Implementation of SIFT Algorithm on a Smartphone”, IEEE GlobalSIP 2013

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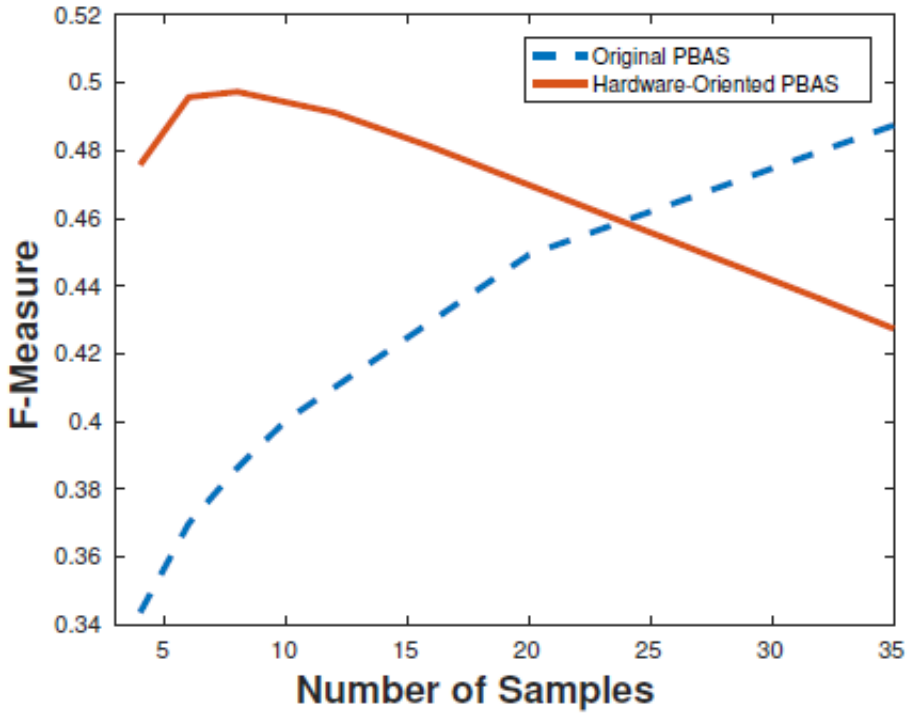
- CMOS Vision Sensor for Background Subtraction

CMOS Vision Sensor for Background Subtraction

- Hardware-Oriented Pixel Based Adaptive Segmenter (HO-PBAS)- D. García-Lesta et al., “In-Pixel Analog Memories for a Pixel-Based Background Subtraction Algorithm on CMOS Vision Sensors”, Int. J. of Circuit Theory and Applications, 2018



	N=8		N=35	
	PBAS	HO-PBAS	PBAS	HO-PBAS
shadow	0.6864	**0.7367**	**0.8058**	0.6249
badWeather	0.5492	**0.6987**	**0.7226**	0.5870
PTZ	0.0447	**0.1220**	0.0718	**0.1056**
dynamicBackground	0.1555	**0.4994**	0.3839	**0.5342**
cameraJitter	0.2387	**0.5585**	**0.4285**	0.2820
thermal	**0.6791**	0.3694	**0.6703**	0.2472
intermittentObjectMotion	**0.4107**	0.2793	0.4187	**0.6903**
turbulence	0.0625	**0.6718**	0.2112	**0.6281**
baseline	**0.7512**	0.7052	**0.7674**	0.6281
lowFramerate	0.3725	**0.5078**	**0.4941**	0.4071
nightVideos	0.2482	**0.4009**	**0.3417**	0.2331
Overall	0.3863	**0.4981**	**0.4874**	0.4275

Table: F-Measure for PBAS and HO-PBAS with N=8 and N=35 (best results in bold).

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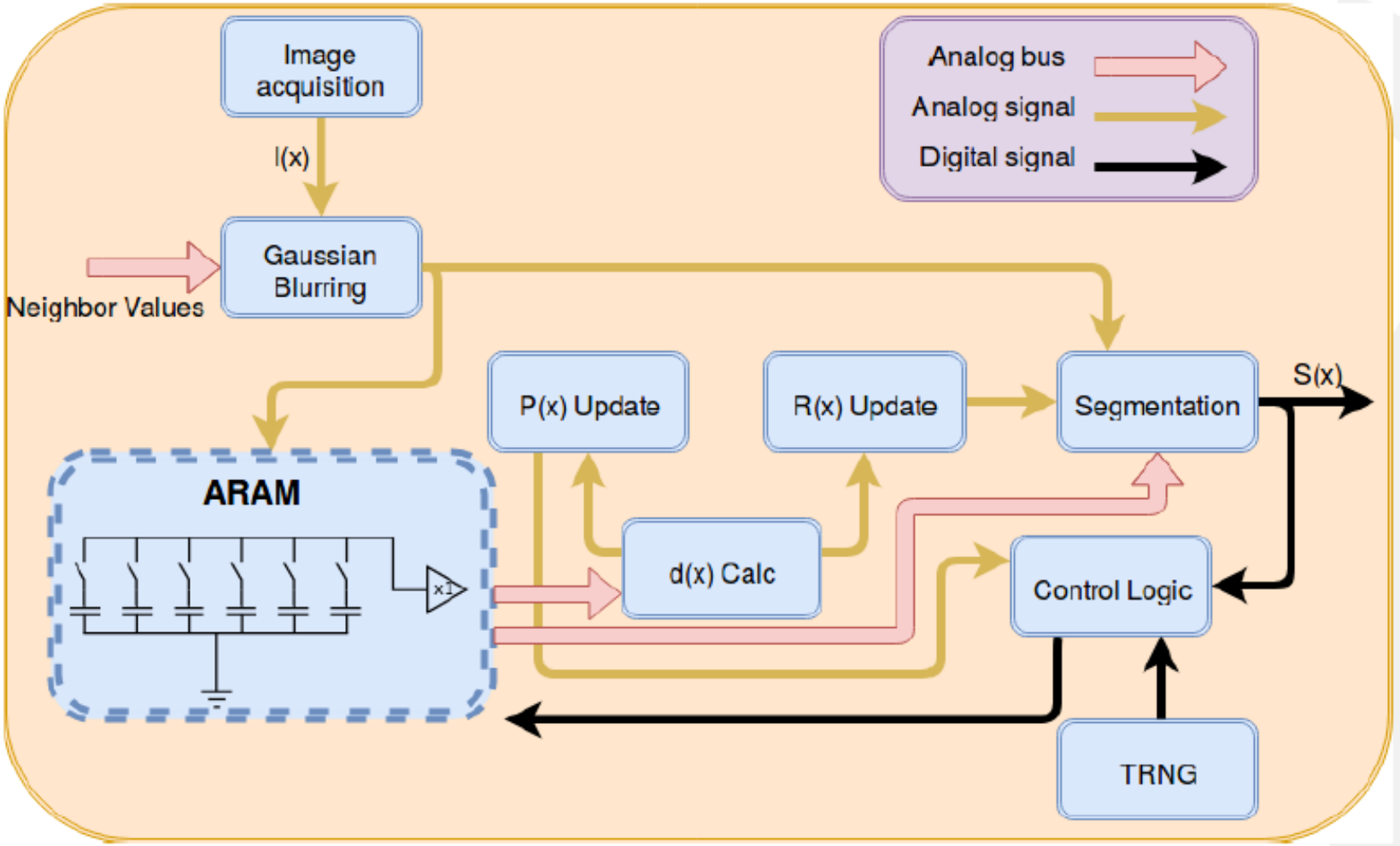
CMOS Vision Sensor for Background Subtraction

- Pixel Architecture



[1] D. Lesta et al., International Journal of Circuit Theory and Applications, pp. 1631-1647 , 2018.

CMOS Vision Sensor for Background Subtraction

- Scalable analog core
- Column parallel single-slope 8-bits ADC
- Ncol x 8 bits row buffer that holds a row conversion while the next one is being converted
- Global control

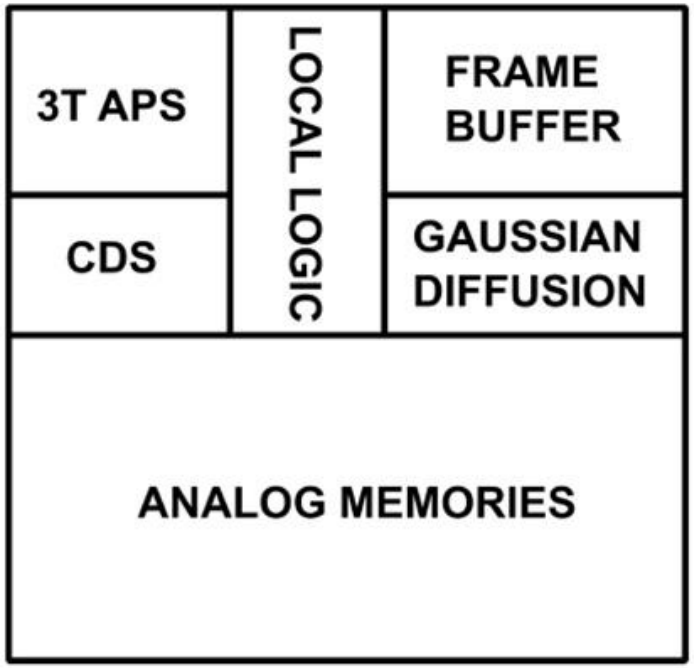
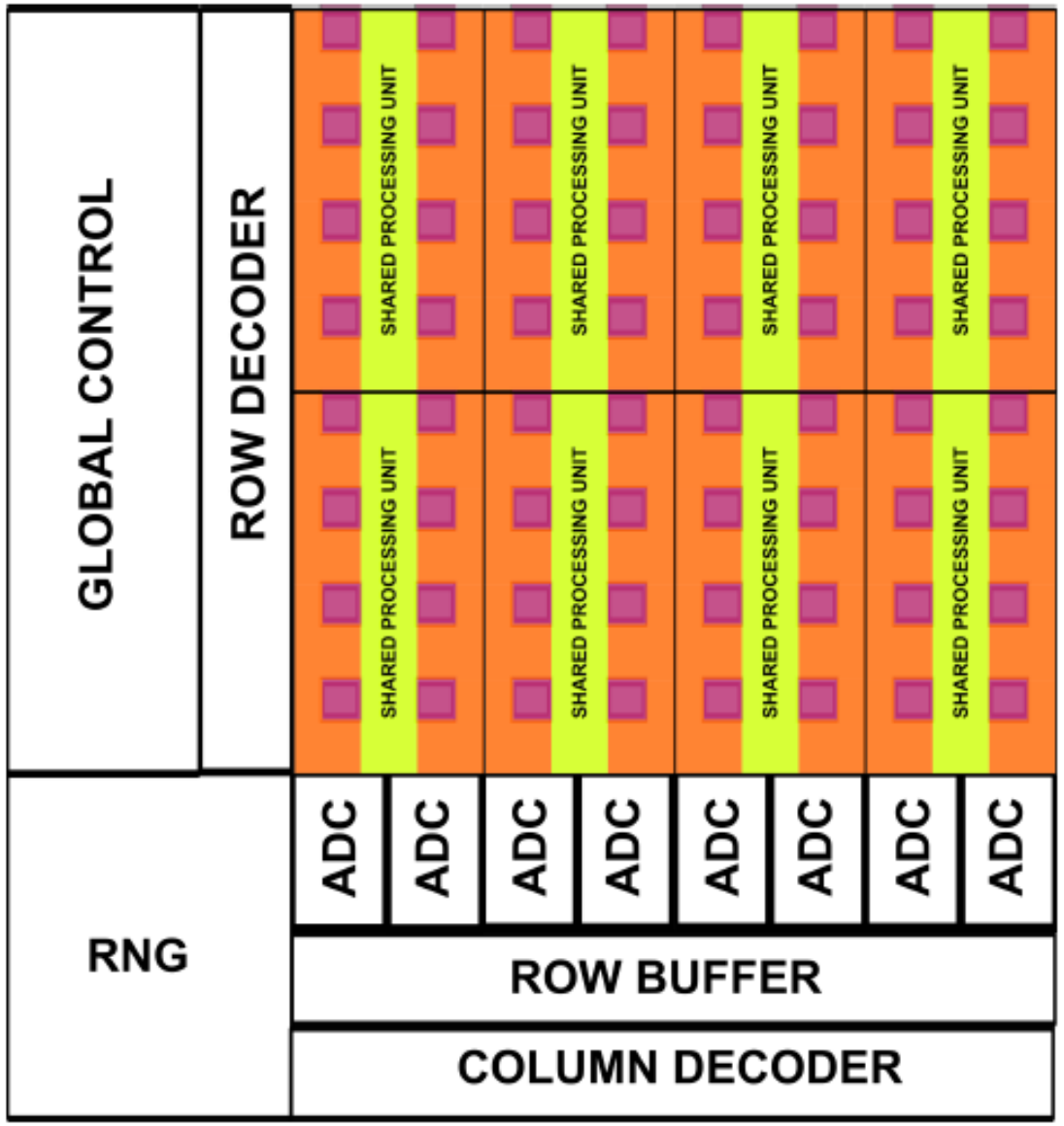


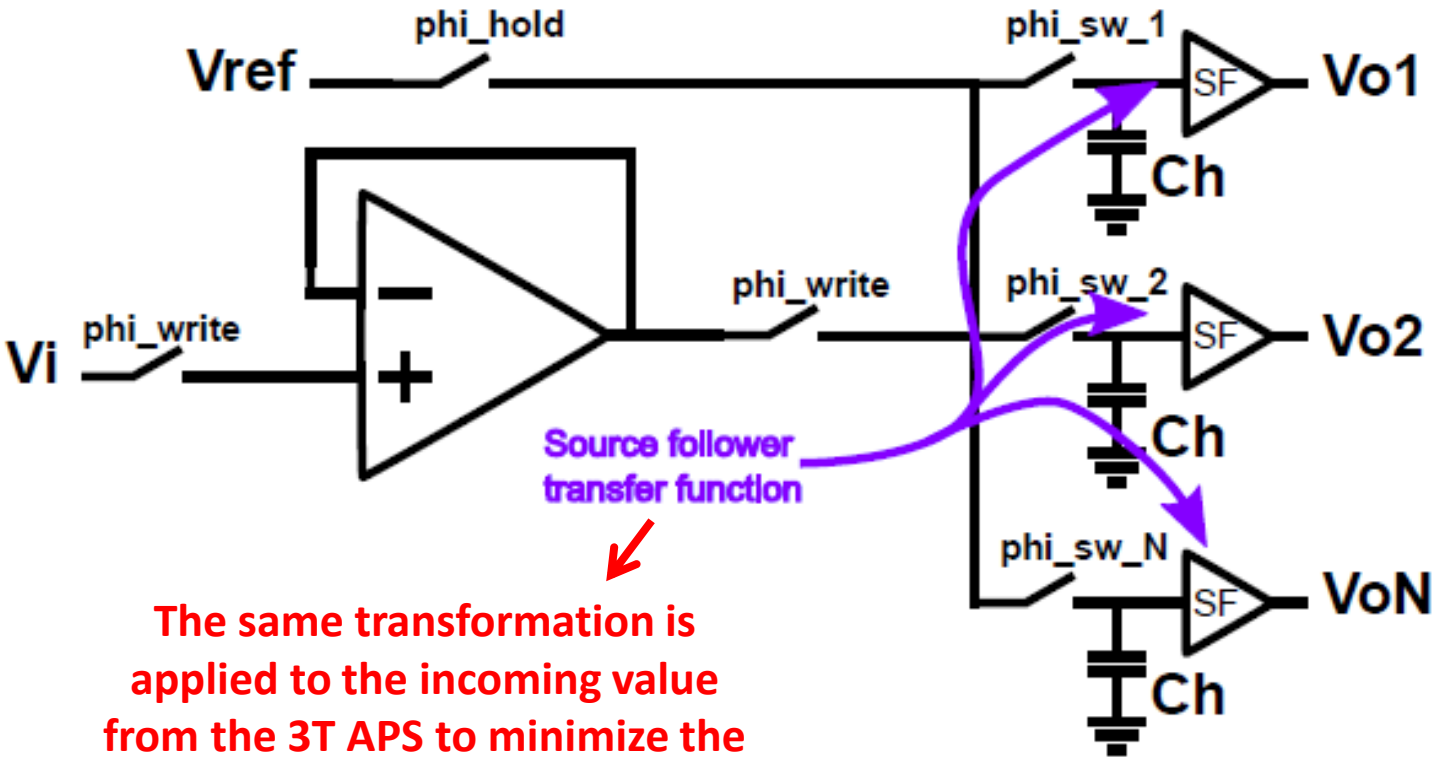
Figure: Pixel floorplan



CMOS Vision Sensor for Background Subtraction

ARAM

- Analog memories
  - Open-loop architecture with SF as output buffers [1]
  - MIM capacitors
  - Non-destructive readings
  - Write error- 3 mV
  - Voltage drift- < 1mV/s

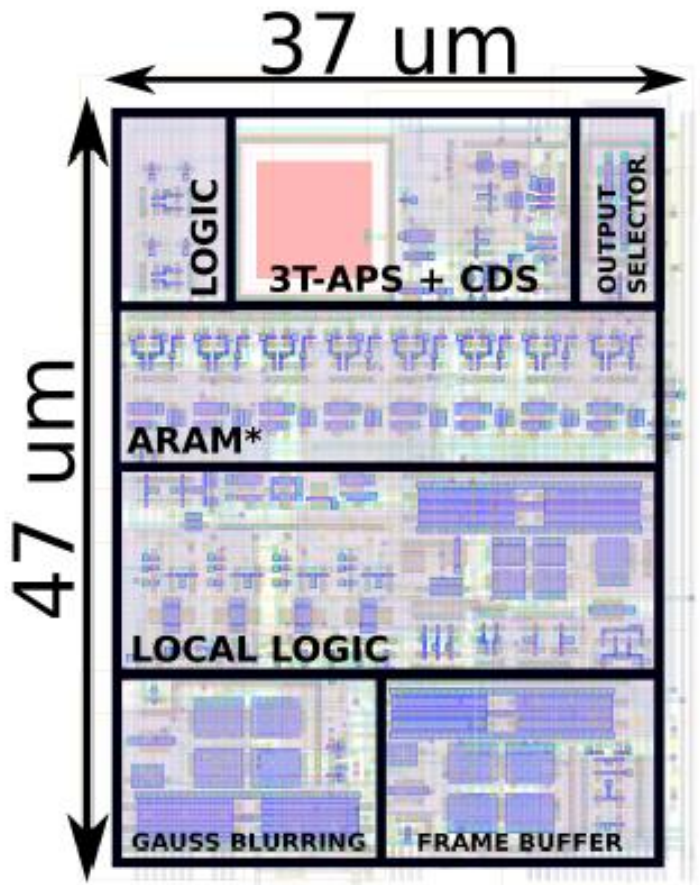


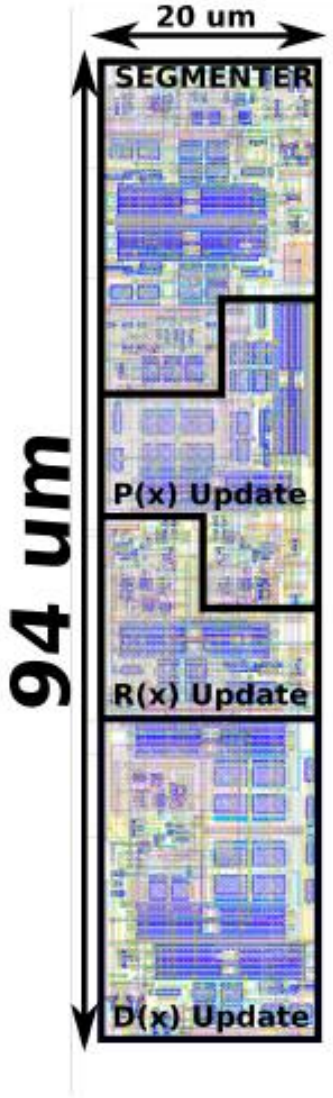
The same transformation is applied to the incoming value from the 3T APS to minimize the impact

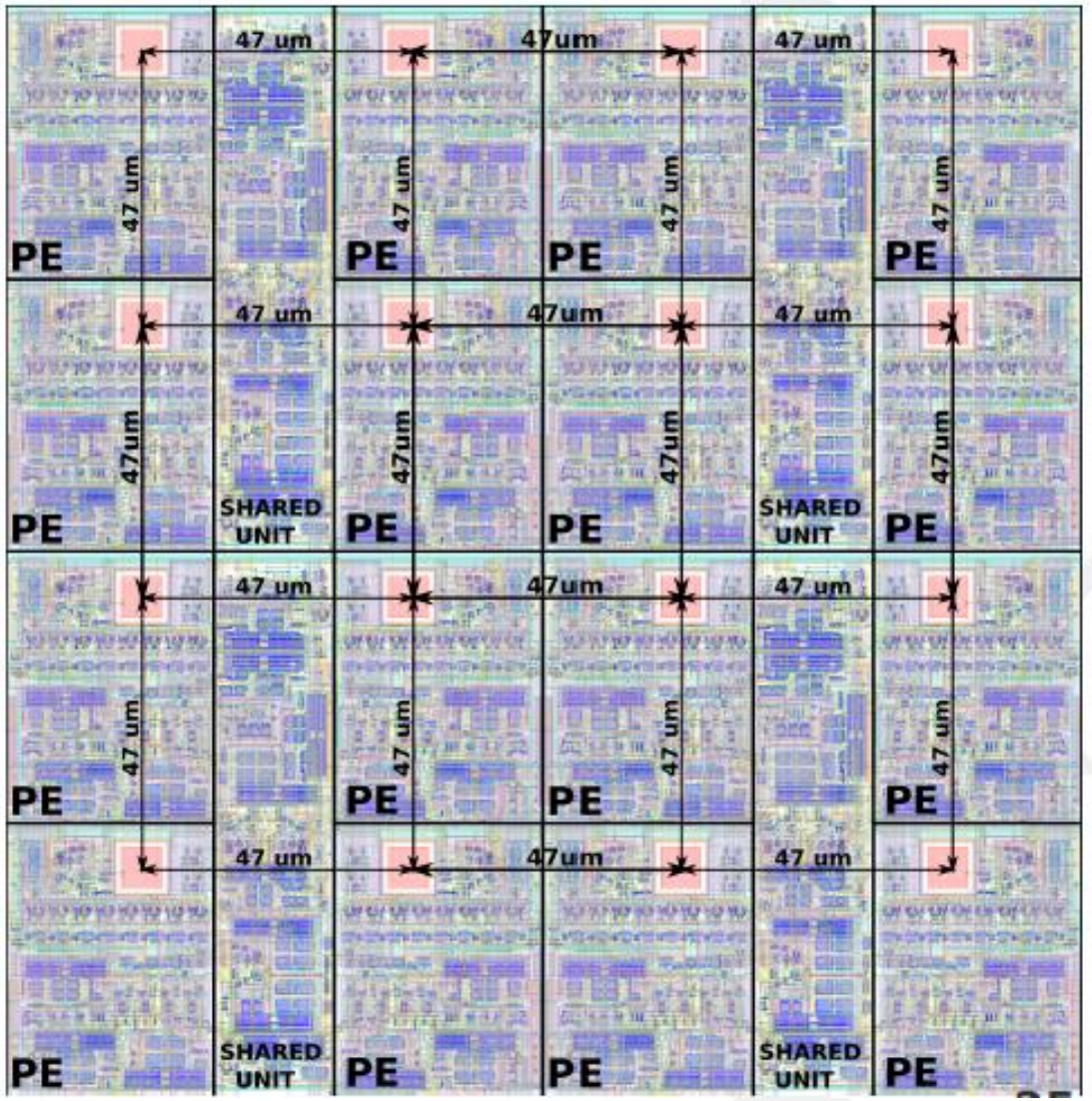
[1] D. Lesta et al., International Journal of Circuit Theory and Applications, pp. 1631-1647 , 2018.

CMOS Vision Sensor for Background Subtraction

Layouts







CMOS Vision Sensor for Background Subtraction

Layouts

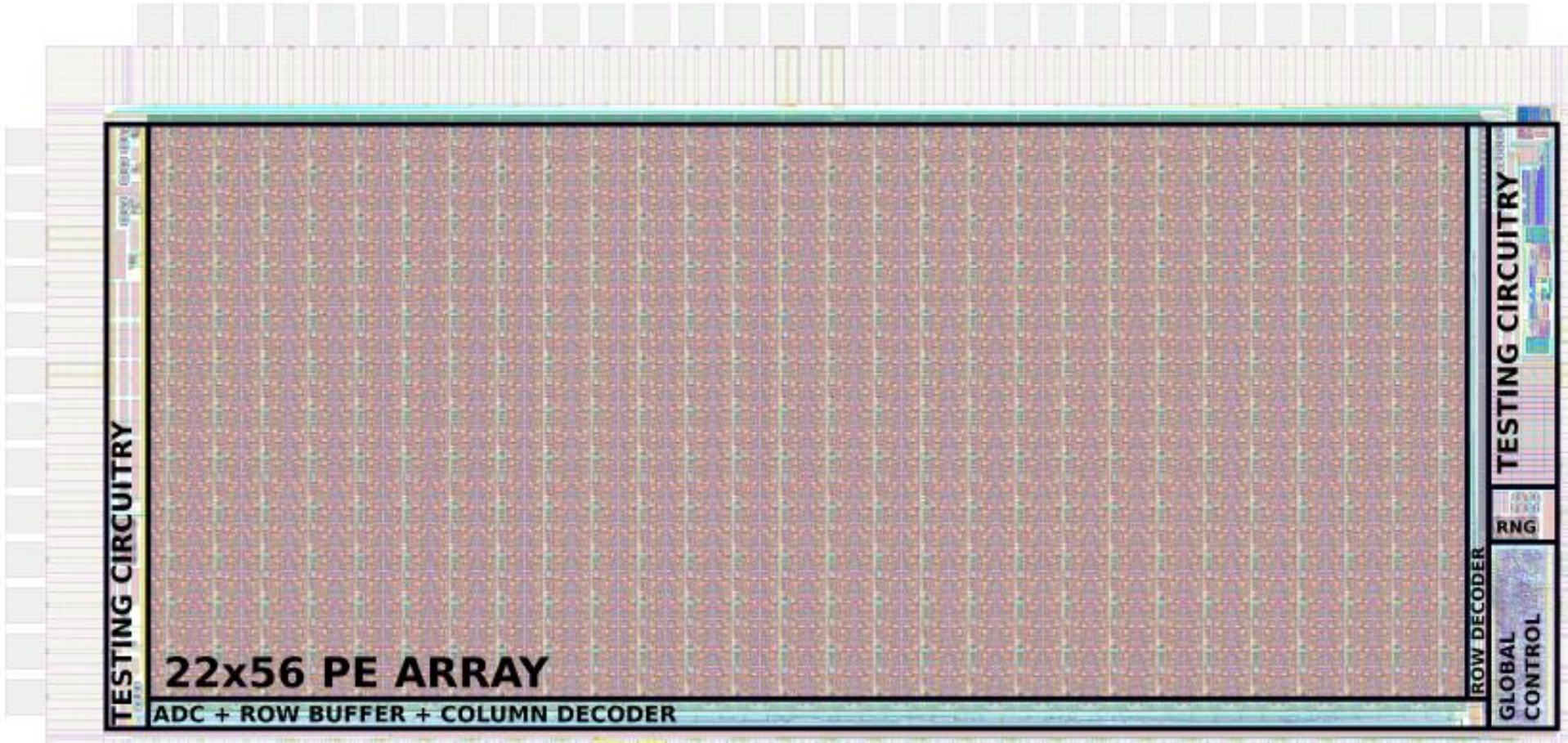


Figure: Proof of concept 22x56 pixel CMOS vision sensor for background subtraction.

- On-chip Micro Energy Harvesting

Micro-Energy Harvesting Chip Features

Chip - Energy Harvesting	Features
Energy transducer and PMU	Both of them on-chip
Technology	Standard 0.18 um CMOS (UMC)
Area	Photodiode- 1 mm2, PMU- 0.575 mm2
Voltage boosting	Capacitive DC-DC converter- programable Dickson topology- gain, fly capacitors and frequency
Start-up	Cold- no external mechanisms
Energy span	2.38 nW- 10 uW
MPPT	Open-loop- different working regions (WR) according to the photodiode voltage; V_{PD}

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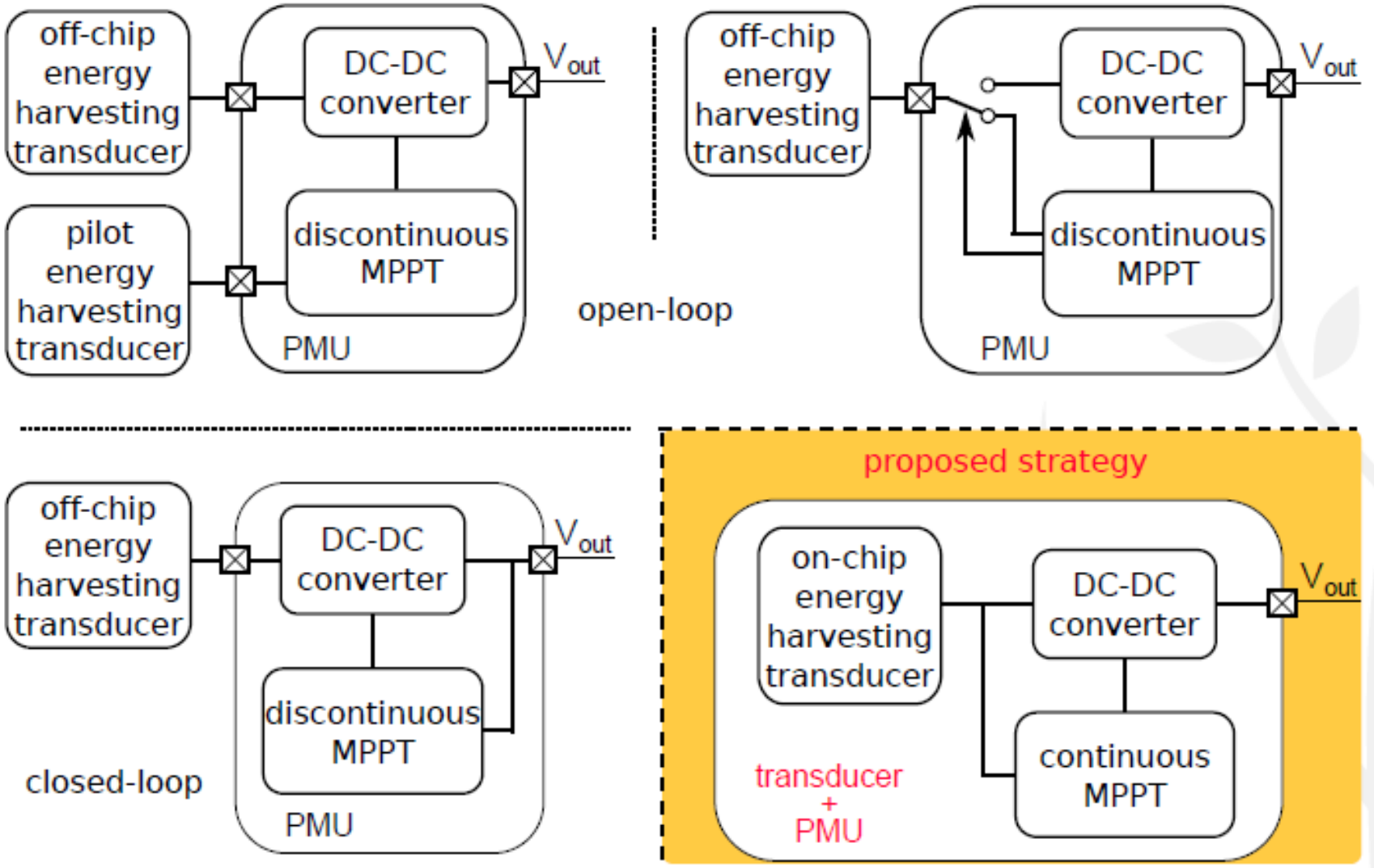
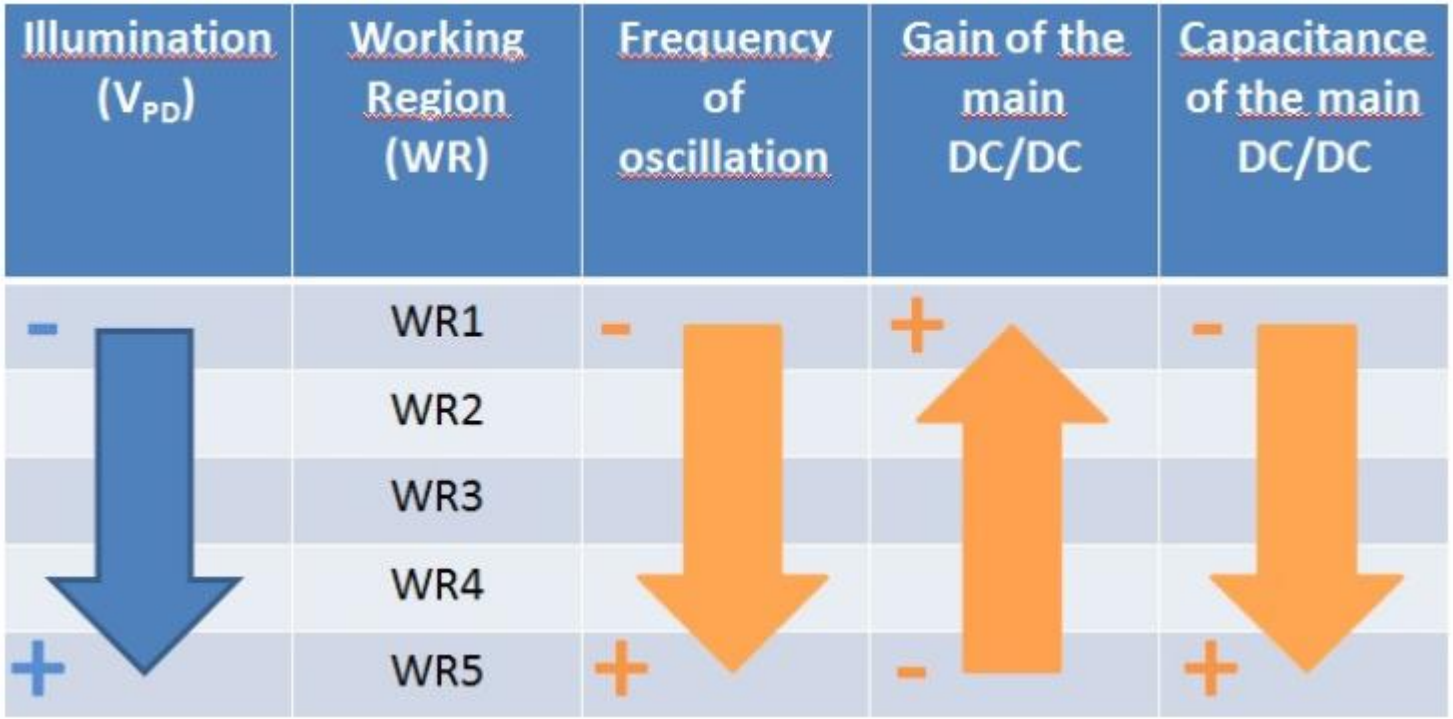
Micro-Energy Harvesting Chip Architecture



Micro-Energy Harvesting Chip Architecture

- **MPPT**
  - Open-loop
  - Continuous and bidimensional-changes in topology, fly capacitors and frequency of the main charge pump (Dickson)
  - 5 working regions (WR) according to illumination levels (VPD)
  - Maximum current for a given output voltage, in this case 1.1 V
  - Voltage levels of WR defined during the design phase with a joint model of photodiode and Dickson charge pump [1]



[1] E. Ferro, P. López, V.M. Brea, D. Cabello. "Dynamic joint model of capacitive charge pumps and on-chip photovoltaic cells for CMOS micro-energy harvesting". Int. J. of Circuit Theory and Applications, vol. 44, no. 10, pp. 1874-1894, 2016.

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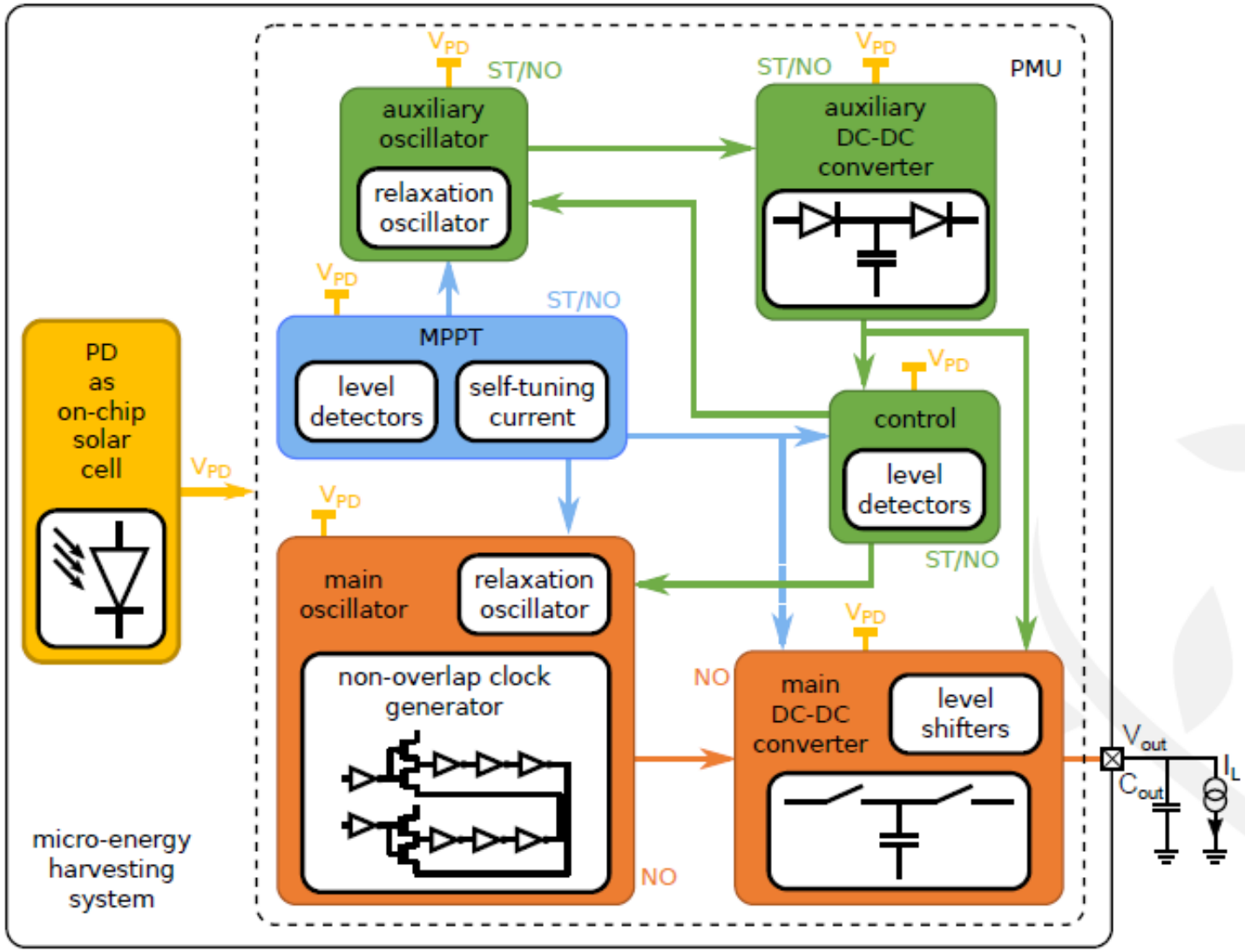
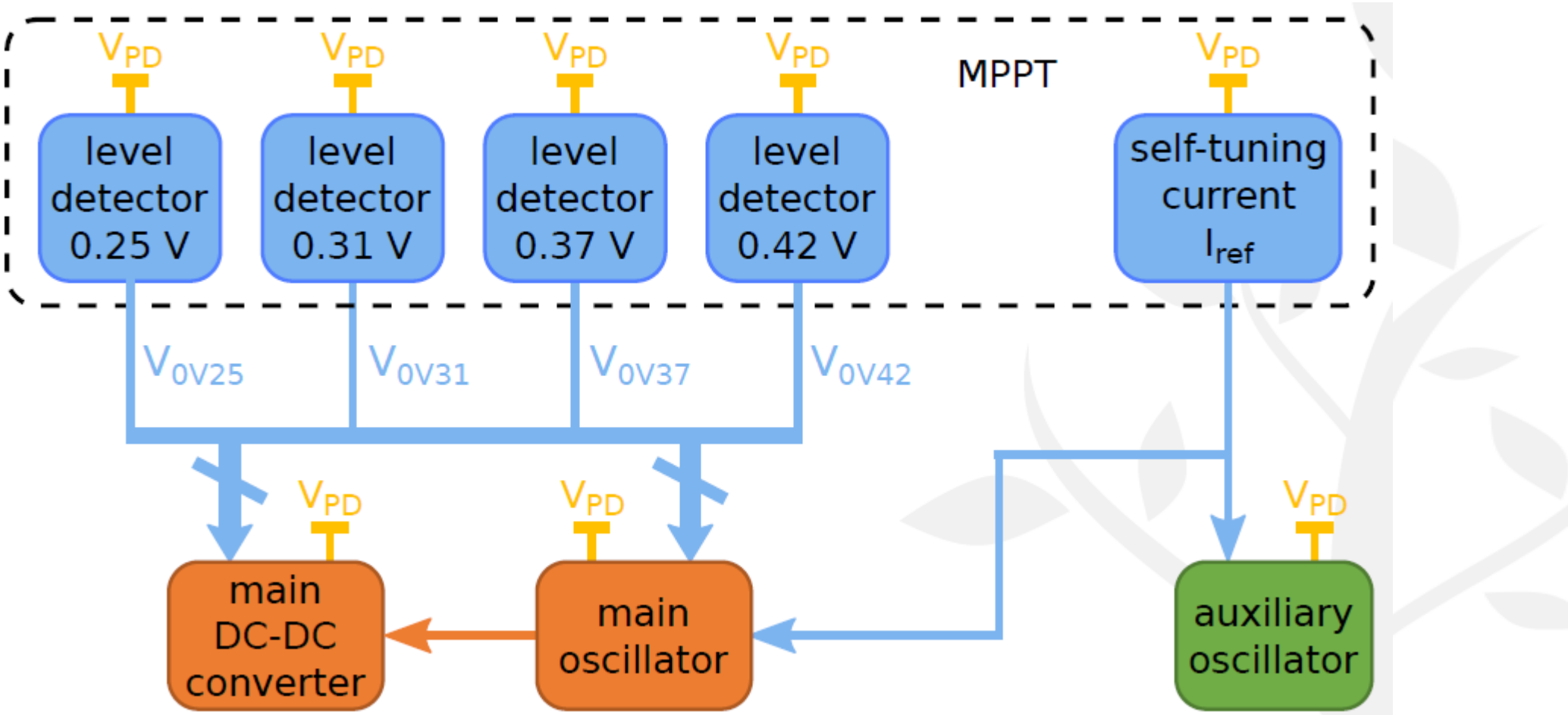
Micro-Energy Harvesting Chip Architecture

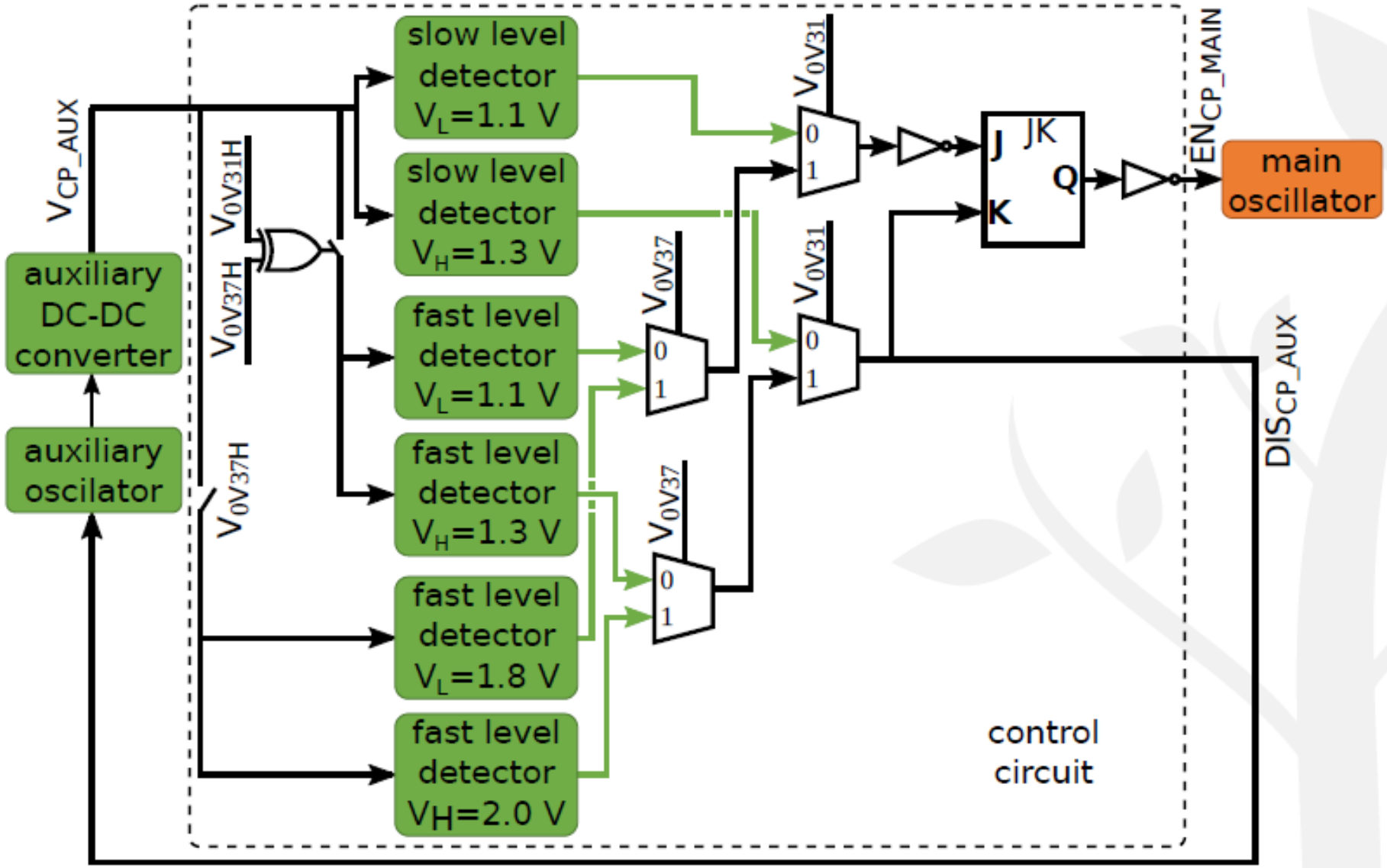


ST: start-up operation NO: normal operation

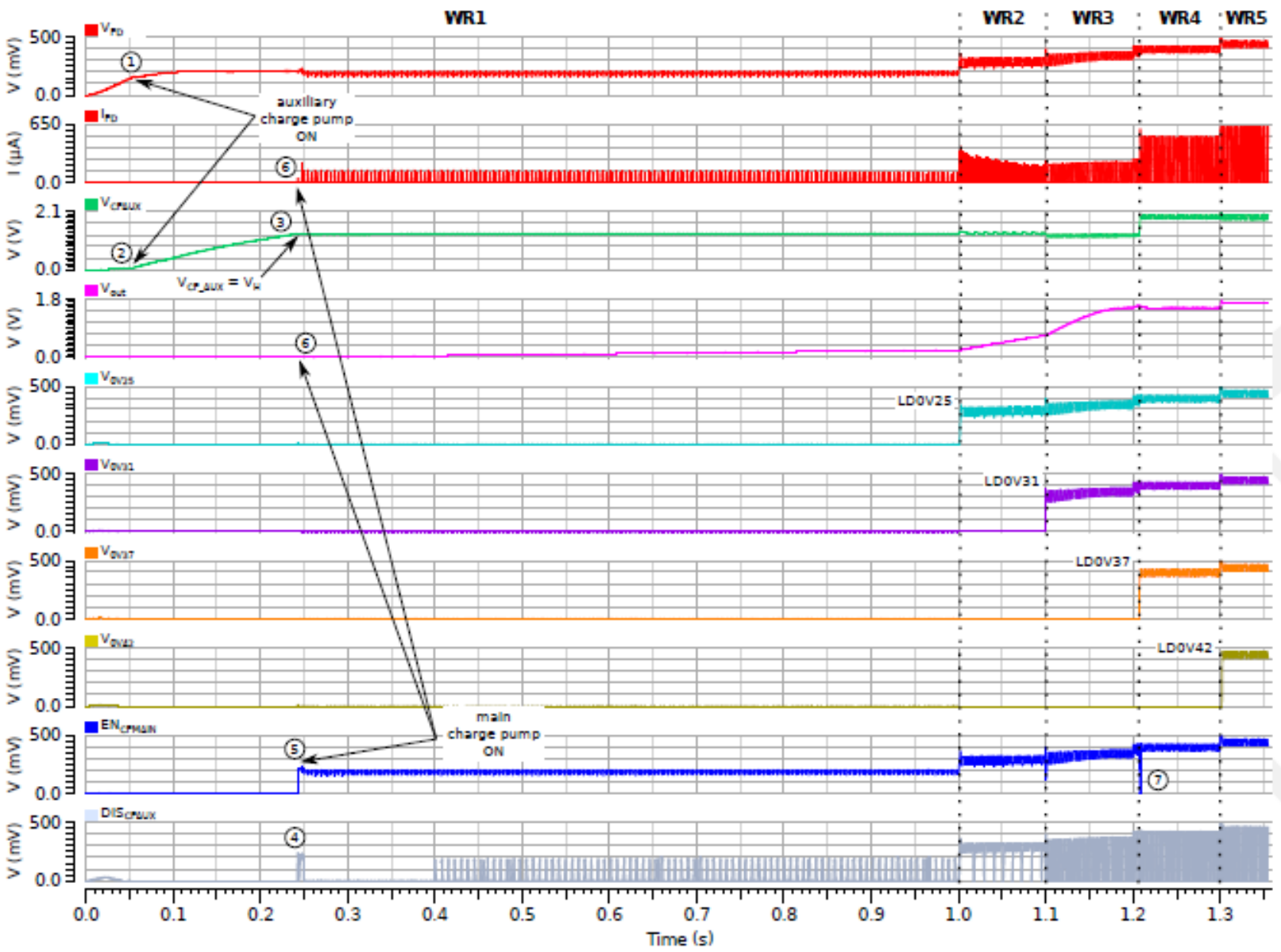
Micro-Energy Harvesting Chip Architecture



Micro-Energy Harvesting Chip Architecture



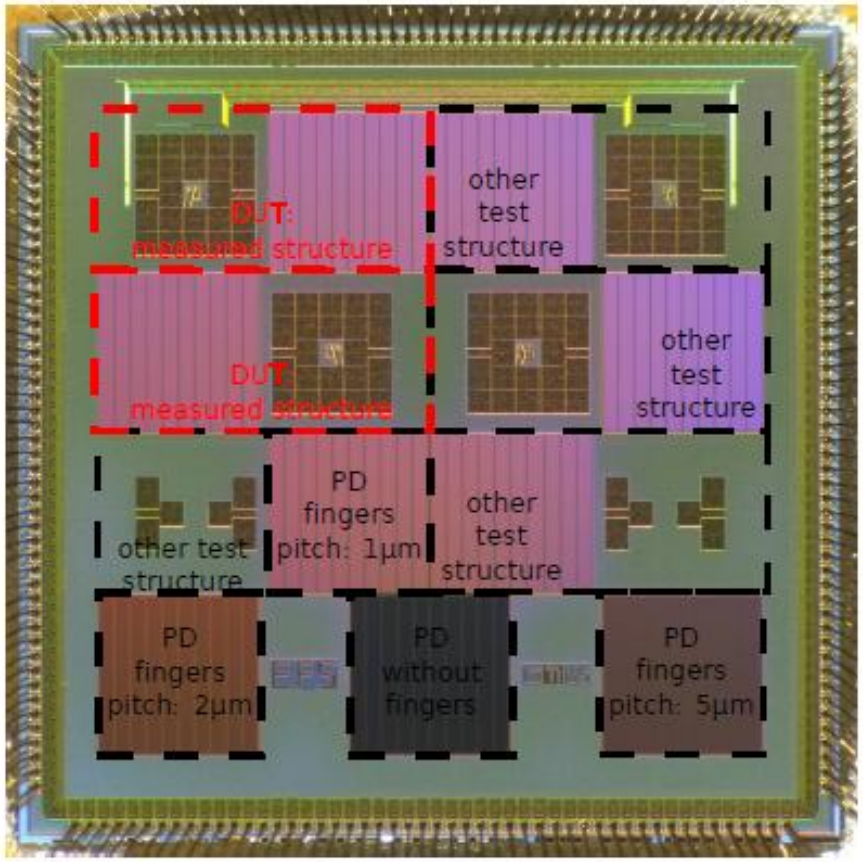
Micro-Energy Harvesting Chip Architecture

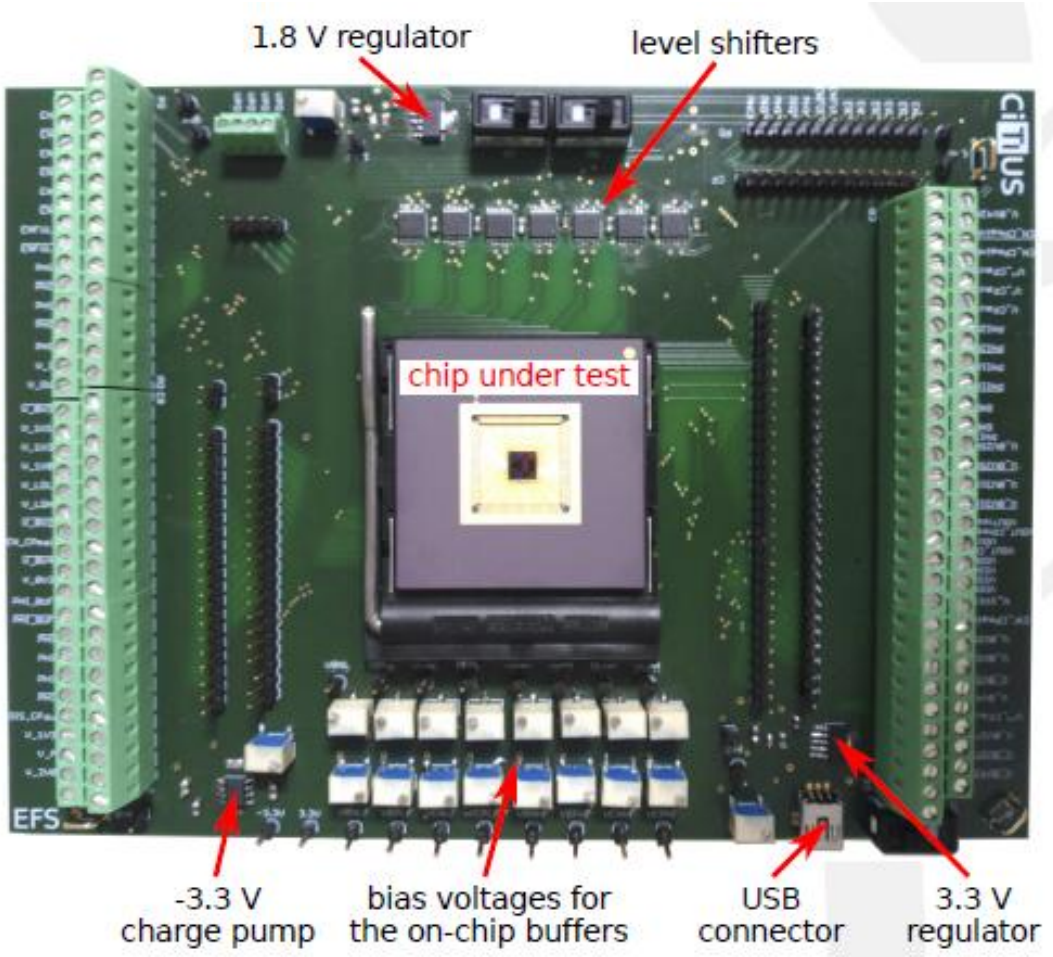


Proof-of-Concept Chip- Power Breakdown (Simulation)

WR	Average PMU input power (µW)	PMU output power (µW)	PMU consumed power (µW)	MPPT (%)	Auxiliary oscillator (%)	Auxiliary DC-DC converter (%)	Main oscilla-tor (%)	Main DC-DC converter (%)
1	0.0048	0.0011	0.0037	**0.74**	1.42	**64.88**	1.98	30.22
2	0.045	0.018	0.027	**0.40**	0.10	11.76	1.38	**86.00**
3	0.30	0.12	0.18	**0.13**	0.054	19.44	0.56	**79.76**
4	1.76	0.79	0.97	**0.063**	0.027	9.81	0.35	**89.64**
5	11.90	5.33	6.57	**0.012**	0.011	4.20	0.090	**95.68**

Proof-of-Concept Chip- Test Structure

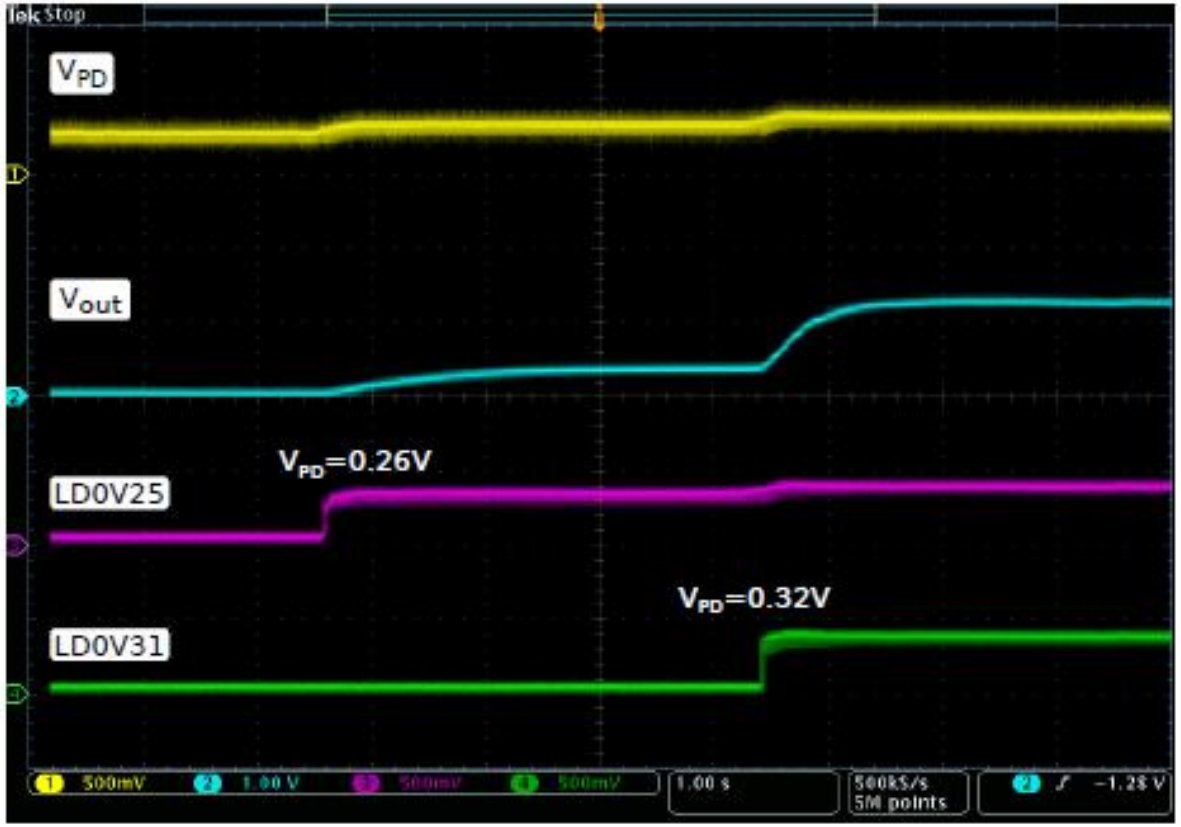


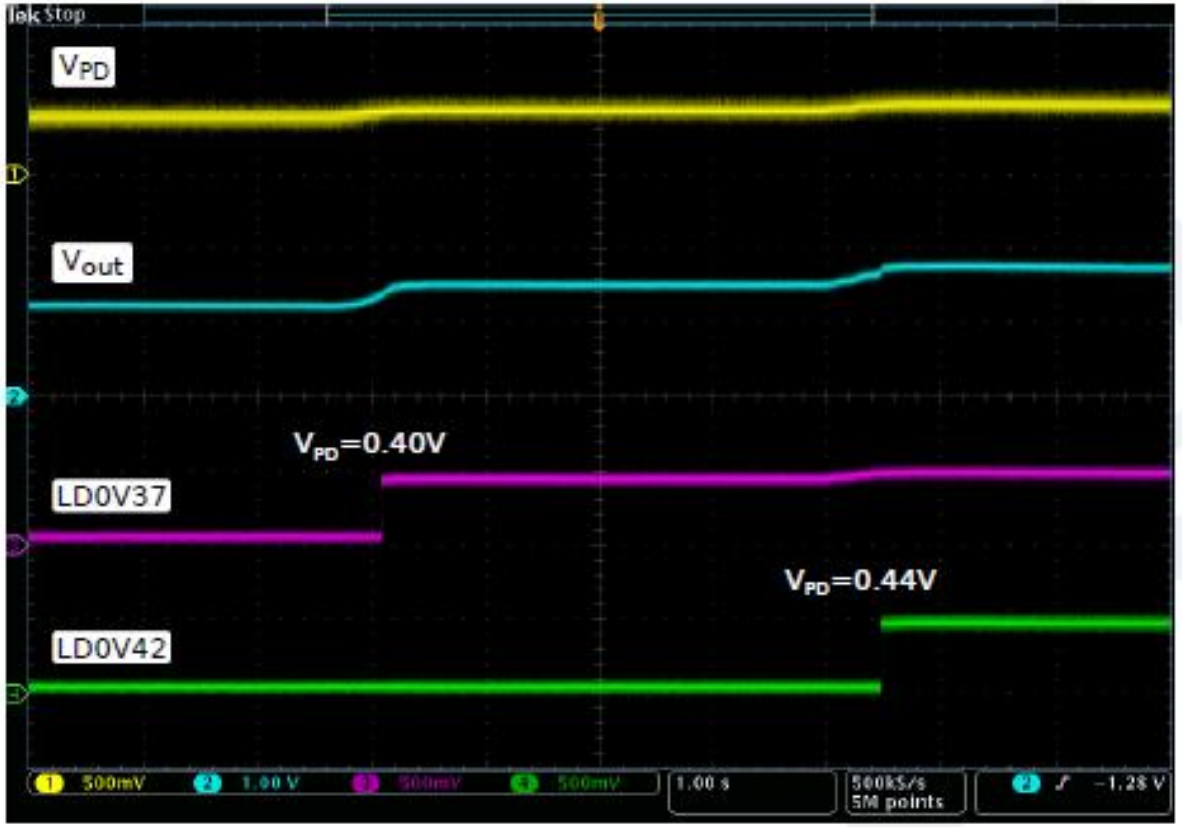


Proof-of-Concept Chip- Experimental Set-Up

Proof-of-Concept Chip- Experimental Results- Working Regions (WR's)

- Expected voltage levels (WR thresholds)- 0.25 V, 0.31 V, 0.37 V, 0.42 V
- Measured voltage levels (WR thresholds)- 0.258 V, 0.316 V, 0.40 V, 0.44 V





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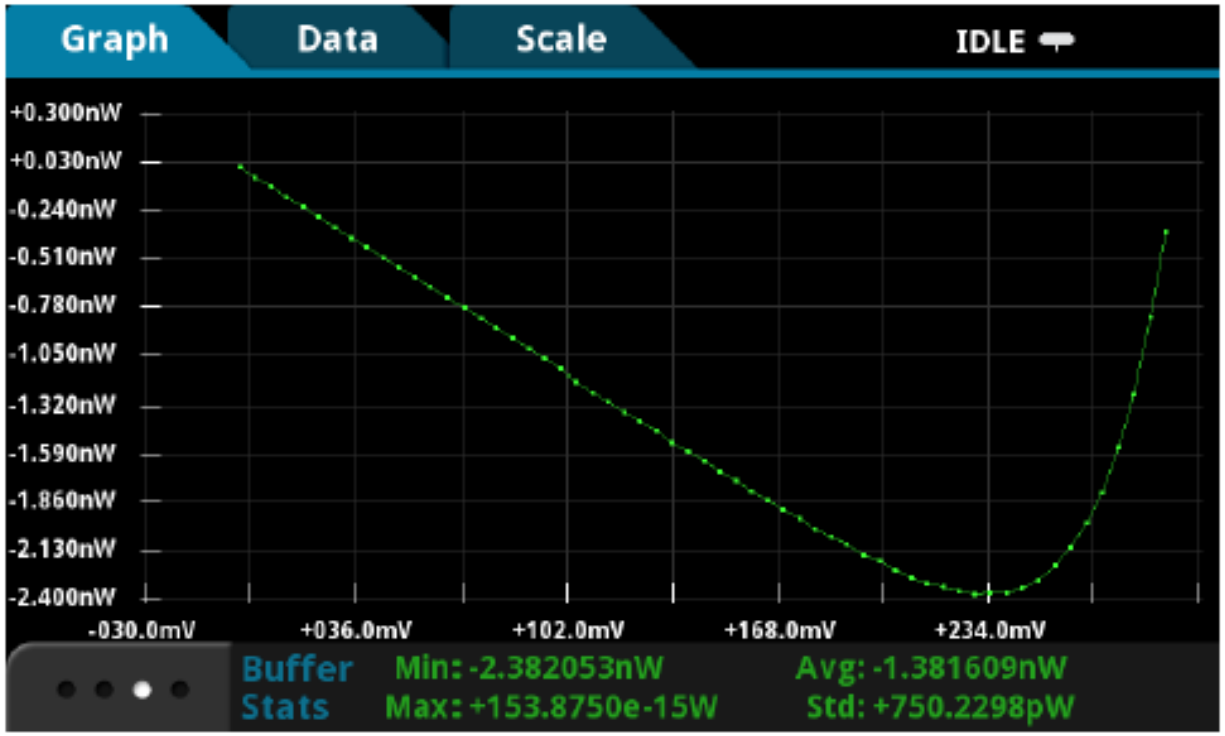
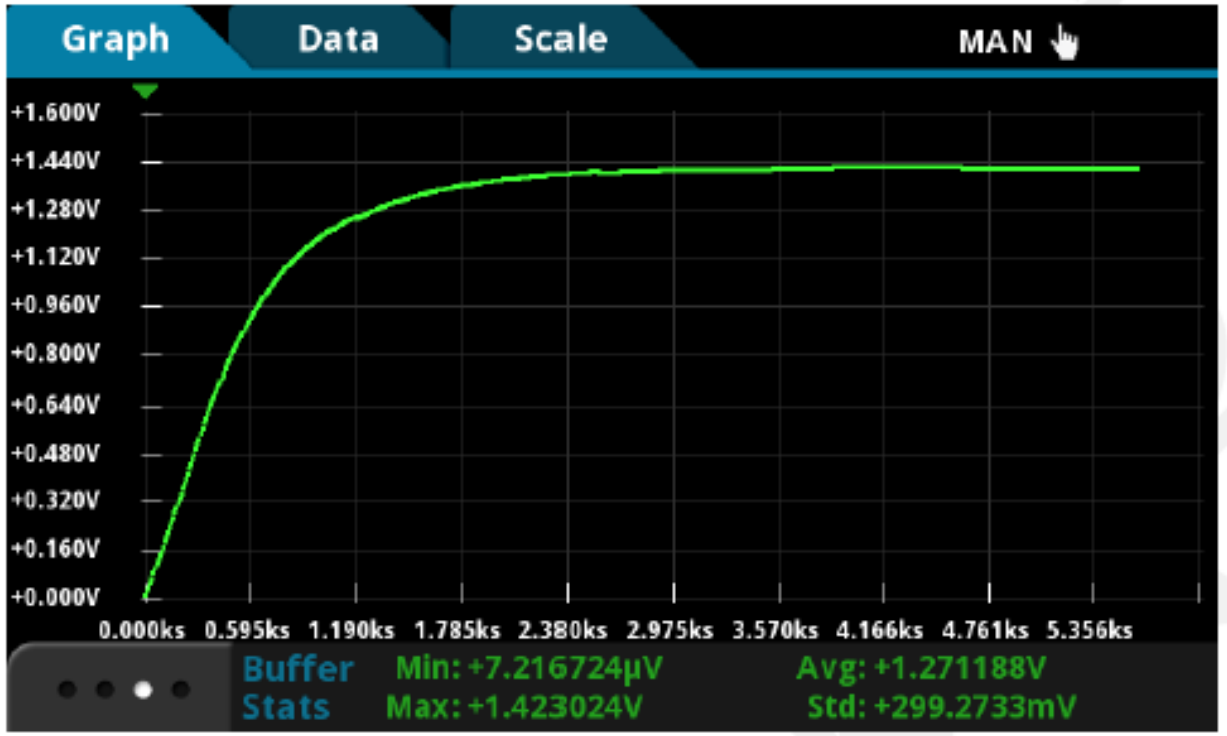
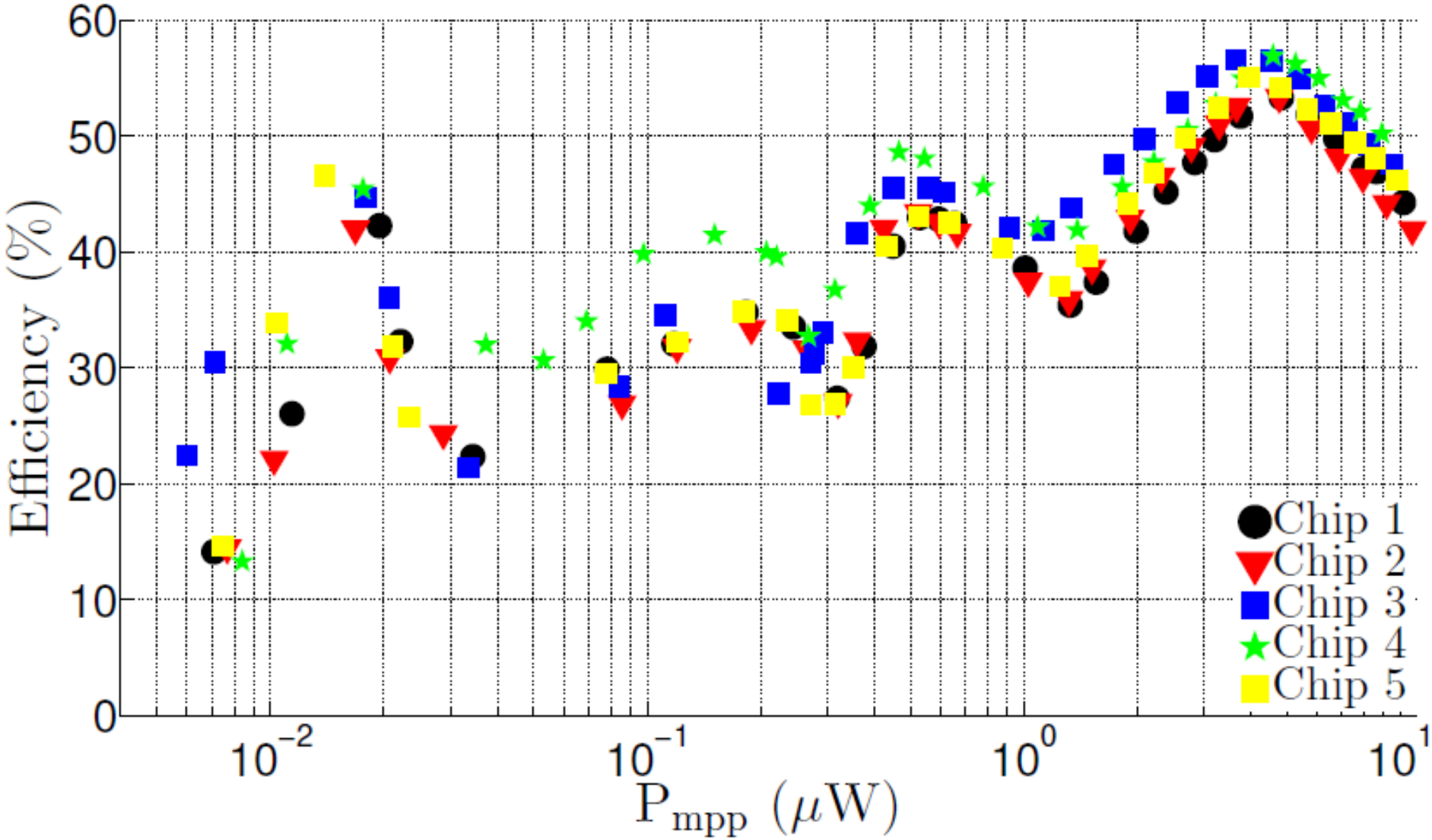
Proof-of-Concept Chip- Experimental Results- Cold Start-Up

- Results with an off-chip 100 nF Ta capacitor
- Start-up power- 2.38 nW





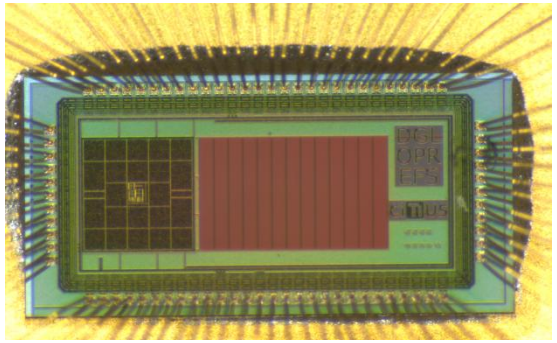
Proof-of-Concept Chip- Experimental Results- End-to-End Efficiency



Proof-of-Concept Chip- State-of-the-Art Comparison

	Martins TBCAS	Chandrakasan JSSC	Blaauw ISSCC	Sinencio ISSCC	Blaauw JSSC	This Work
Technology	standard 0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	standard 0.18 µm CMOS
Voltage boosting	charge pump	boost with voltage doubler	self-oscillating voltage doubler	charge pump	discontinuous charge pump	charge pump
Transducer + PMU on-chip	yes	no	no	no	no	yes
Transducer + PMU area (mm^2)	1.3 + 0.24	- + 1.53	- + 0.86	- + 0.552	- + 2.72 + off-chip cap.	1 + 0.575
Input power range (nW)	-	1.1 - 6.25	1.7 - 12500	5900 - 47000	0.02 - 1500	2.38 - >10000
Output power range (nW)	-	0.544 - 4	0.5 - 5000	3840 - 30550	0.005 - 600	0 - 4500
Cold start-up	yes	no	yes	yes	no	yes
Minimum input power to start-up (nW)	-	-	6	-	-	2.38
MPPT	no	no	user-operated	yes	yes	yes
Output regulation	no	no	no	yes	no	no
End-to-end peak efficiency (%) @ P_{out} (µW)	67@1.27	53@0.0012	50@0.12	72@-	50@0.008	57@2.07

Proof-of-Concept Chip- Off-the-Shelf PMU's Comparison



	Our Chip	BQ25570 Texas Inst. March 2015	BQ25504 Texas Inst. June 2015
Size	On-chip solar cell and PMU < 1.6 mm^2	PMU 3.5 mm x 3.5 mm	PMU 3.5 mm x 3.5 mm
Start-Up current	< 5 nA (9.52 nA x 0.25 V)	15 uW (60.000 nA x 0.25 V)	15 uW (60.000 nA x 0.25 V)
Off-chip components	No	Inductors and resistors	Inductors and resistors
Bias current	nA	448 nA	330 nA

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Conclusions and Outlook

- Past and on-going work
  - Device modeling and experimental characterization
  - Focal-Plane Processing, in standard CMOS technologies for conventional Computer Vision algorithms
  - Light micro-energy harvesting in standard CMOS technologies for implantable, wearable or IoT devices

- Future work- MENELAOS^{NT} (ETN- 2020- 2023, European Funding), ENVISAGE (2019- 2021, Spanish Funding)
  - Time-of-flight sensors (standard CMOS technologies)
  - CMOS vision sensors incorporating deep learning techniques
  - Light micro-energy harvesting in standard CMOS technologies

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Thanks for your attention!