# The lonely perpetrator in the DCDC FEAST2 case

## How an individual transistor threatened the operation of the CMS pixel detector

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These slides have been prepared solely for the purpose of supporting an oral presentation and are not suitable to convey a clear message outside this context.

A full report as well as an executive report are available at the following link:

**http://project-dcdc.web.cern.ch/project-DCDC/public/Reports.html**

***Investigation = the act or process of examining a crime, problem, statement, etc. carefully, especially to discover the truth***

# The truth about the FEAST2 affair

**The crime scene**

**Witnesses**

**The autopsy**

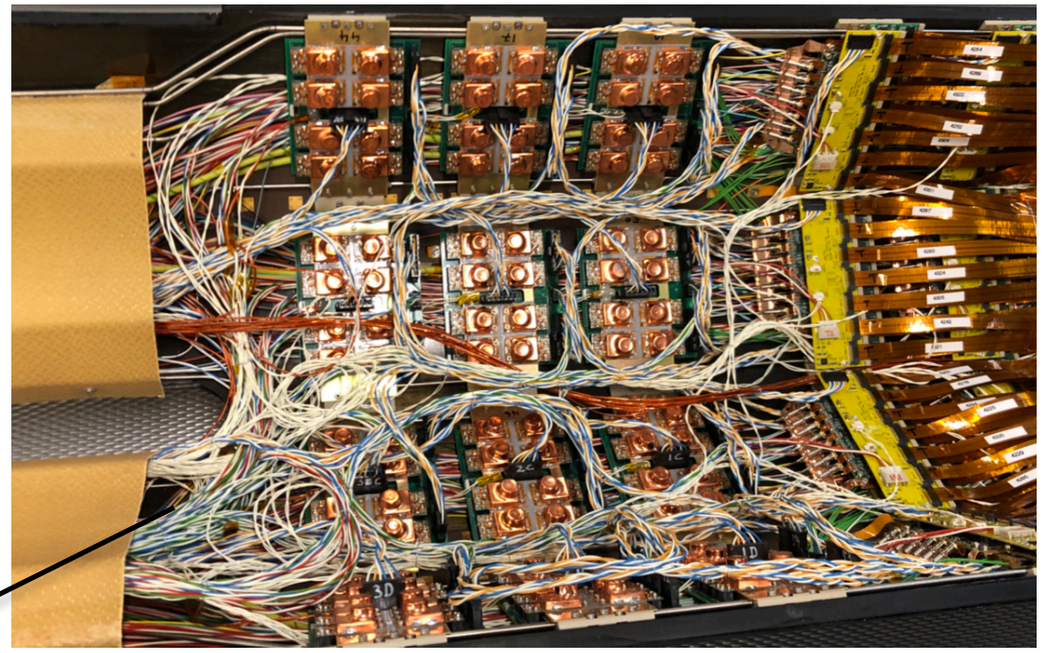
**The motive**

**The crime reconstruction**

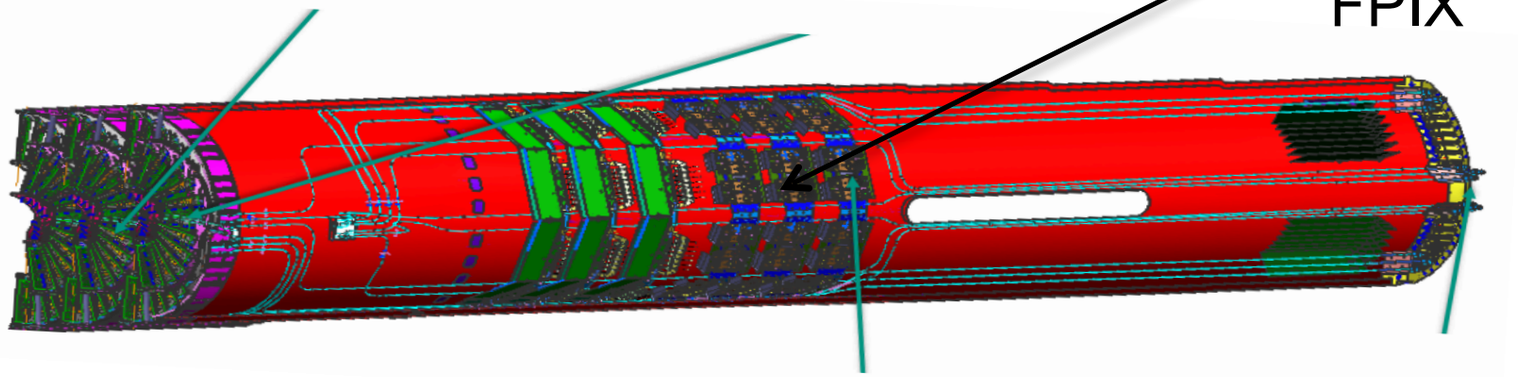
**The perpetrator**

# The crime scene

# FEAST2 in the CMS pixel detector



FPIX

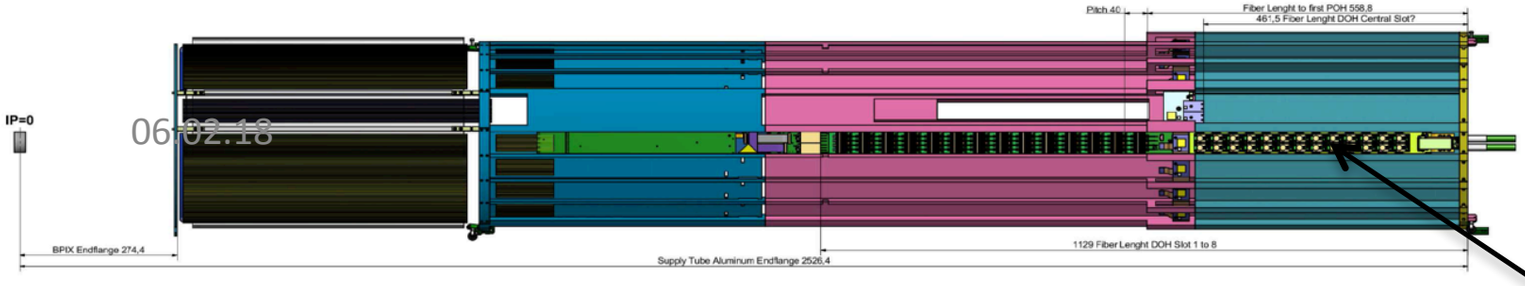


384 in total

IP

Bpix DC-DC: radius 240mm, z range 2067- 2430mm from i/p.
Fpix DC-DC: radius 140mm, z range 1315-1530mm from i/p

BPIX



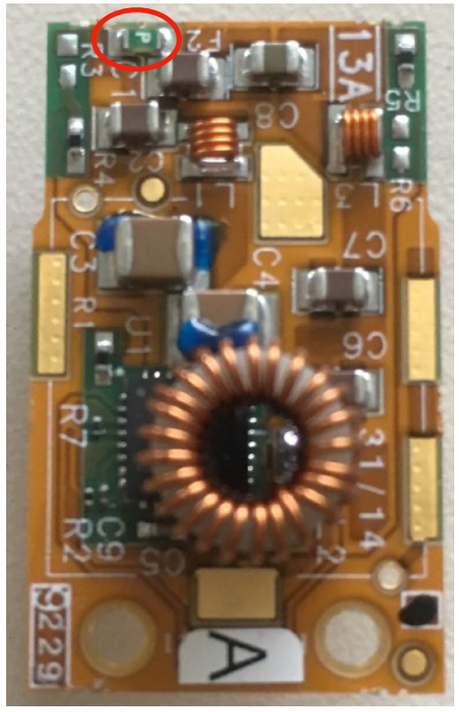

832 in total

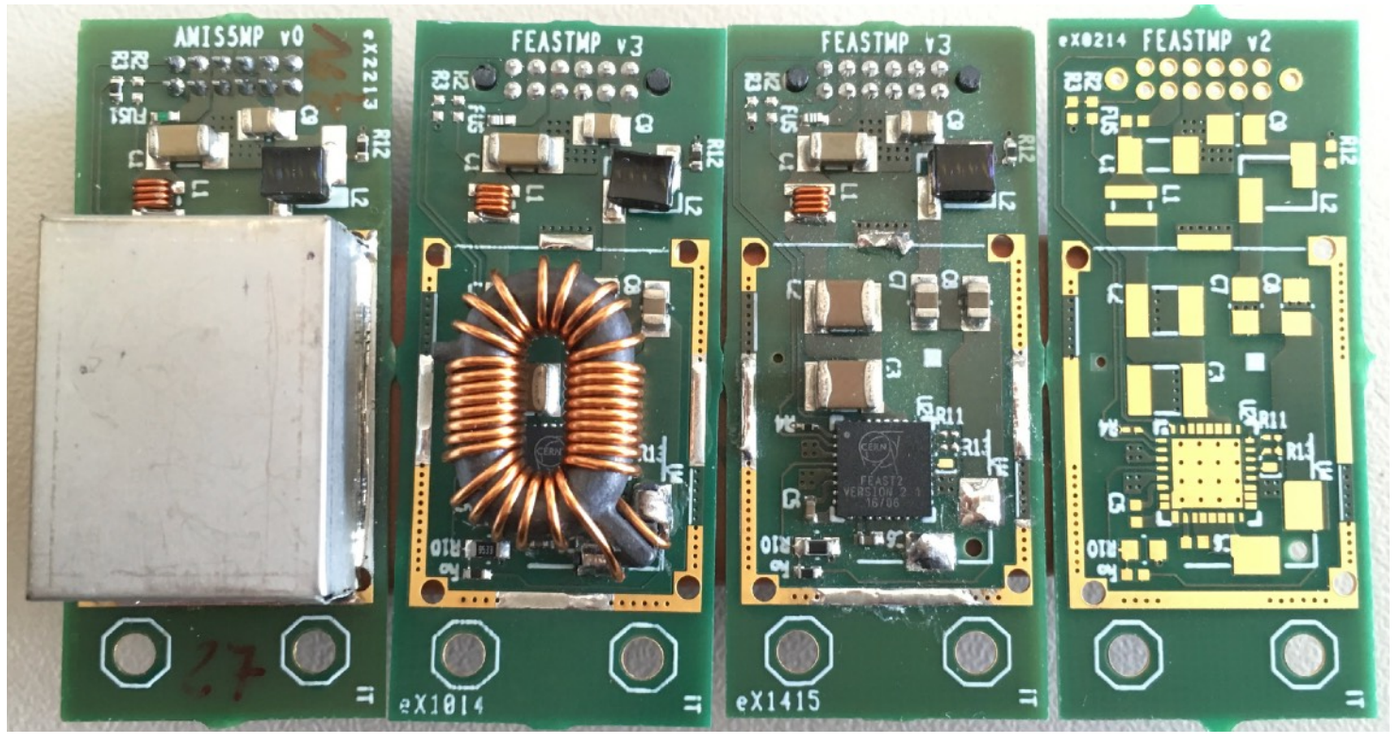
**Cooling at -20°C**

# Module in the CMS pixels

# Module everywhere else

This fuse prevents
the lowering of Vin



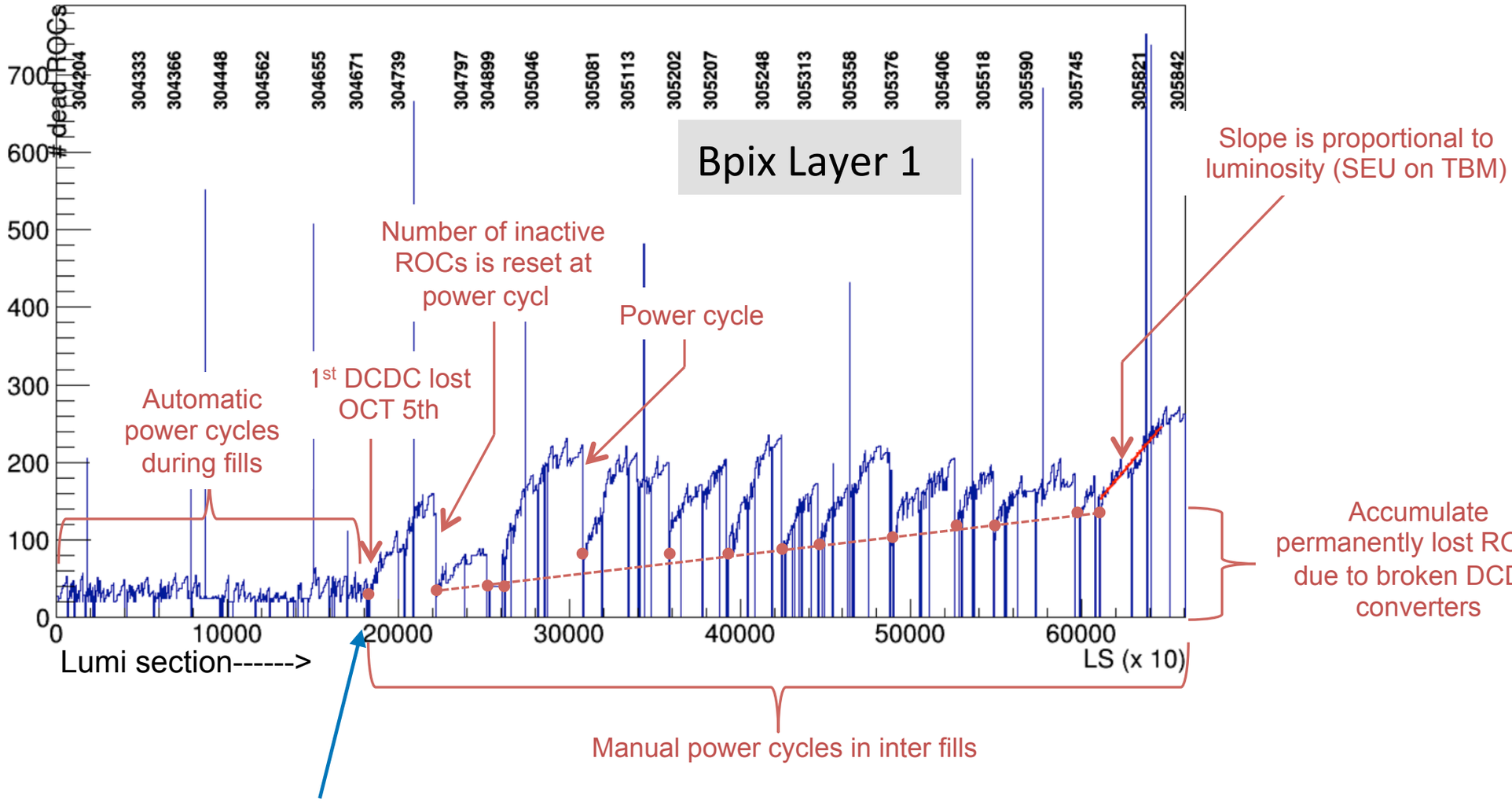

**Aachen module**

**CERN module (FEASTMP)**

**Vin 12V** — **FEAST2 module** — **Vout 2.5-3.3V**

# Witnesses

# Failure of FEAST DCDCs in the CMS pixel detector




**No correlation with:**

- output voltage
- output current
- position in the detector
- anything other than the beam

**DCDCs fail during disable/enable cycles**

# Plan around November 2017

**Rest of 2017 Physics Run**

Nothing can be done.
Accept loss of modules

**YETS 17-18**

Request longer Year-End Stop
Open the detector
Extract all DCDC modules
Replace (all?) modules (fuse changed)

**2018 Physics Run**

Find a patch ensuring
data taking

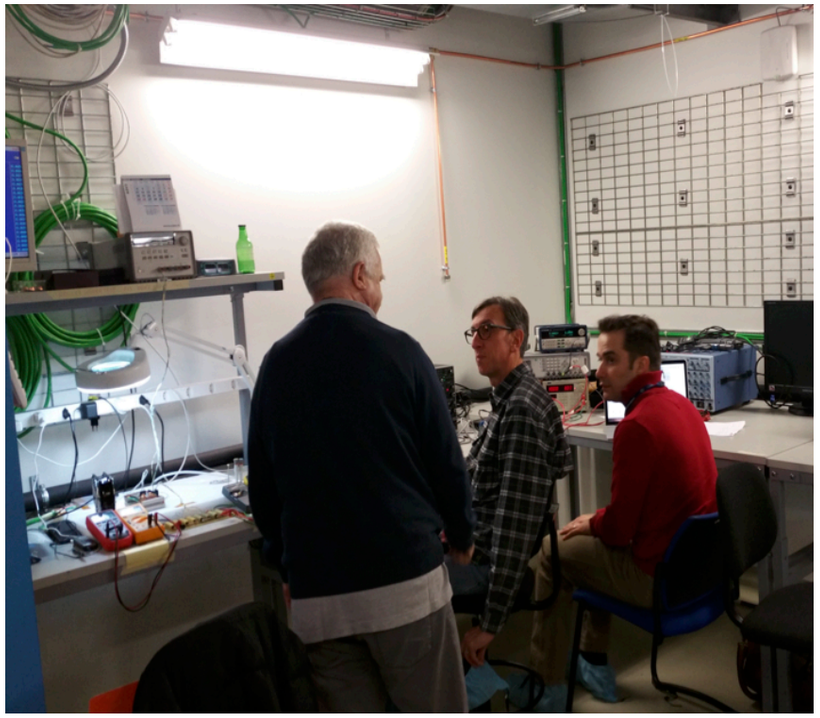
**LS2**

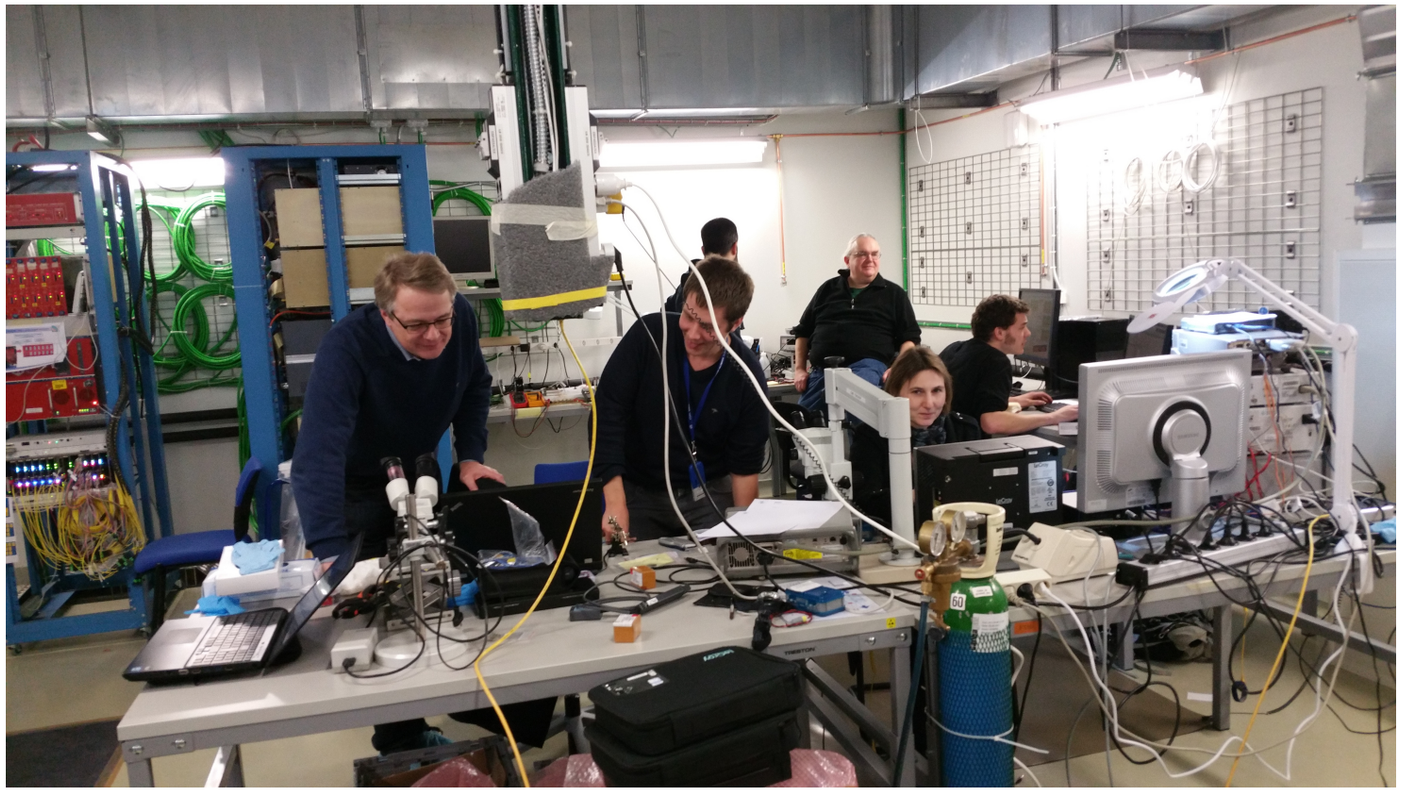
Solve the problem
for the long term

"At this pace, game over
for CMS around May 2018"

# The autopsy

# YETS 17-18: Merry Christmas!





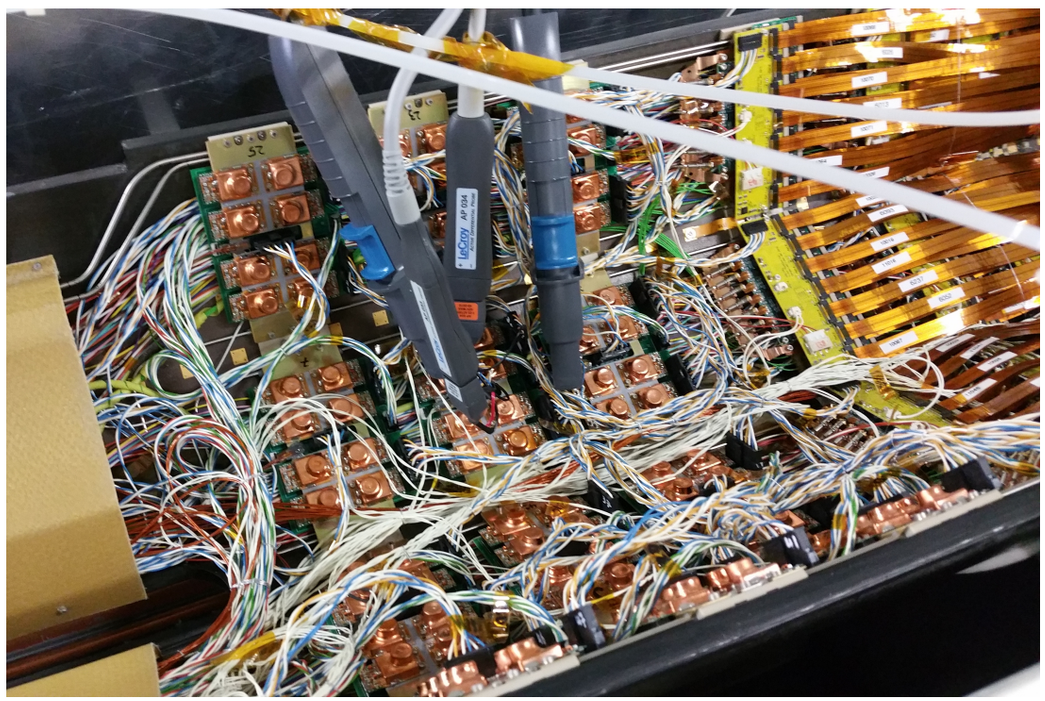


Photo memories from the 2017 Christmas Break

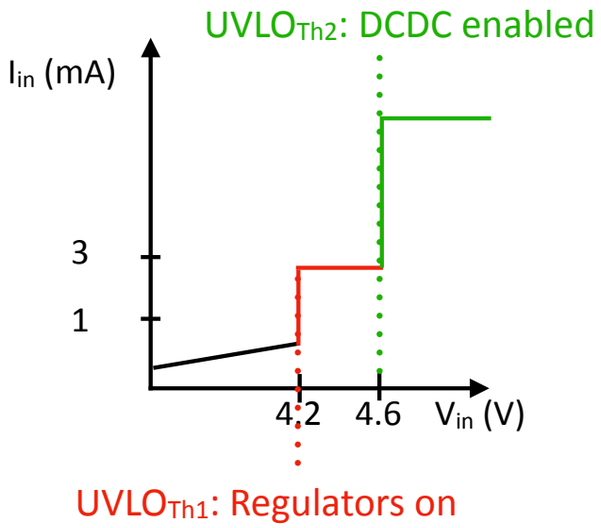
# FEAST2 modules in the CMS experiment were found to present 2 distinct types of damage

- “Broken” samples failed to provide any output voltage
- “High-current” samples were perfectly functional, but were found to have an excessive current below UVLO

Perfectly working in the system but found to have anomalous current when tested

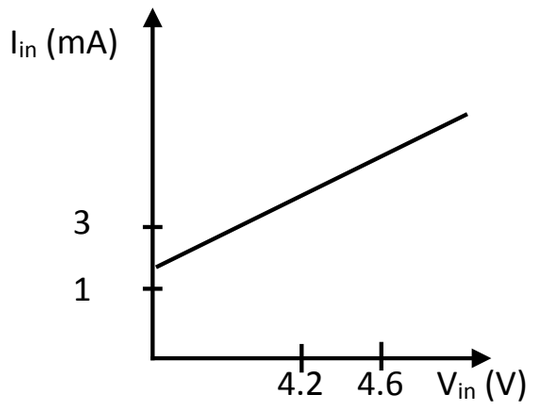
| | Pixel Names | Number of Converters | Tested Broken | Tested working with High Current | Tested working with normal current | BROKEN | HIGH CURRENT |
|---|---|---|---|---|---|---|---|
| | | TOTAL | "BROKEN" | "HIGH CURRENT" | "GOOD" | % with respect to total | % with respect to total working |
| BPIX (+Z, Near) | BPIX-BpI | 208 | 4 | 48 | 156 | 1.9 | 23.5 |
| BPIX (-Z, Near) | BPIX-BmI | 208 | 10 | 48 | 150 | 4.8 | 24.2 |
| BPIX (+Z, Far) | BPIX-BpO | 208 | 13 | 70 | 125 | 6.3 | 35.9 |
| BPIX (-Z, Far) | BPIX-BmO | 208 | 11 | 70 | 127 | 5.3 | 35.5 |
| FPIX (+Z, Near) | FPIX-BpI | 96 | 7 | 41 | 48 | 7.3 | 46.1 |
| FPIX (-Z, Near) | FPIX-BmI | 96 | 7 | 34 | 55 | 7.3 | 38.2 |
| FPIX (+Z, Far) | FPIX-BpO | 96 | 9 | 23 | 64 | 9.4 | 26.4 |
| FPIX (-Z, Far) | FPIX-BmO | 96 | 6 | 22 | 68 | 6.3 | 24.4 |
| BPIX - not connected to modules | | 32 | 2 | 8 | 22 | 6.3 | 26.7 |

## “Good”



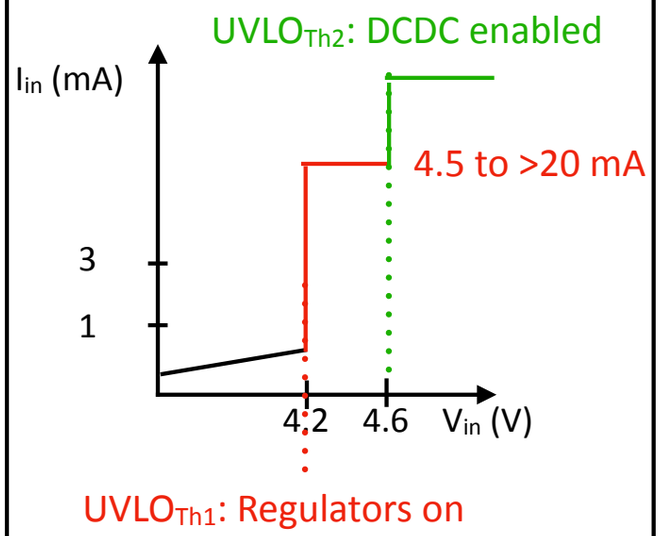

**Perfectly working in the experiment**

## “Broken”



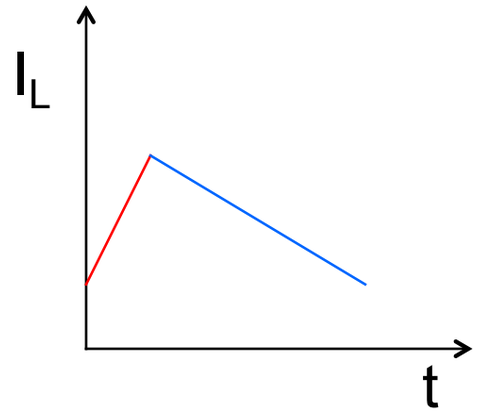

**Failed in the experiment**

## “High current”

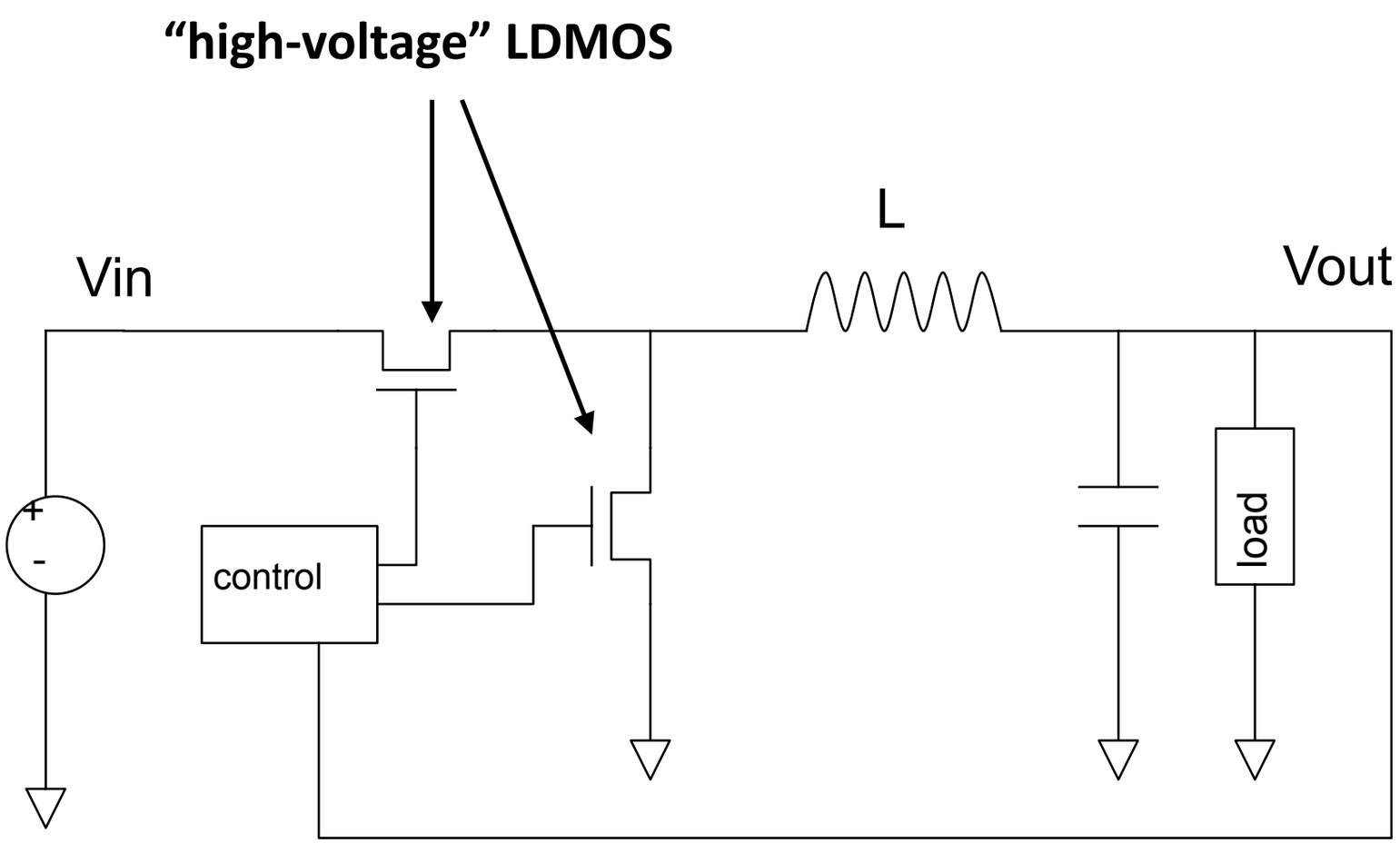



**Perfectly working in the experiment**

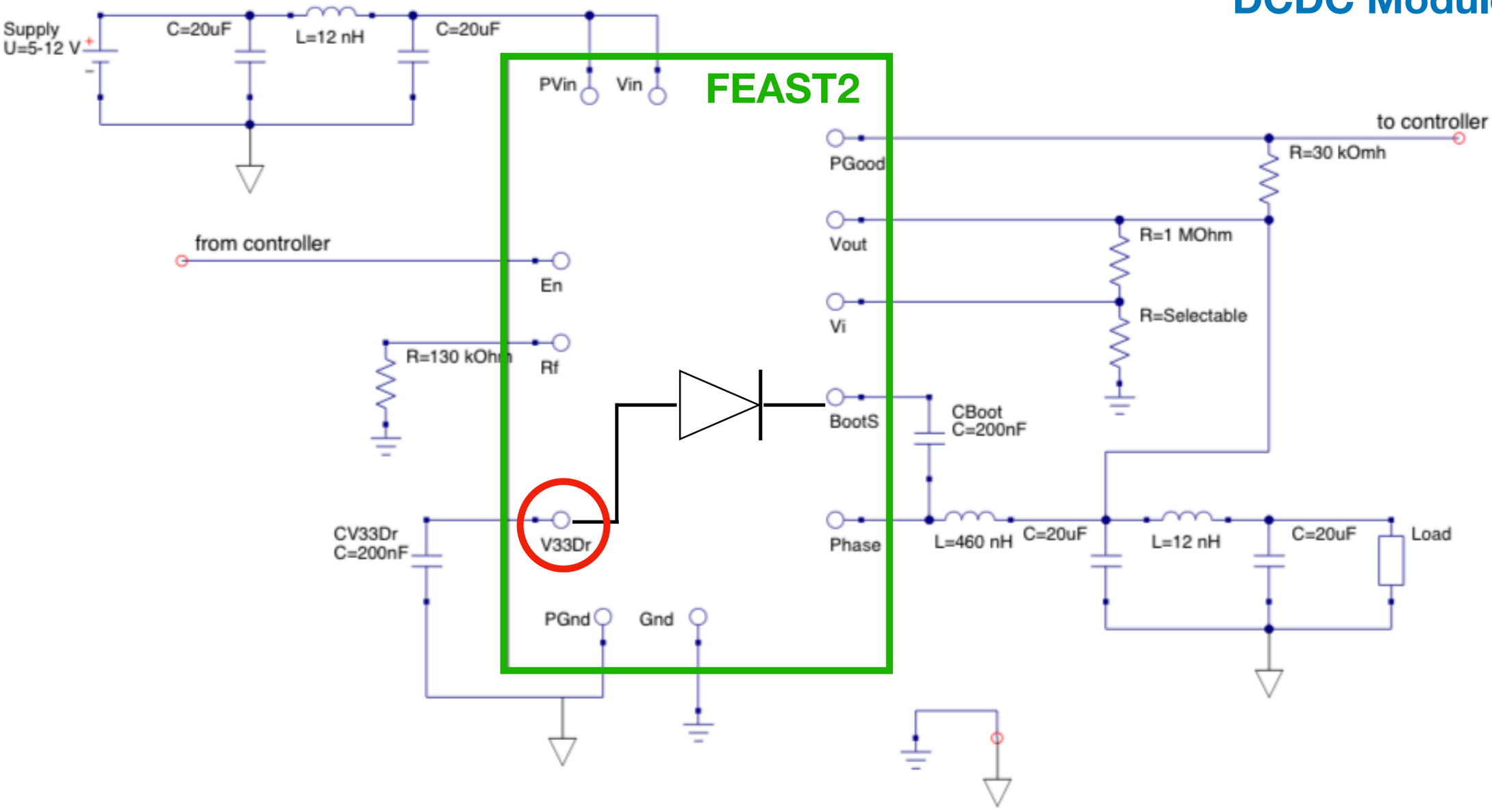
## Operation of a switching converter

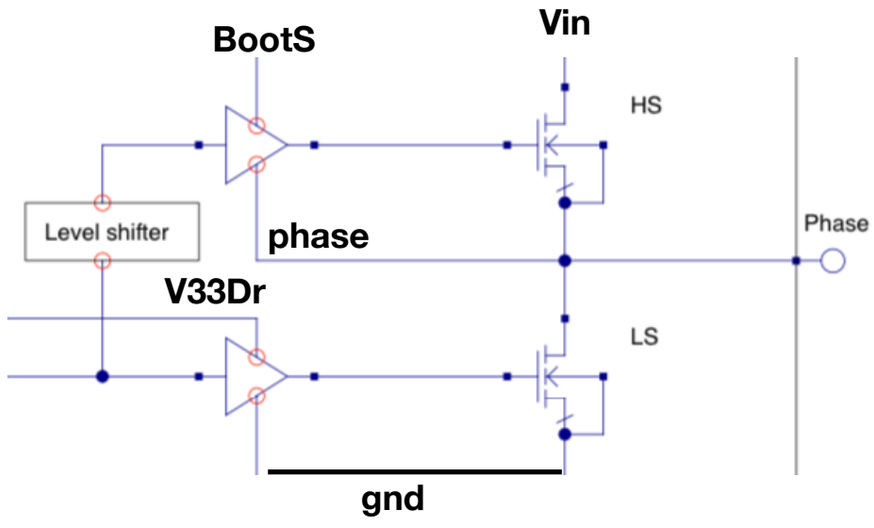



$$\frac{Vout}{Vin} = \text{Duty cycle}$$

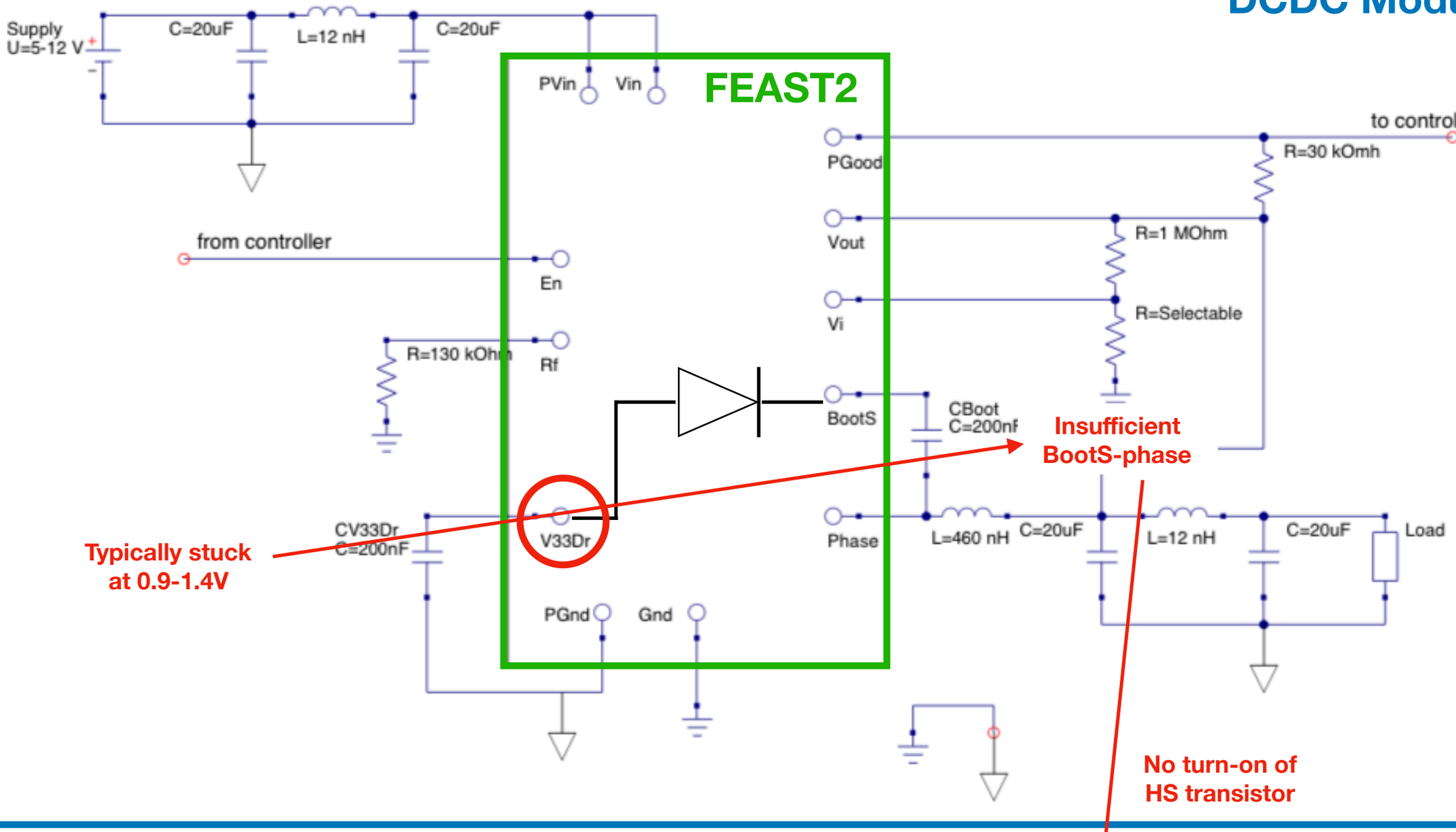


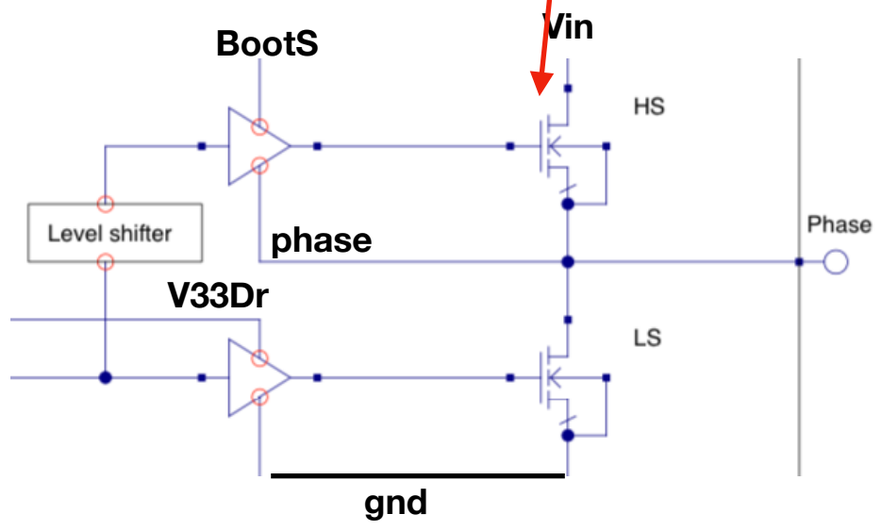
# DCDC Module


Supply
U=5-12 V
C=20uF
L=12 nH
C=20uF
PVin
Vin
FEAST2
PGood
to controller
R=30 kOmh
Vout
R=1 MOhm
Vi
R=Selectable
from controller
En
R=130 kOhm
Rf
BootS
CBoot
C=200nF
CV33Dr
C=200nF
V33Dr
Phase
L=460 nH
C=20uF
L=12 nH
C=20uF
Load
PGnd
Gnd

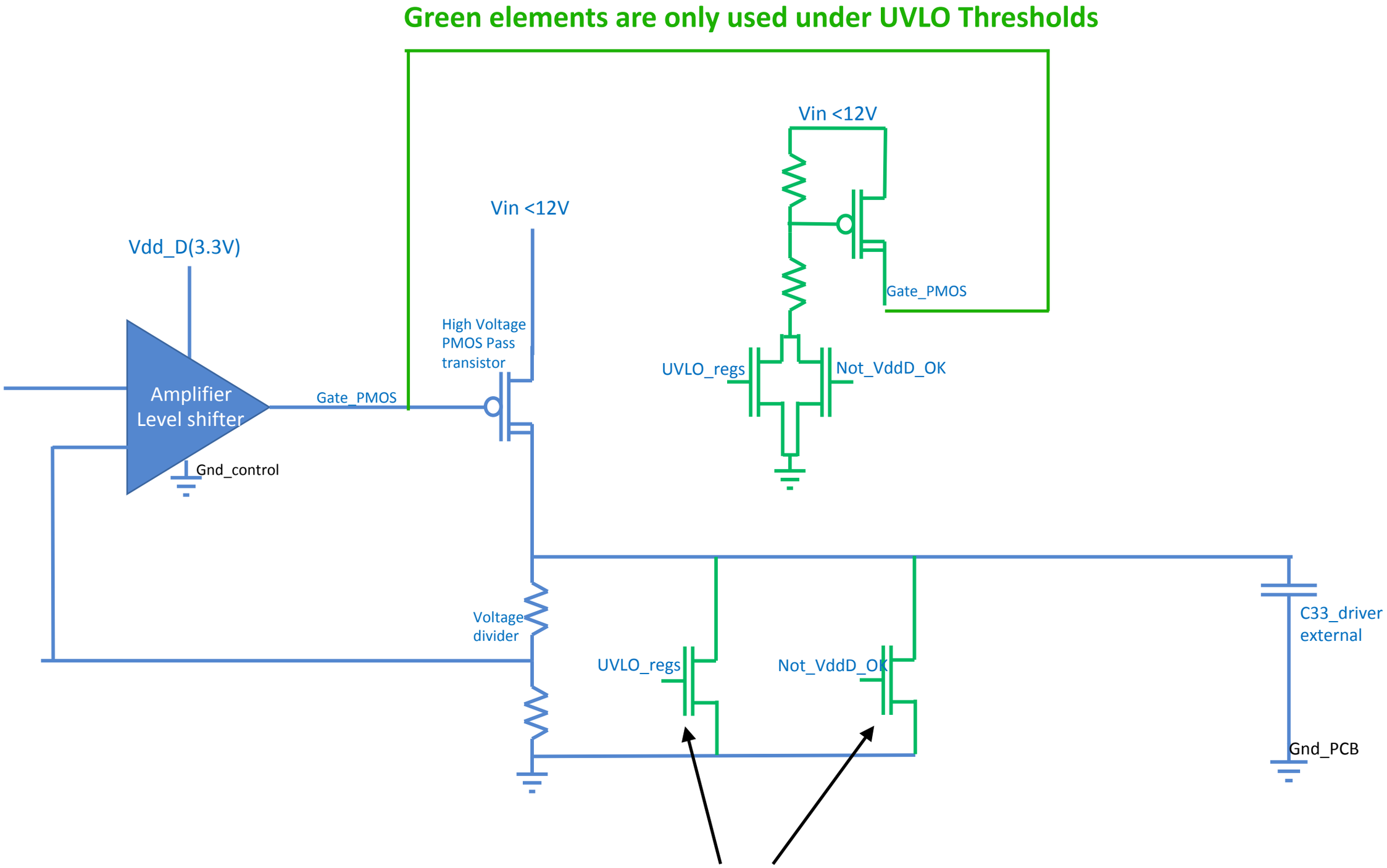

BootS
Vin
HS
Level shifter
phase
Phase
V33Dr
LS
gnd

# DCDC Module


Supply
U=5-12 V
C=20uF
L=12 nH
C=20uF
PVin
Vin
FEAST2
PGood
to controller
R=30 kOmh
Vout
R=1 MOhm
from controller
En
Vi
R=Selectable
R=130 kOhm
Rf
BootS
CBoot
C=200nF
Insufficient
BootS-phase
Typically stuck
at 0.9-1.4V
CV33Dr
C=200nF
V33Dr
Phase
L=460 nH
C=20uF
L=12 nH
C=20uF
Load
PGnd
Gnd
No turn-on of
HS transistor

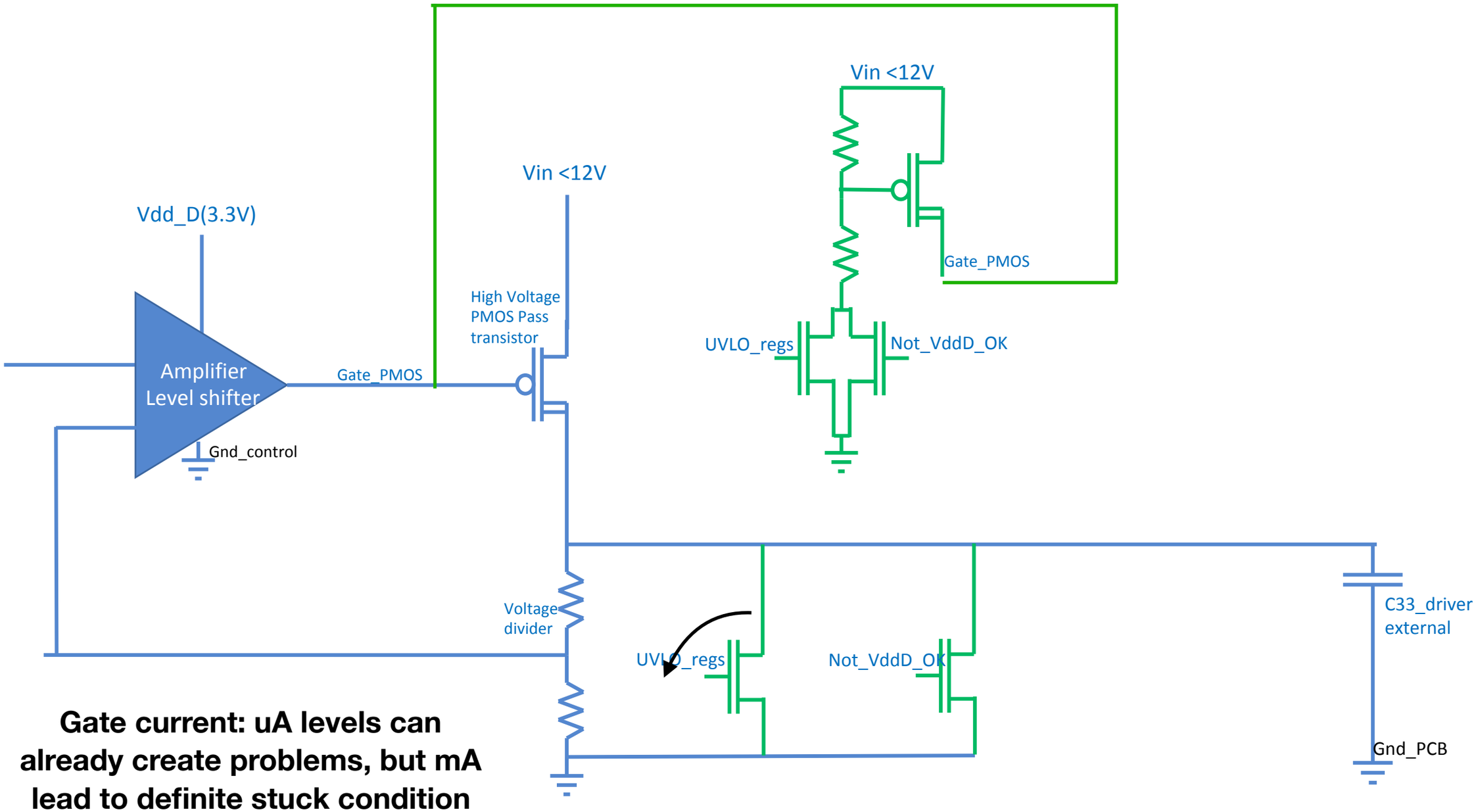

BootS
Vin
HS
Level shifter
phase
Phase
V33Dr
LS
gnd

# On-chip V33Dr regulator with clamps




**Clamp transistors for soft-start procedure (transistors rated to 3.3V)**

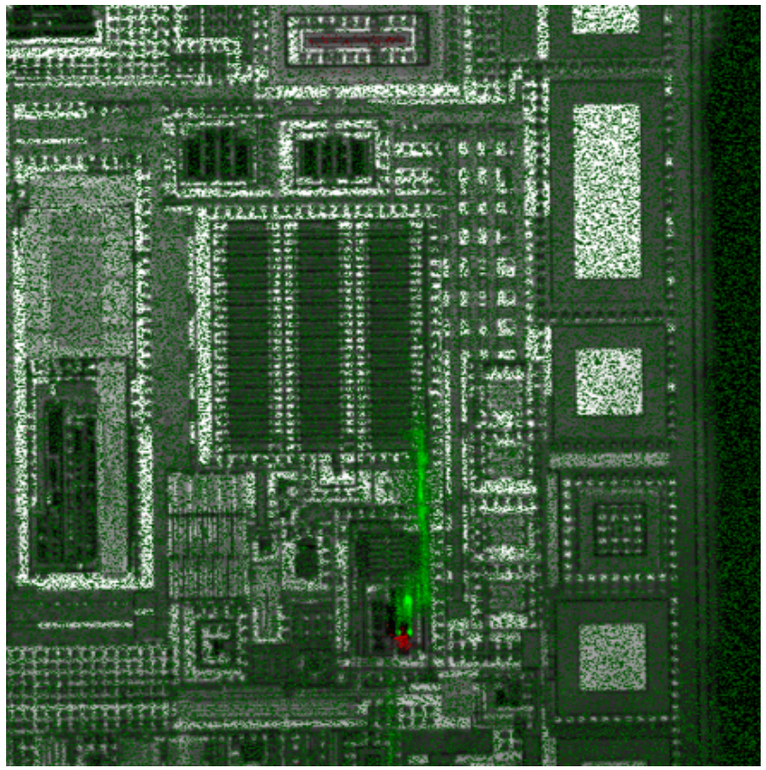
# What happens if the clamp transistors are damaged?



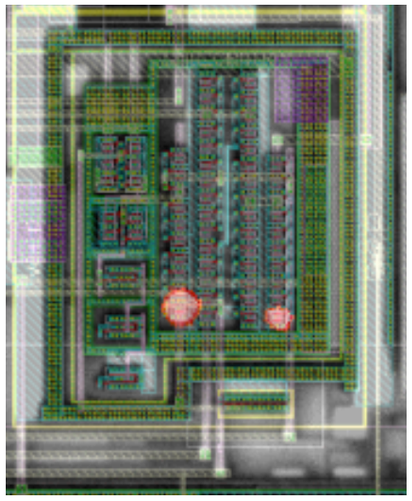

**Gate current: uA levels can already create problems, but mA lead to definite stuck condition**

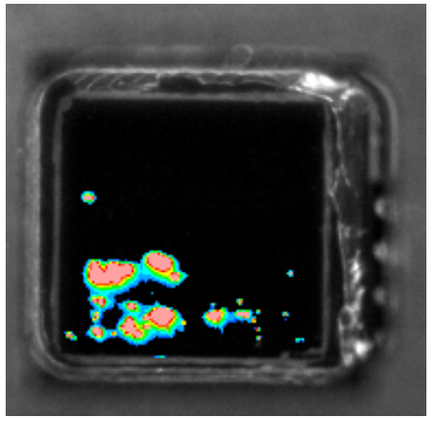
**This also disrupts the correct value of the UVLO_regs voltage, hence preventing the UVLO from working correctly**

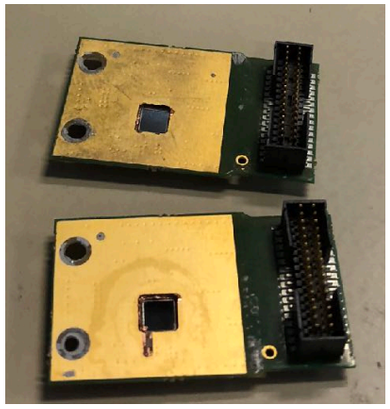
# Failure Analysis (FA) with emission microscopy and Optical Beam Induced Resistance Change (OBIRCH) at MASER (NL)

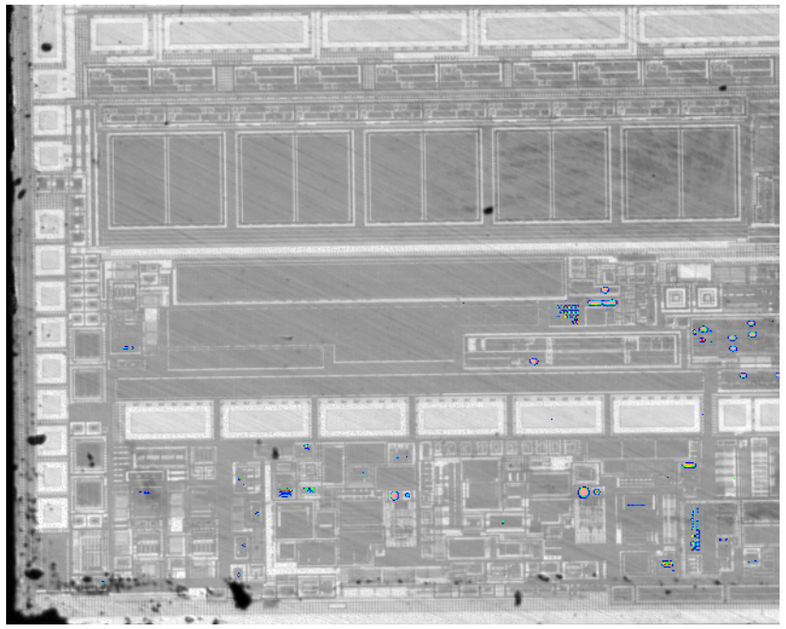


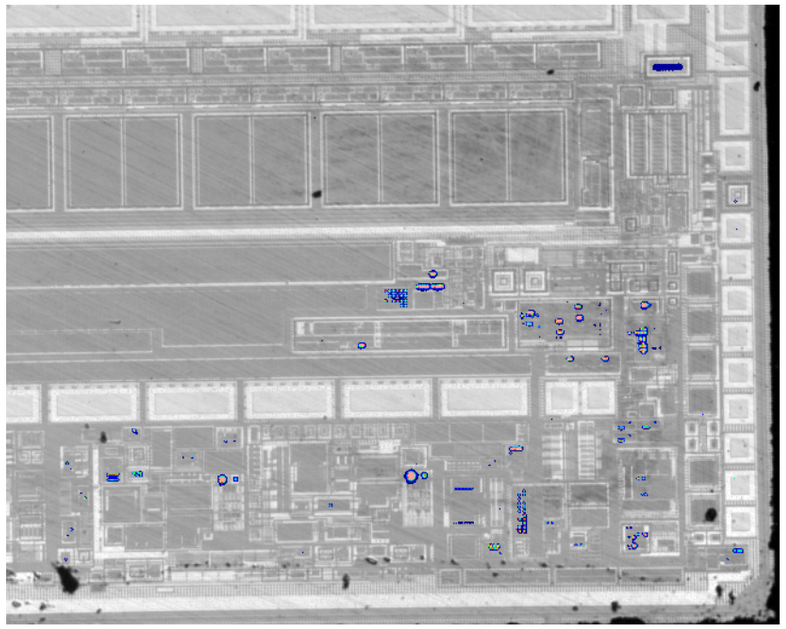
*During OBIRCH a laser beam selectively illuminates the metal lines, altering their resistance. The consequent input current change is measured, allowing the mapping of current paths. In broken FEAST2 samples, current flows to the clamp transistors.*











*Emission images are based on the detection of photons generated from hot carriers (therefore only conducting NMOS transistors are well visible). "Broken" or "High-current" FEAST2 samples showed different current paths.*

# The motive

## Why the clamp transistor(s) is(are) damaged?

Flawed ASICs?

Flawed PCBs?

Radiation in ASIC?

EM noise?

Radiation in package?

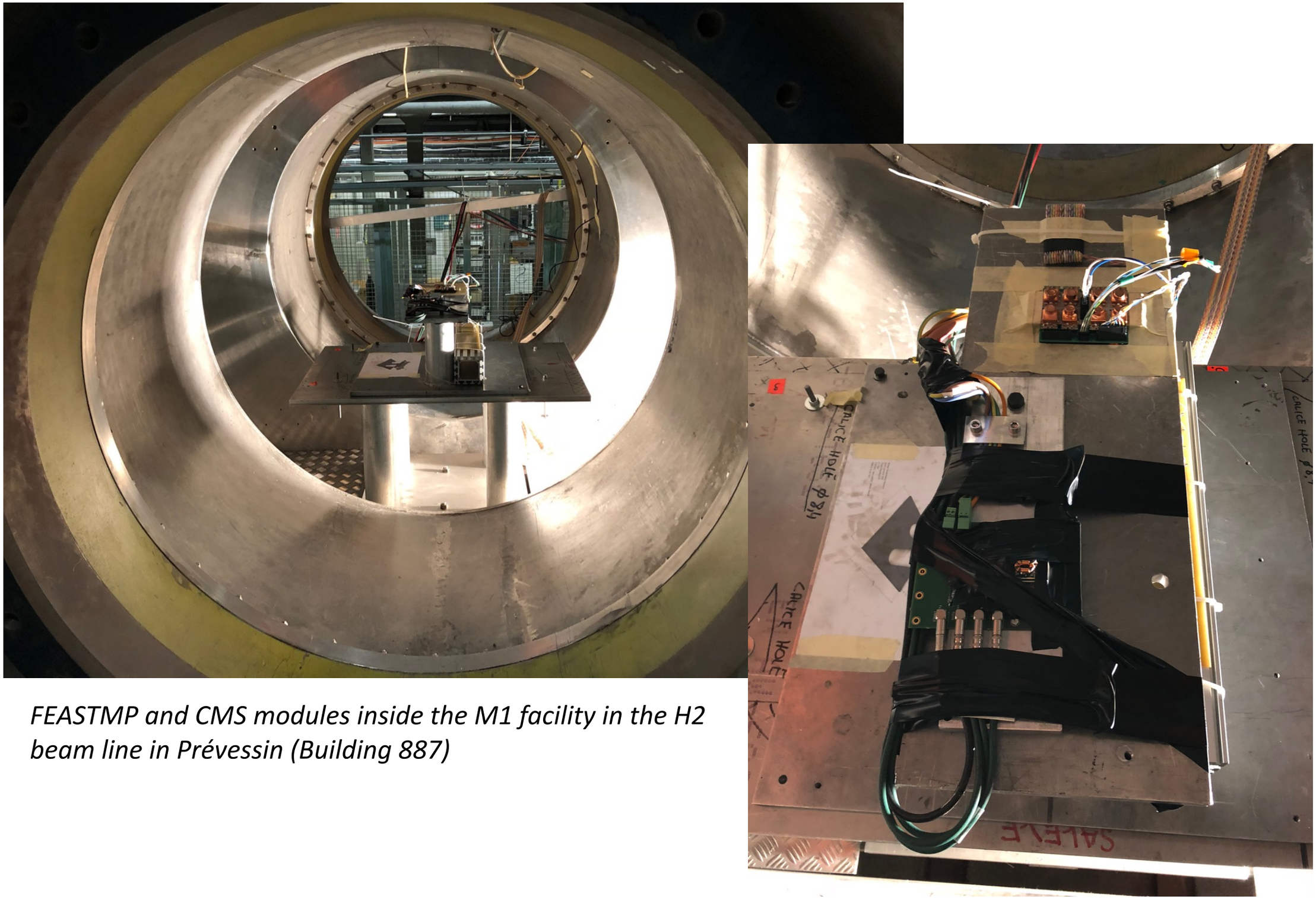
Environmental conditions?

Electrical stress?

Combination of any of the above??

# Environmental conditions?

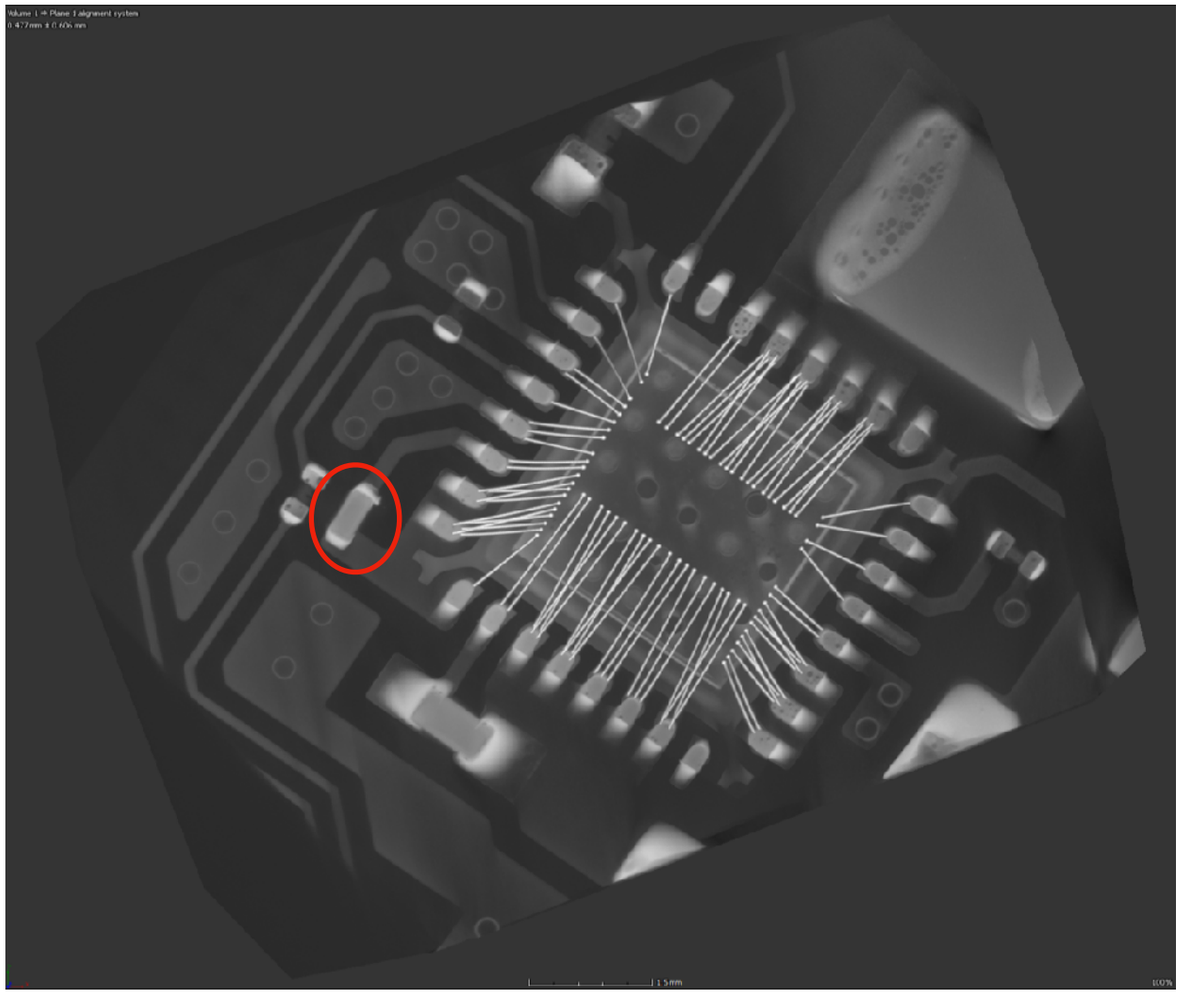
## Test in a 3T magnetic field revealed no problem



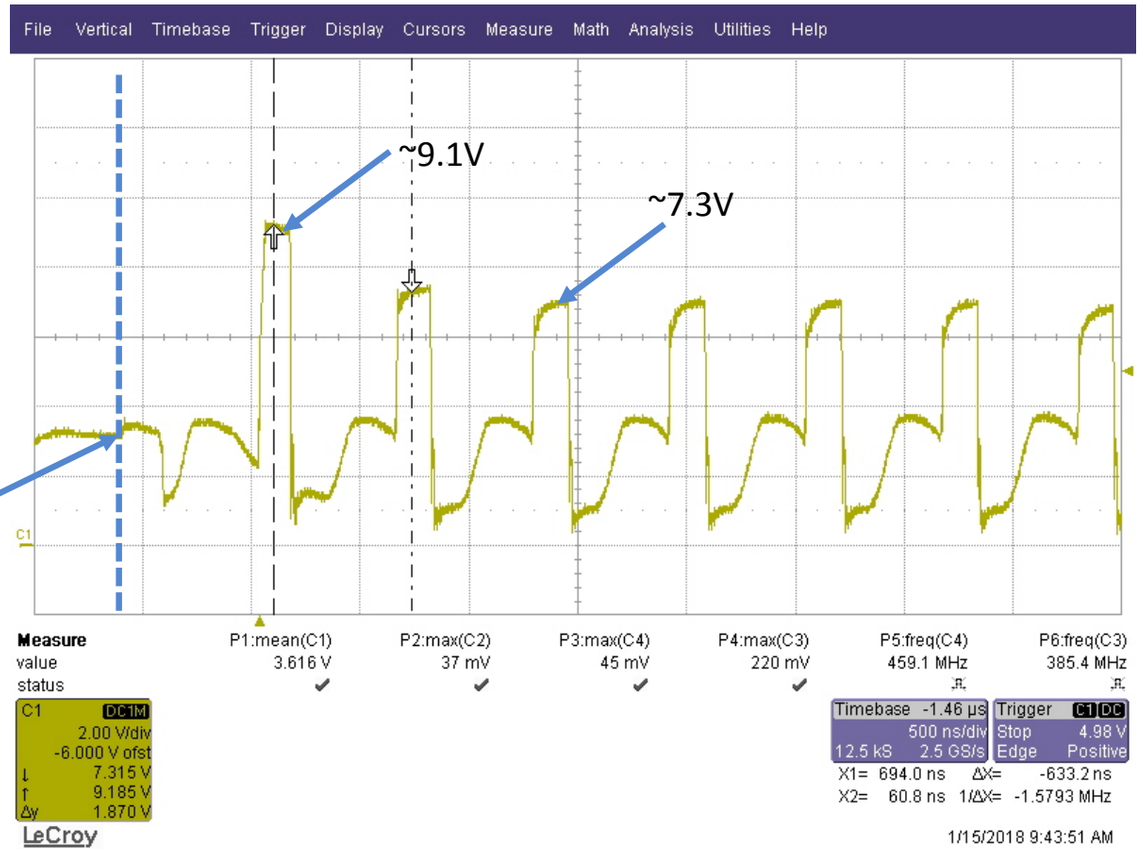

*FEASTMP and CMS modules inside the M1 facility in the H2 beam line in Prévessin (Building 887)*

# Flawed PCBs?

**Faulty capacitor, or intermittent contacts of the capacitor in the PCB generated a stress that produced somewhat similar damage**



*3D X-ray imaging of the module to inspect the quality of the soldering of the capacitor to the PCB*



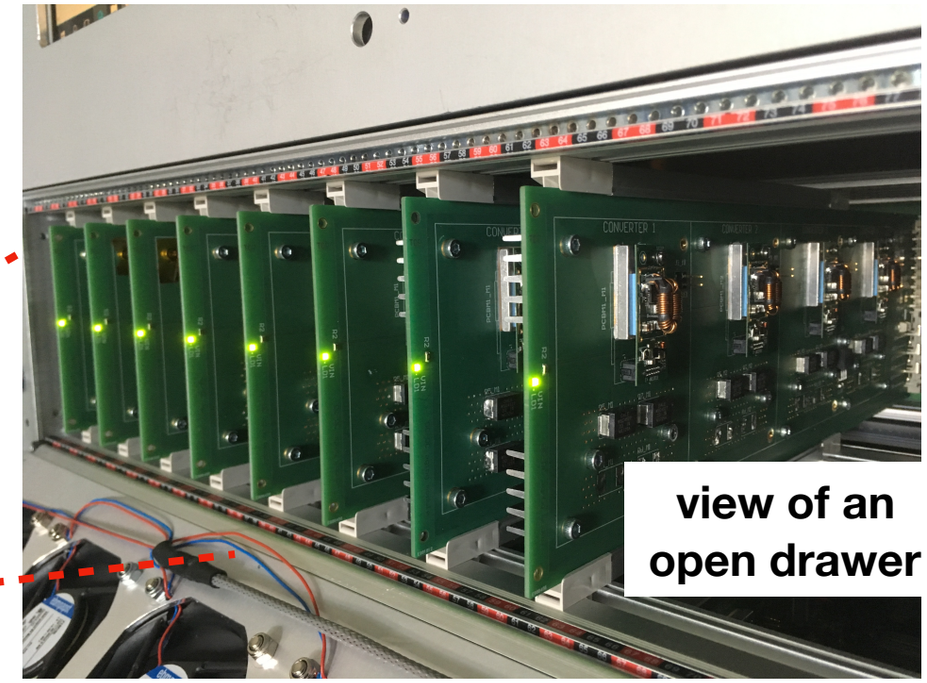

*Waveform of the V33Dr node when the capacitance has intermittent contacts to the PCB*

# Electrical stress?

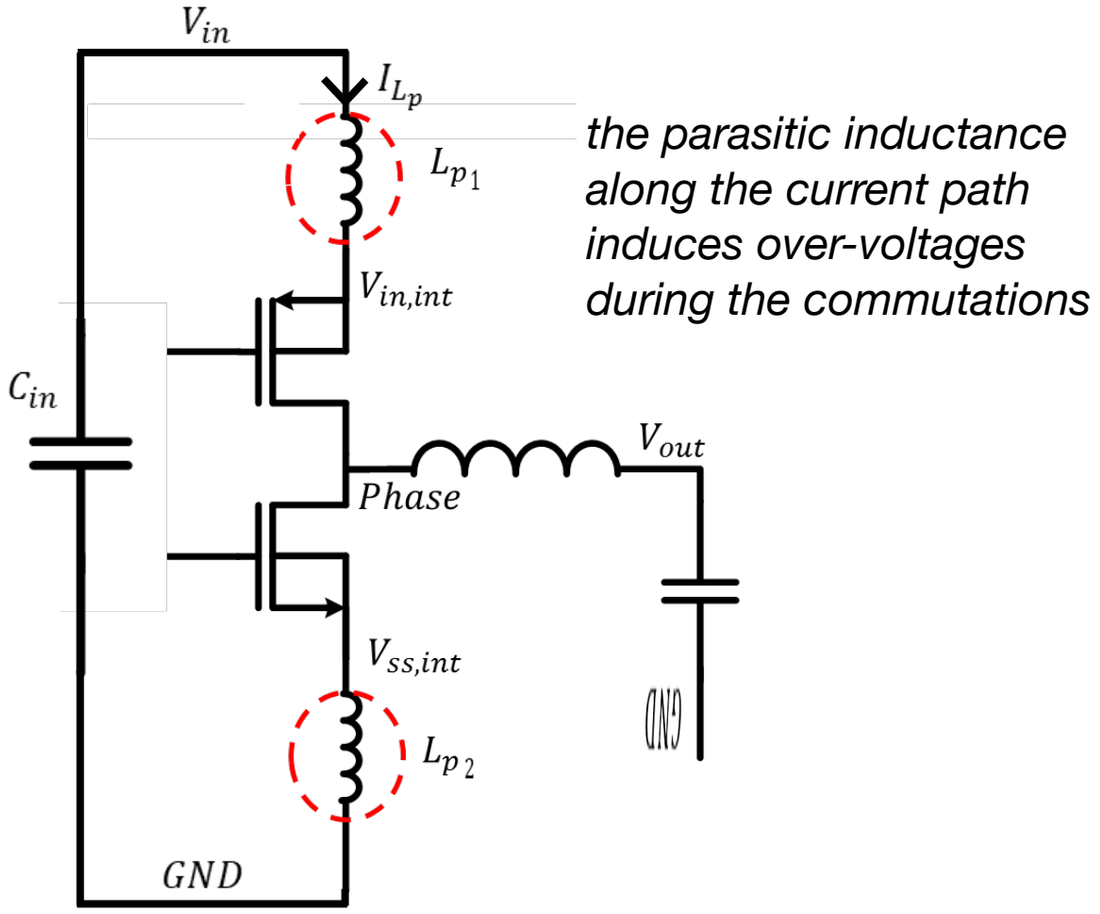
## Long-term ageing tests on 124 converters did not reveal problems with FEAST2 ASICs

3 drawers with 8x4 modules

“Crate96” system with 32x3 modules




view of an open drawer

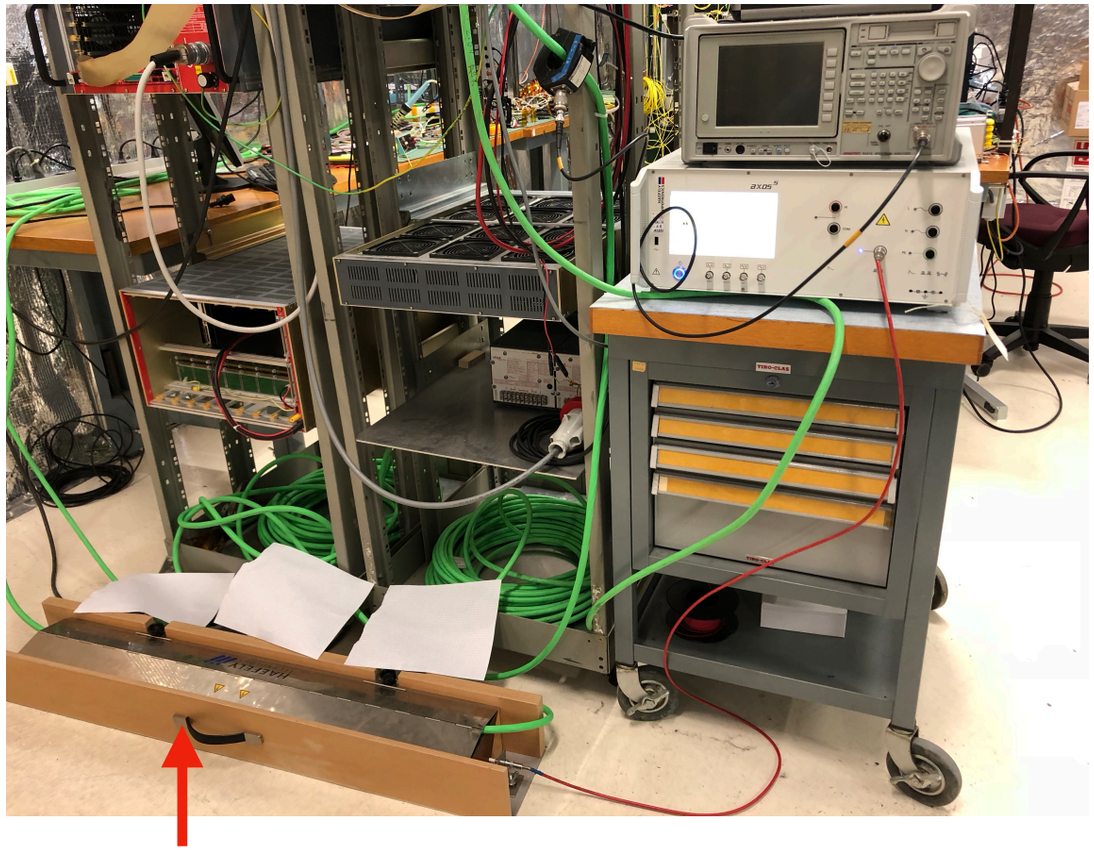



*the parasitic inductance along the current path induces over-voltages during the commutations*

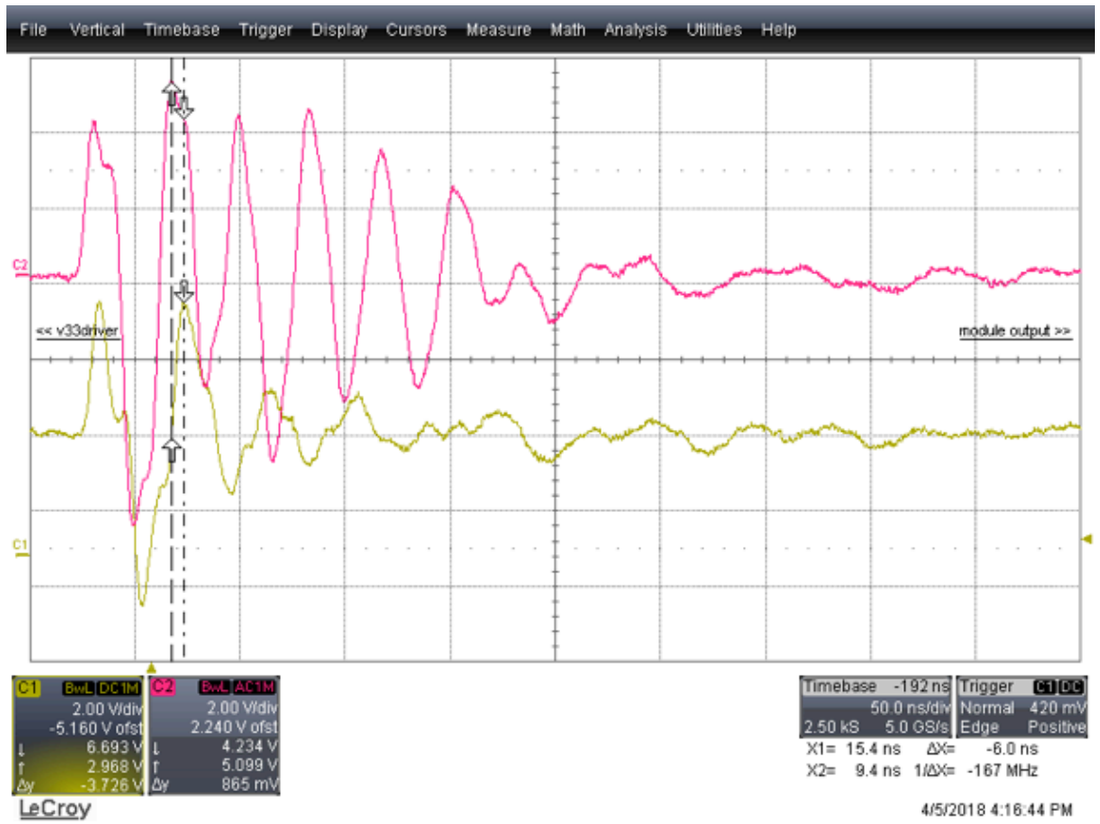
## EM noise?  Environmental conditions?

**Injection of EM noise by capacitive coupling to the input/output and signal lines. The converter appears to be very resilient**

Led by F. Szoncso and D. Valuch



*Capacitive high-frequency coupler used on the input bus line*




*AC-observation of the effect of a 3kV (!) pulse with 50ns duration on Vin and V33Dr. The peak is several V above the DC (V33Dr reaches 8V)!*

## EM noise? Environmental conditions?

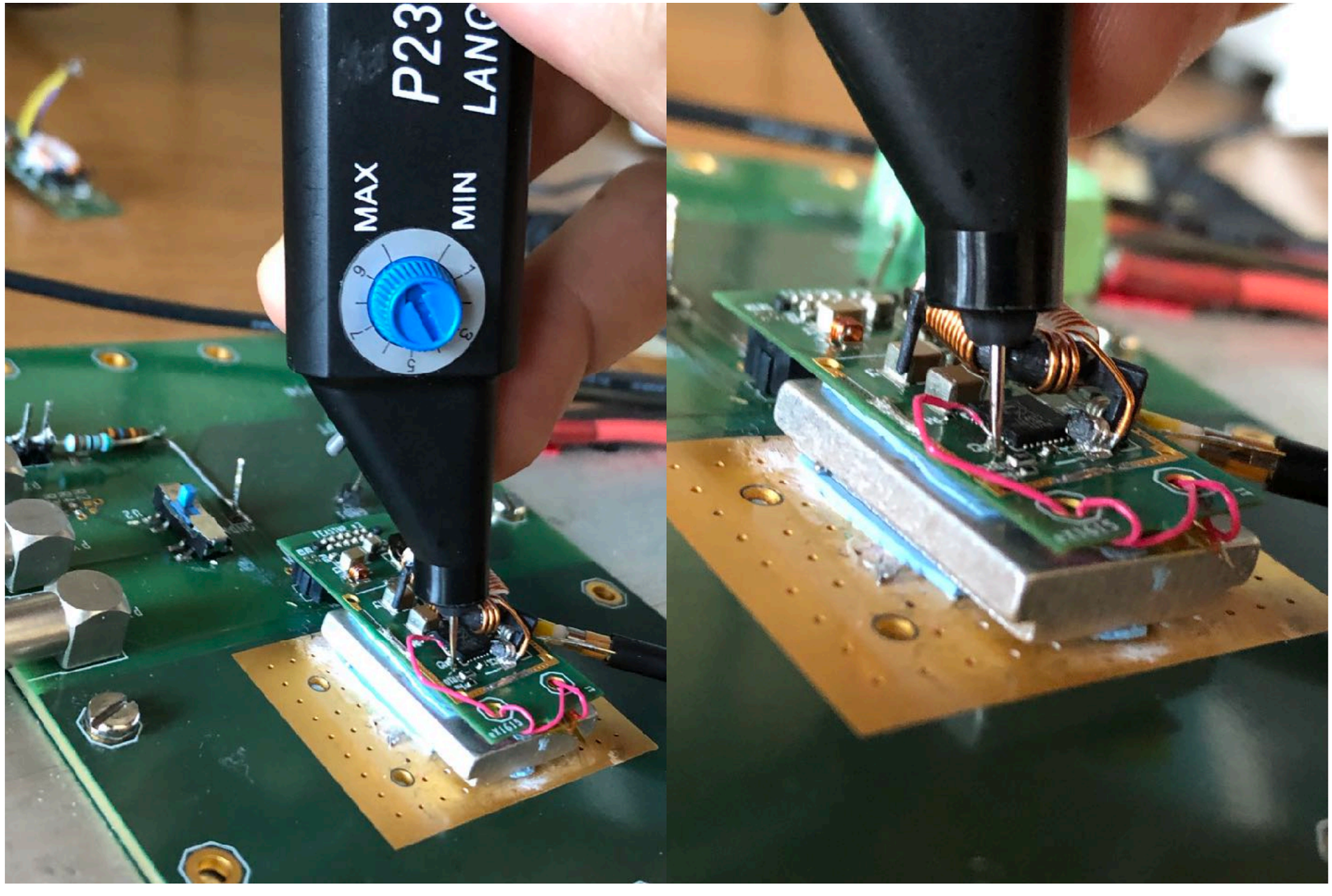
### High-frequency, large power RF noise injection could produce damage with different signature

Led by F. Szoncso and D. Valuch

*High frequency (GHz) and high power transient pulses are injected via an antenna in a special chamber in CERN Prévessin. At very large power, the ASIC can be damaged but the signature is different than in samples failing in CMS. Coupling is through the long enable line.*

## EM noise?  Environmental conditions?

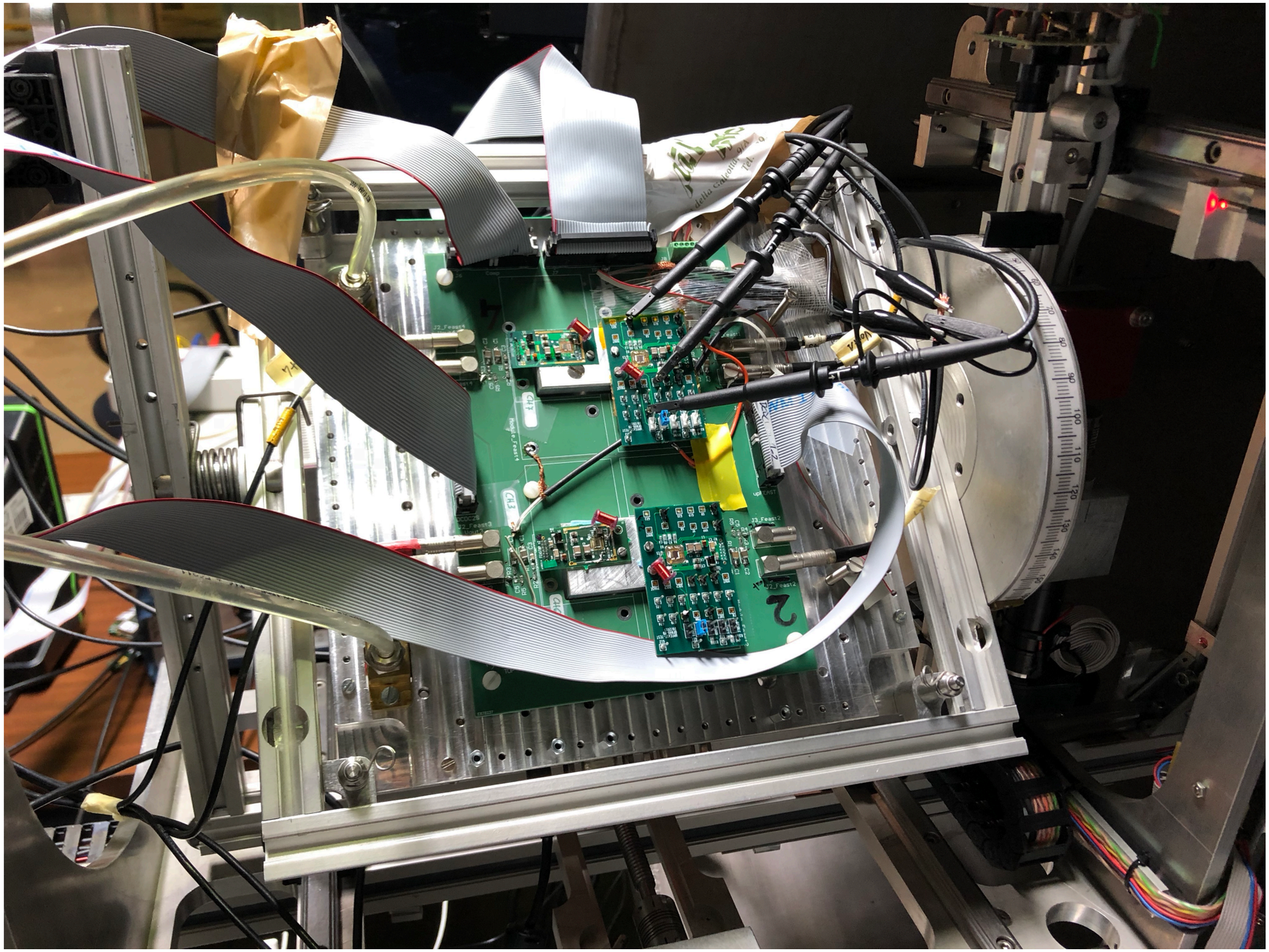
**Stress tests with an ESD gun (1.2kV pulses) could produce somewhat similar damage - but the energy injected needs to be really large**


*An ESD gun is used to inject a discharge to the different pins of the FEAST2 package.*
*To produce any damage, a visible spark has to be produced.*

## Radiation in ASIC?

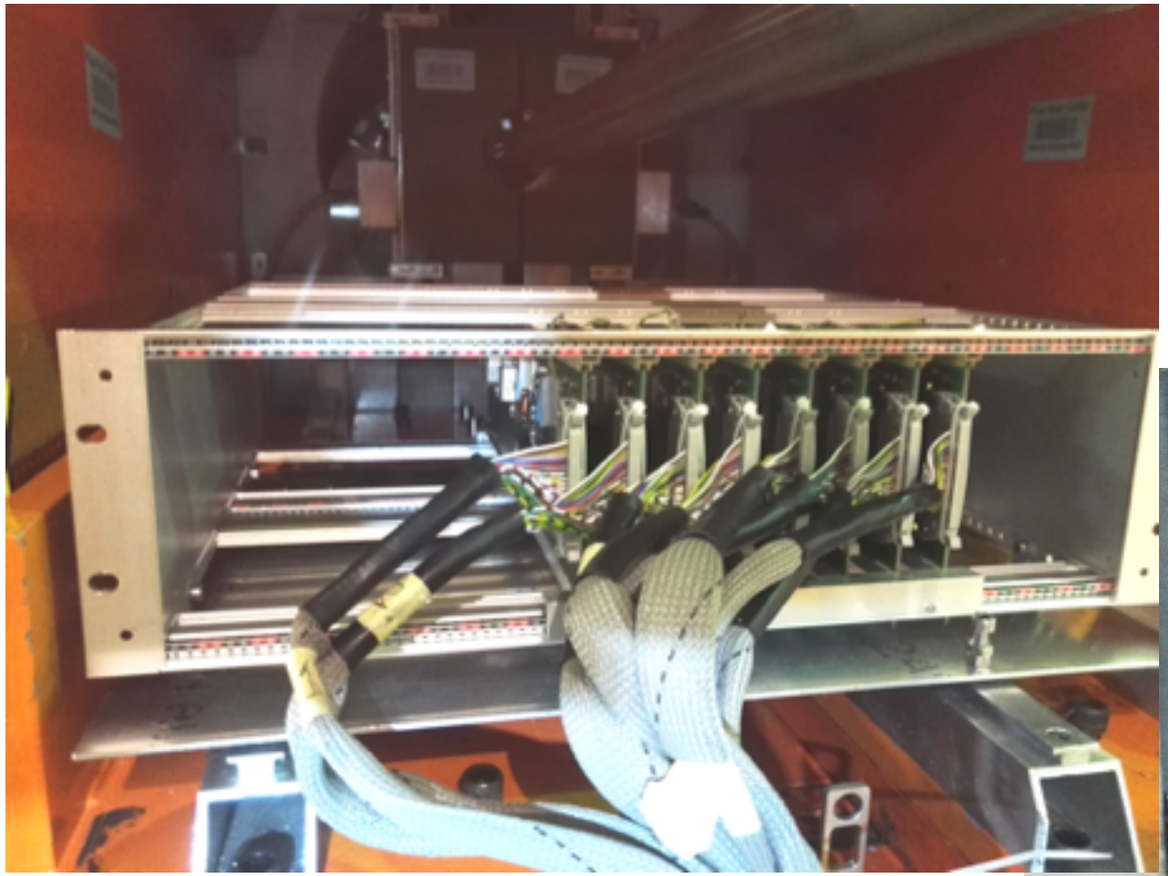
**SEE Heavy Ion irradiation on samples pre-exposed to X-rays, Protons and Neutrons did not show any sign of damage**

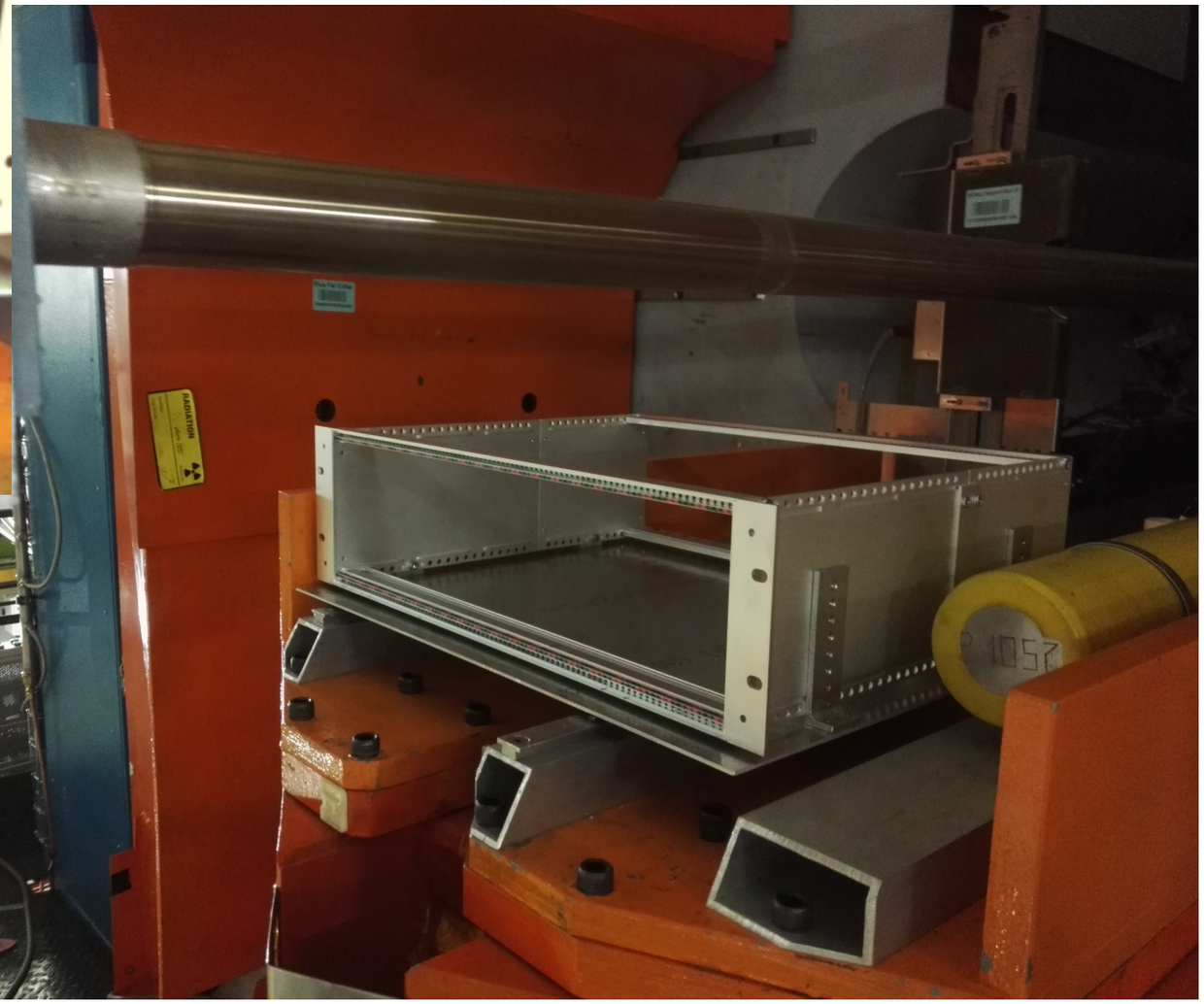


*4 modules prepared on a motherboard are placed inside the irradiation chamber where they will be exposed to a Heavy Ion beam. The FEAST2 chips were previously irradiated with X-rays, 230MeV protons or neutrons from a reactor.*

## Radiation in ASIC?  Environmental conditions?

**Exposure of 32 FEAST2 in the CMS Castor Table was meant to reproduce some of the environmental conditions (proximity to the beam line, EM environment, radiation environment)**






*32 sample DCDC modules, both FEASTMP and CMS modules, are exposed and constantly monitored in the CMS Castor Table during the 2018 run.*

**Radiation in ASIC?** **Environmental conditions?** **EM noise?**

**Two irradiation runs at the CERN IRRAD facility were instrumental in understanding the origin of the damage**

## Exposure of 32 FEAST2 at -25C at the CERN IRRAD facility

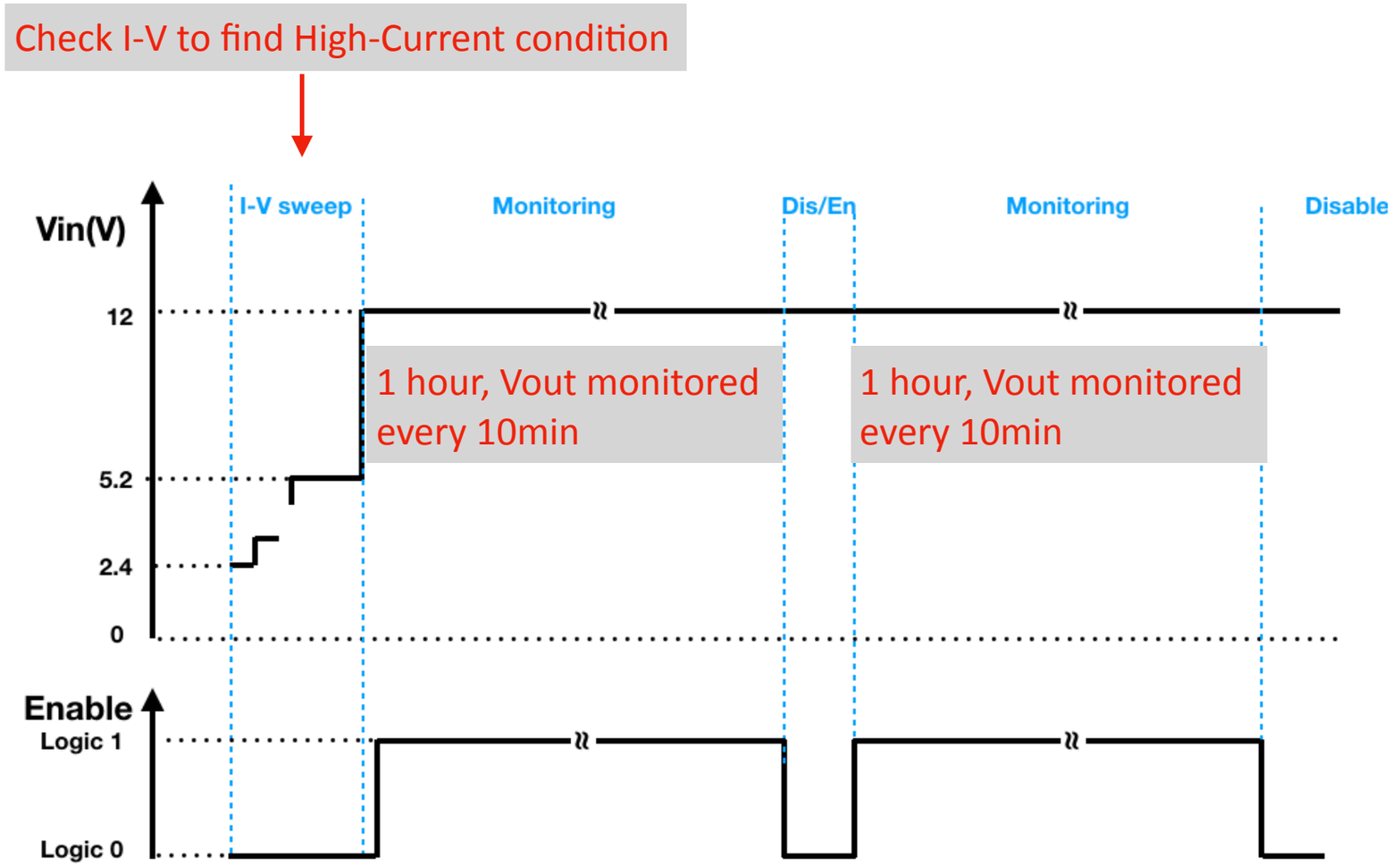
The facility run in a purposely modified configuration to expose the converters in a mixed field:

*MANY THANKS to the IRRAD TEAM!*

*32 samples, both FEASTMP and CMS modules, are exposed and constantly monitored in a cold box (-25C) in the CERN IRRAD facility (May 2018).*


*32 modules inside the cold box*

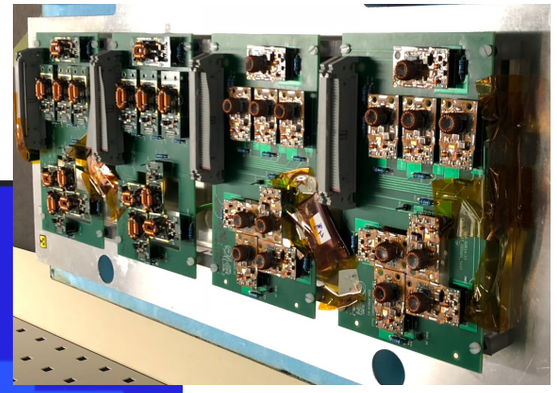
# A specific bias and control sequence was used during the exposure

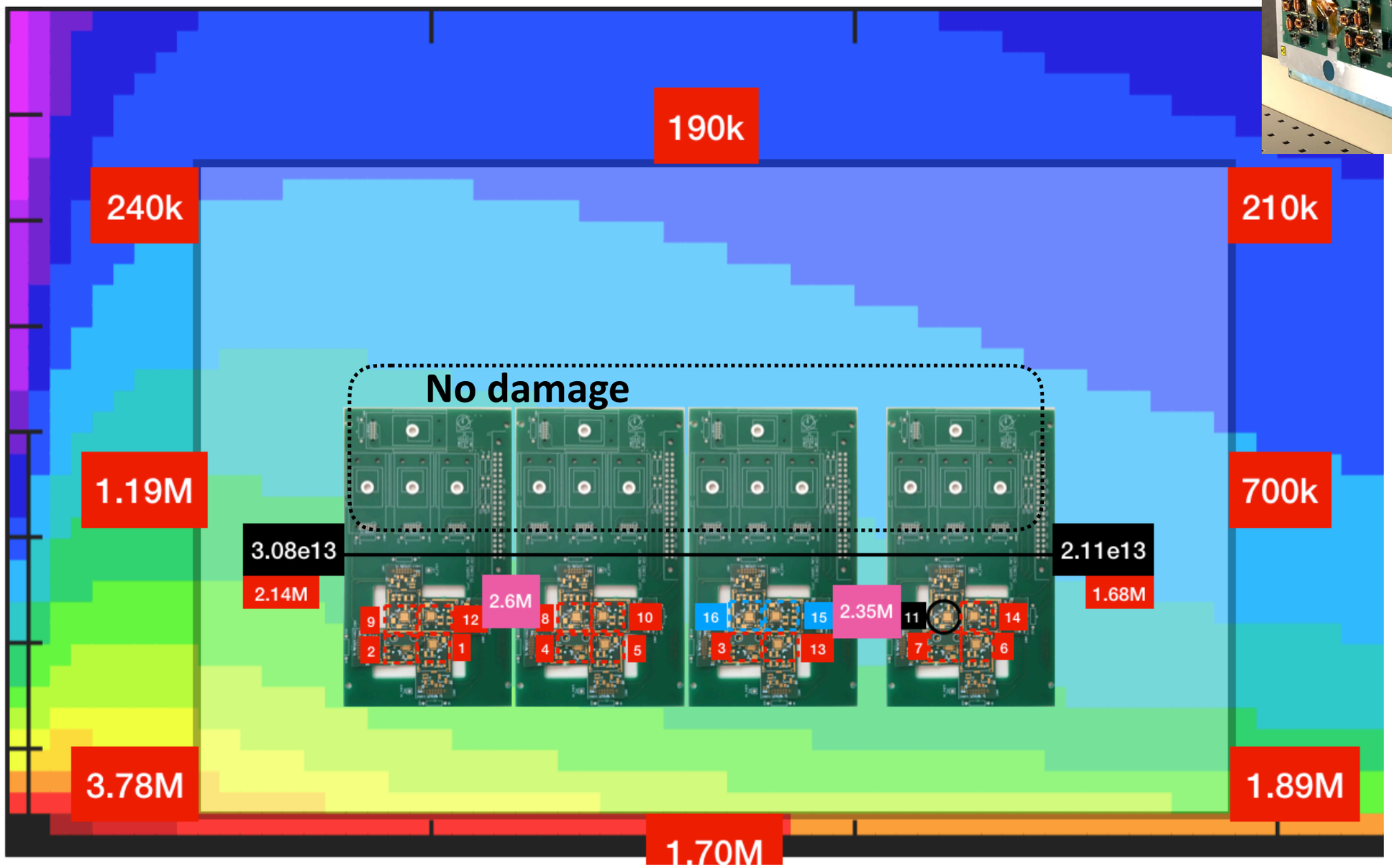



The full sequence lasts about 2 hours, with 97% of the time in “monitoring”

**The results powerfully revealed some important correlation:**

- **Between the damage and the integrated flux**
  - The first damage occurs after 9 days, then several samples per day
  - Only samples closer to the beam are damaged
  - Samples are damaged also after the end of the exposure
- **Between the occurrence of the damage and the disable-enable sequence**
  - Also true for the “High-Current”

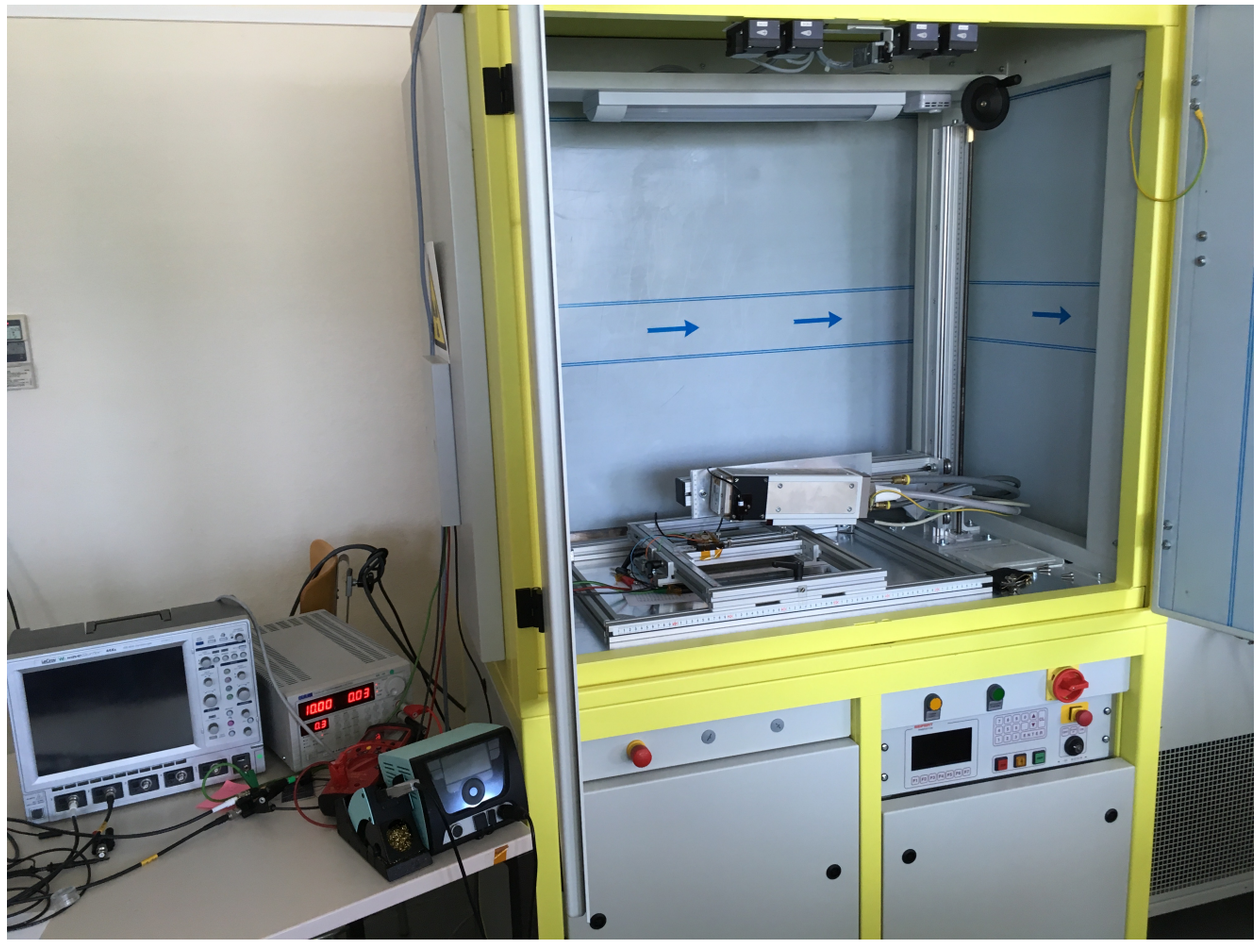





**Red** = High-Current damage occurred during exposure
**Blue** = High-Current damage occurred after exposure
**Black** = failure

**X-ray irradiation using the same enable/disable cycle as in IRRAD, and monitoring the current under UVLO thresholds, it was eventually possible to produce the same damage!**

**Now we had a tool to study the mechanism in detail!**



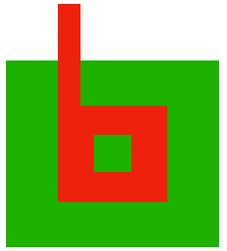
*X-ray machine of the EP-ESE group*

# The crime reconstruction

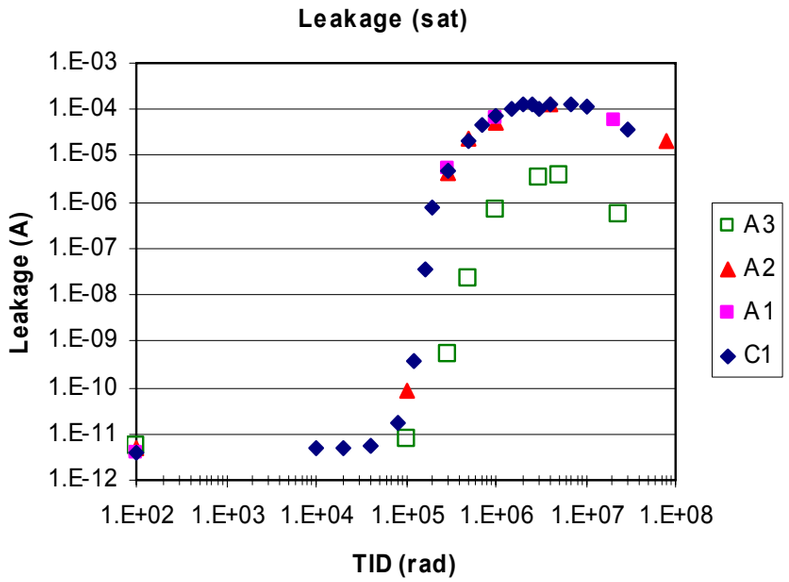
# Radiation tests on the I3T80 nLDMOS transistor in 2008 revealed the impossibility to use Enclosed Layout Transistors (ELT): TID-induced leakage could not be avoided!

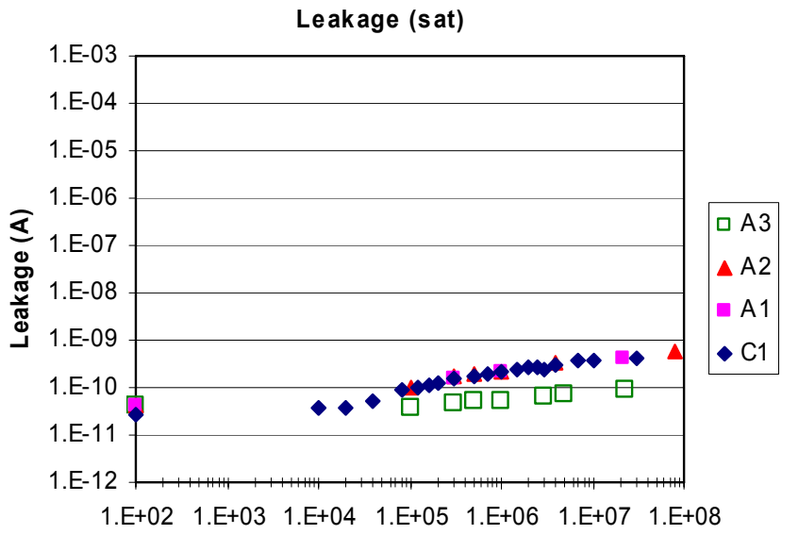
## Linear layout

## ELT

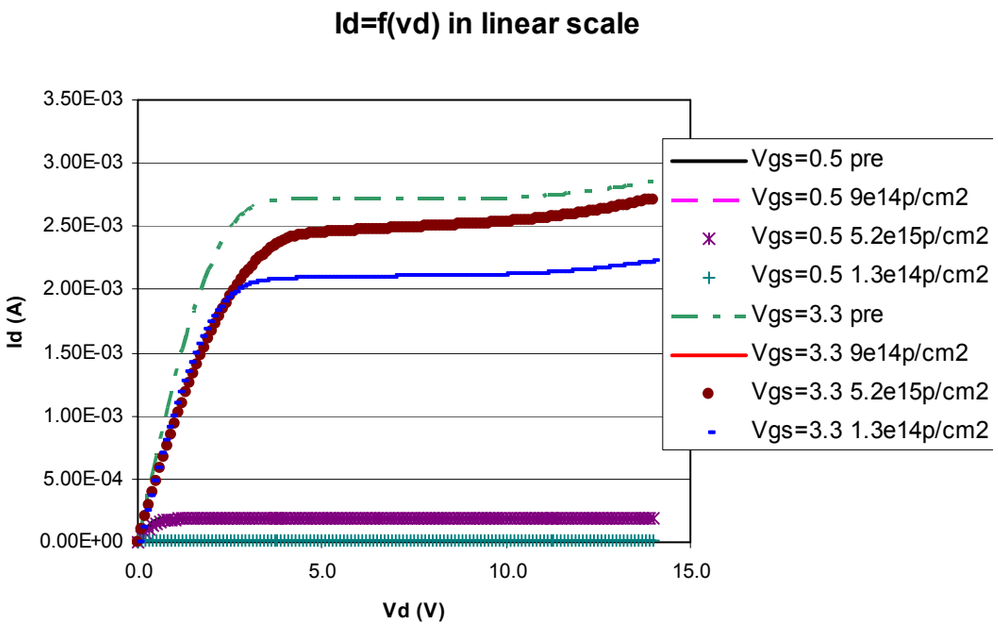


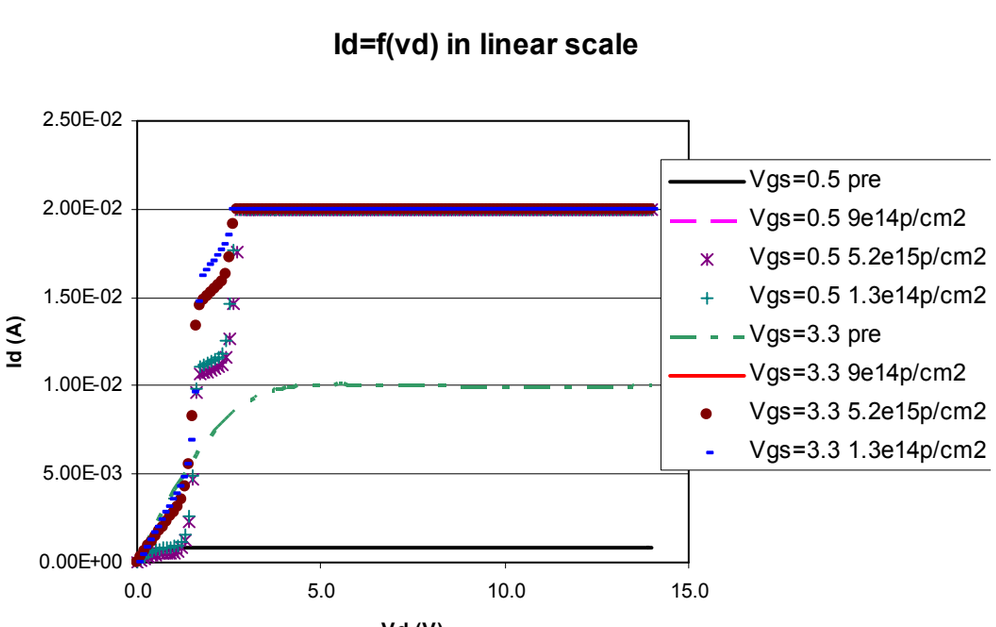
## TID



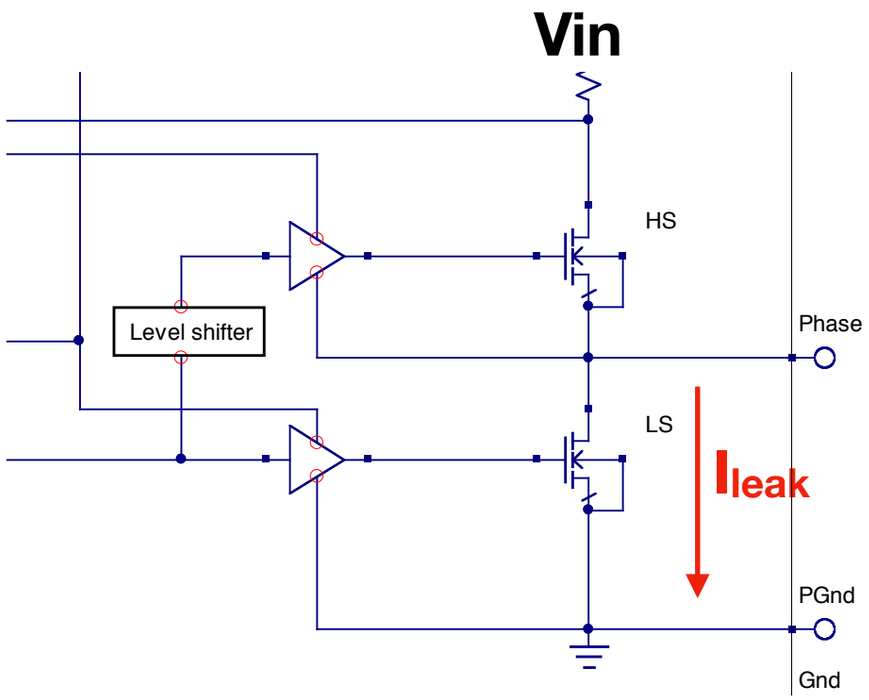



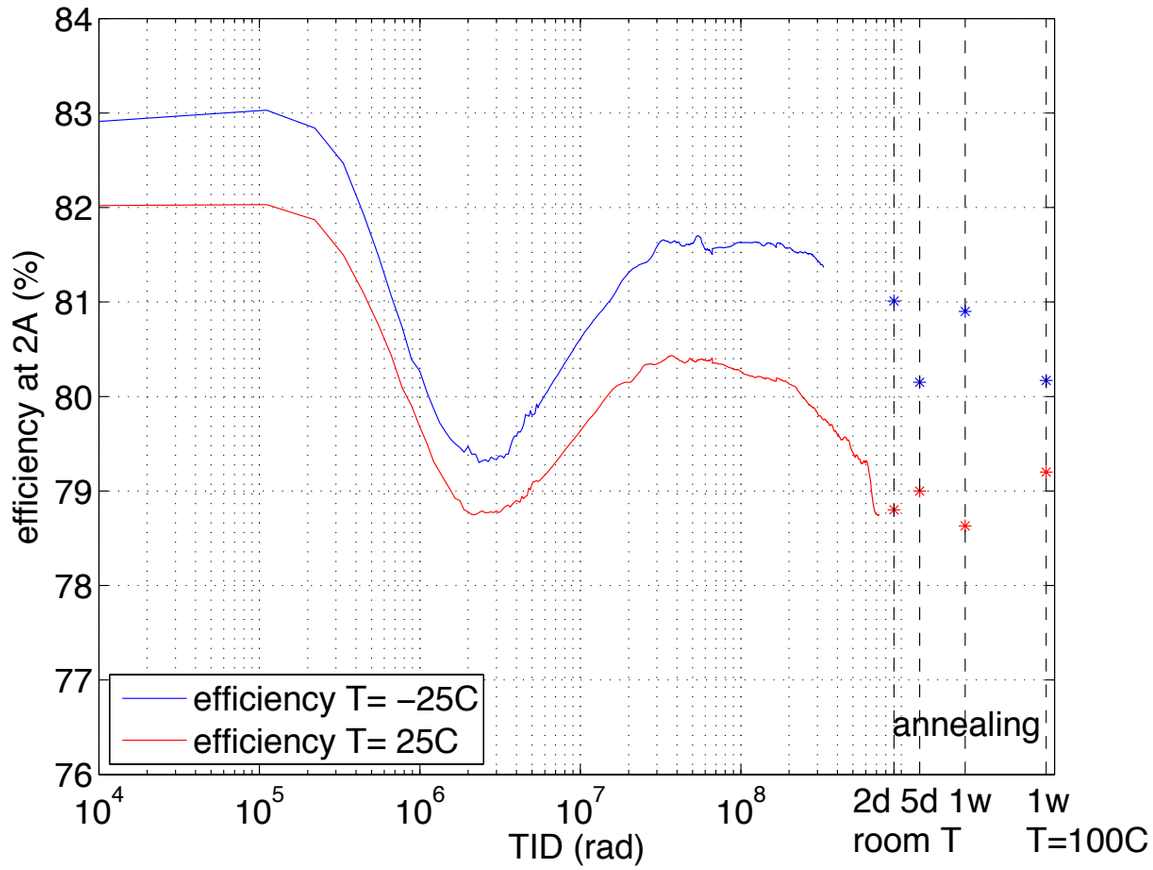

## Displacement Damage



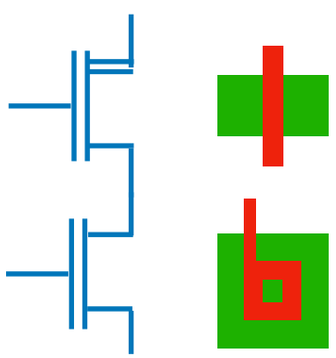



**The leakage current in the nLDMOS transistors, used for the power train, induces an acceptable decrease in efficiency.**




**Elsewhere in the circuit, the leakage path is “cut” by adding core ELT transistors in series**



**Linear layout nLDMOS**

**ELT core nMOS**

**The qualification testing strategy of FEAST was based on:**

- **the irradiation of the device to the maximum radiation levels**
- **the verification on-line that the device was always functional (except for neutron tests, when the verification was done after irradiation)**
- **periodic and/or final full characterisation of the main electrical parameters: efficiency, line and load regulation, thresholds (UVLO, enable, OCP, OTP)**

✓ **X-rays for TID up to 700Mrad**

✓ **Heavy Ions for SEEs**

✓ **Pulsed laser test for SEEs**

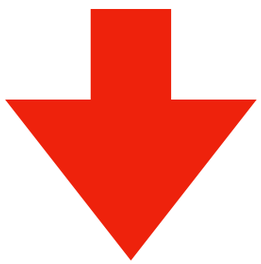
✓ **Neutrons from a reactor for displacement damage**

✓ **230MeV protons for SEEs (+ TID + DD)**

**Somewhere else, in another continent, the TBM chip for the CMS pixel system was being designed**

**During a late and quick addition of functionality, logic unprotected from SEUs was integrated in the final chip**

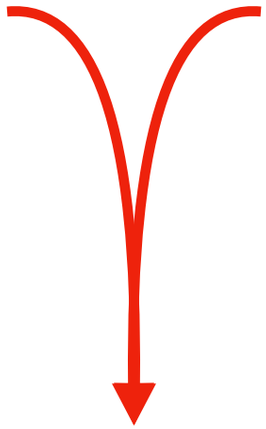
**A reset command was not implemented**



**In a severe radiation environment the correct functionality is frequently corrupted, and a power cycle is needed to re-initialise the chip**

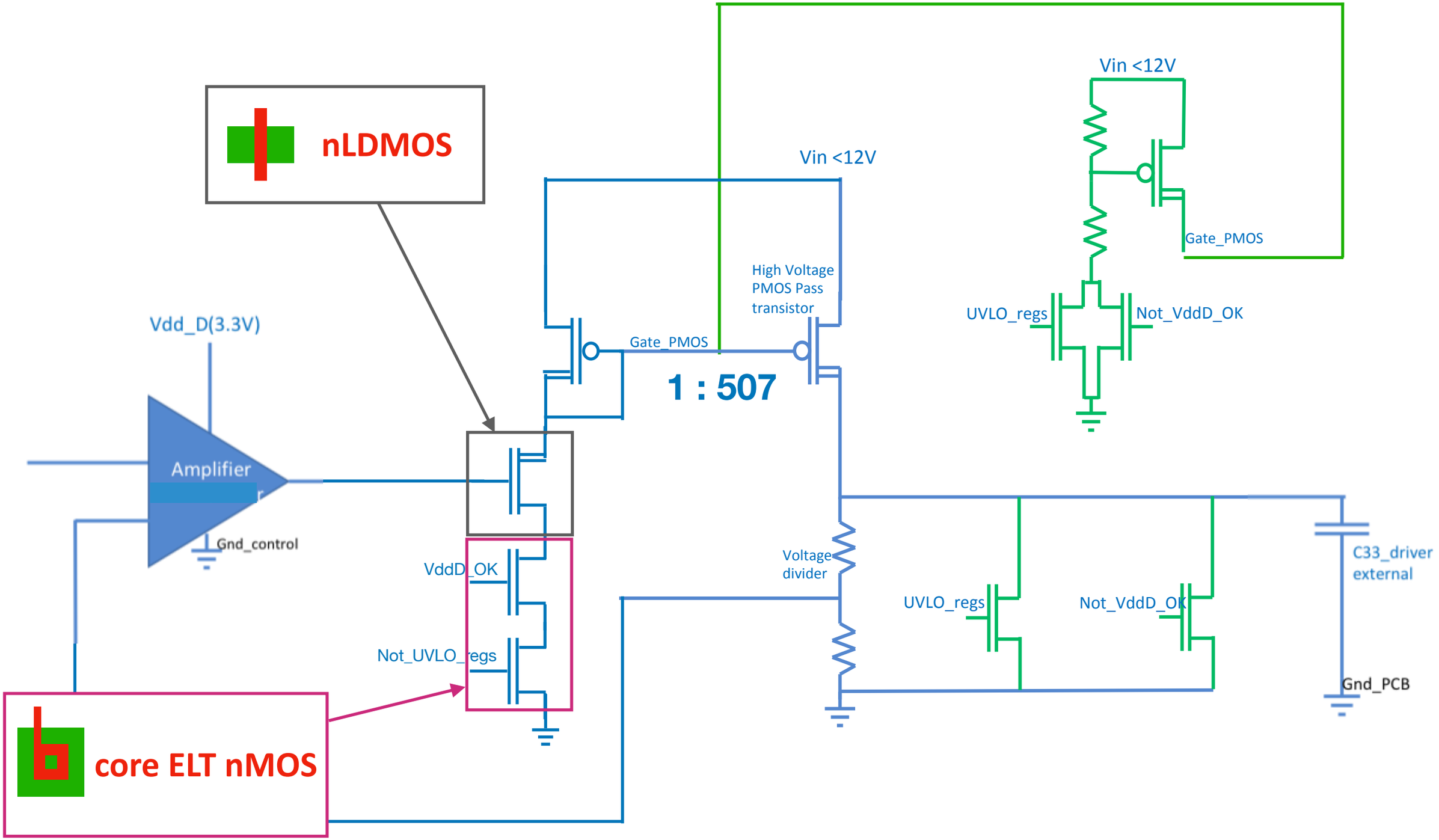
**Potentially “leaking” nLDMOS in FEAST**

**Unprotected logic and no reset in TBM**



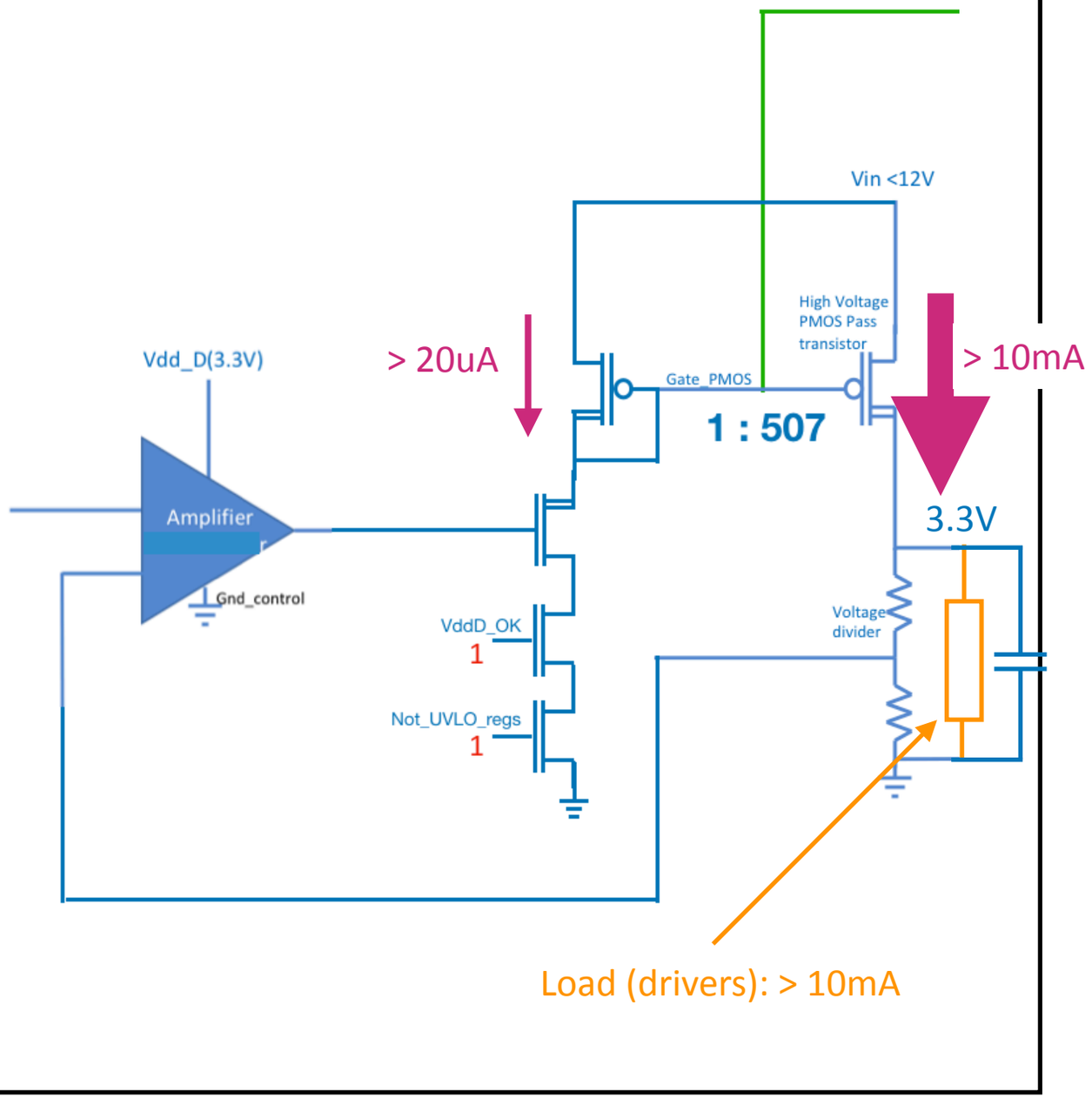
**Failure of FEAST2 in the CMS pixel system during the 2017 run**

**The problem is localised in the linear regulator (V33Dr) that provides the required current to the drivers of the power transistors (HS and LS)**

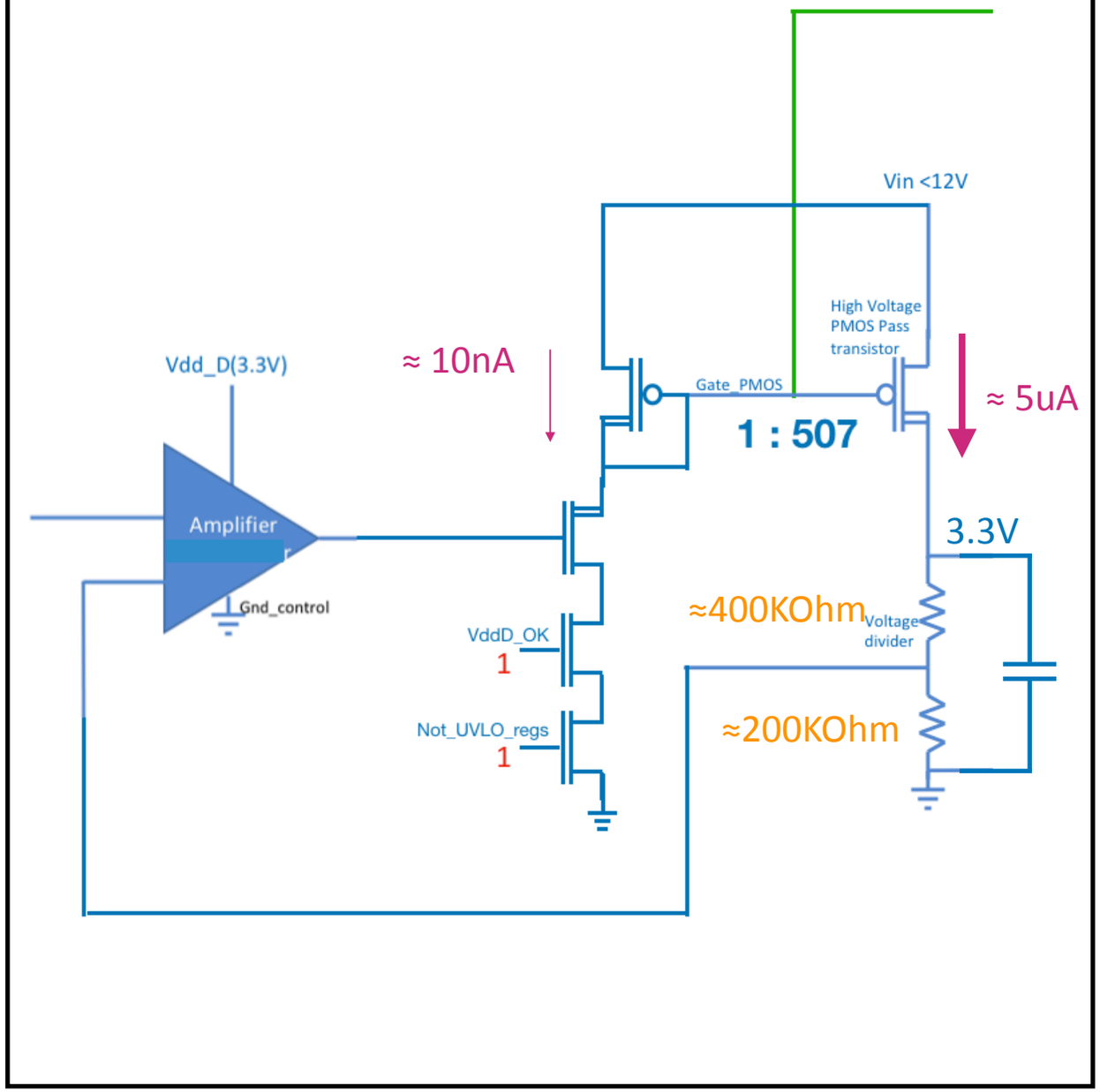


# These are the conditions when FEAST2 is “enabled” or “disabled”

## “enabled”

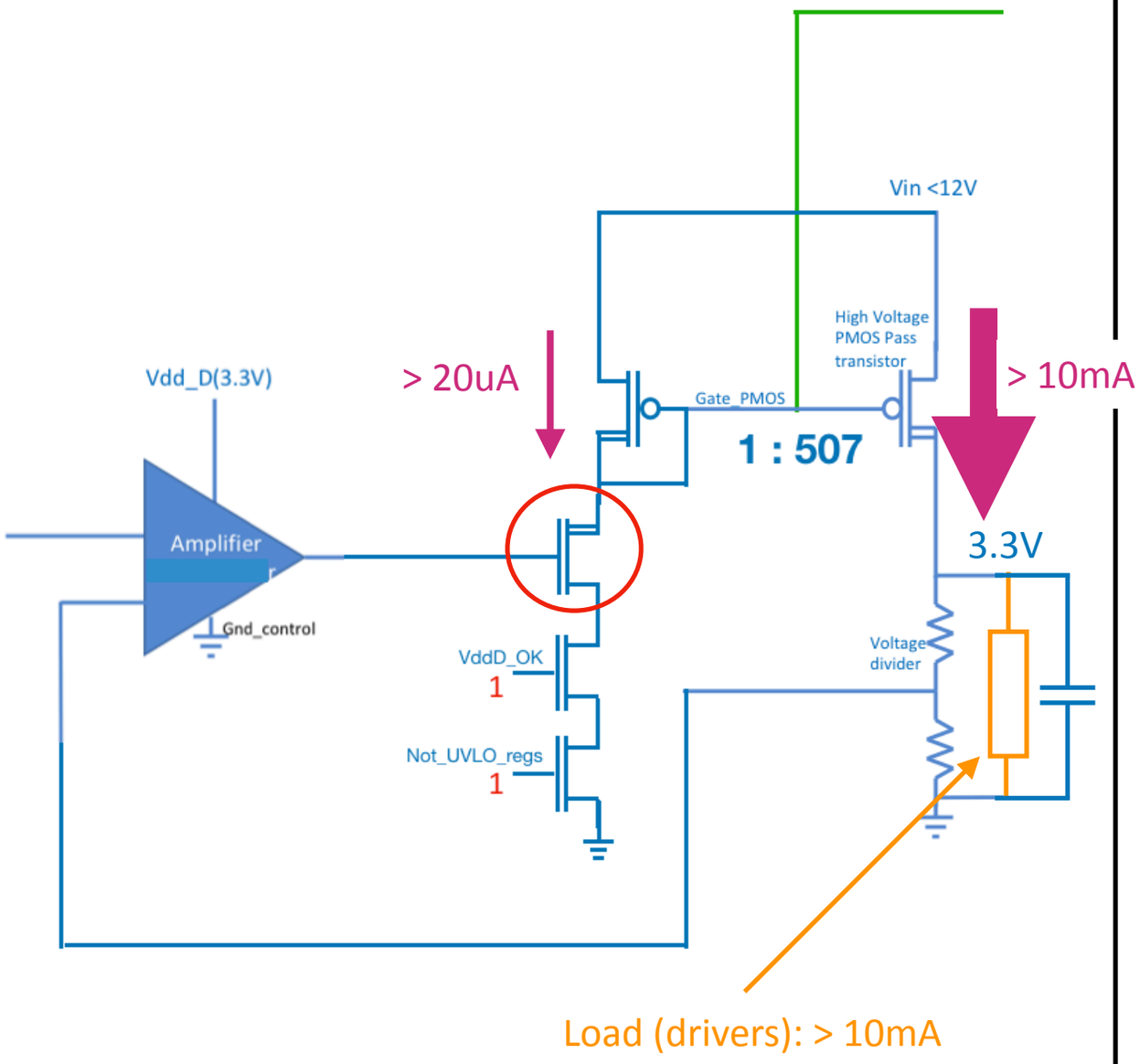



## “disabled”

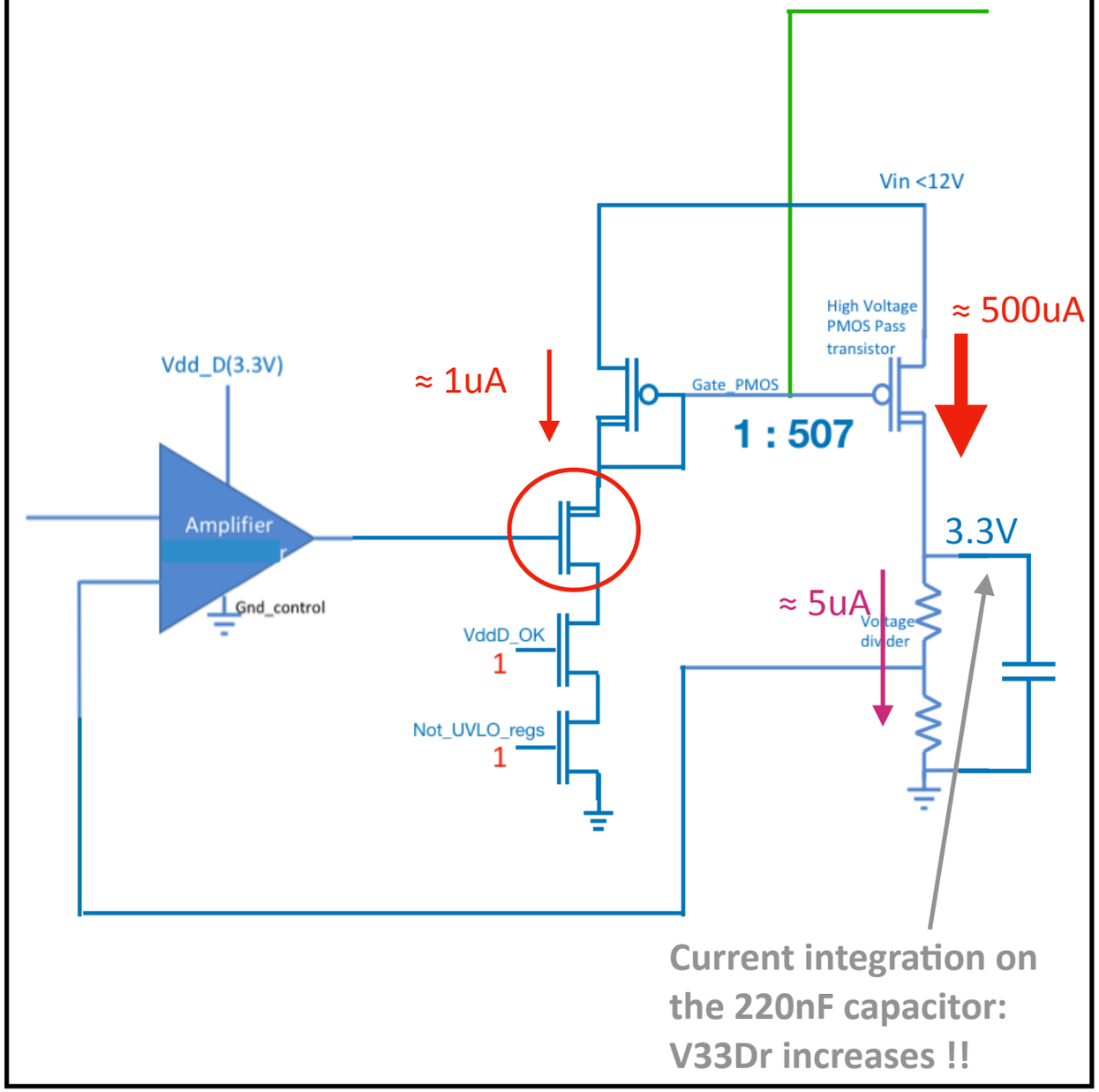


**In the presence of a large TID-induced leakage in the nLDMOS, consequences appear ONLY when FEAST2 is disabled (no load for the V33Dr regulator)**

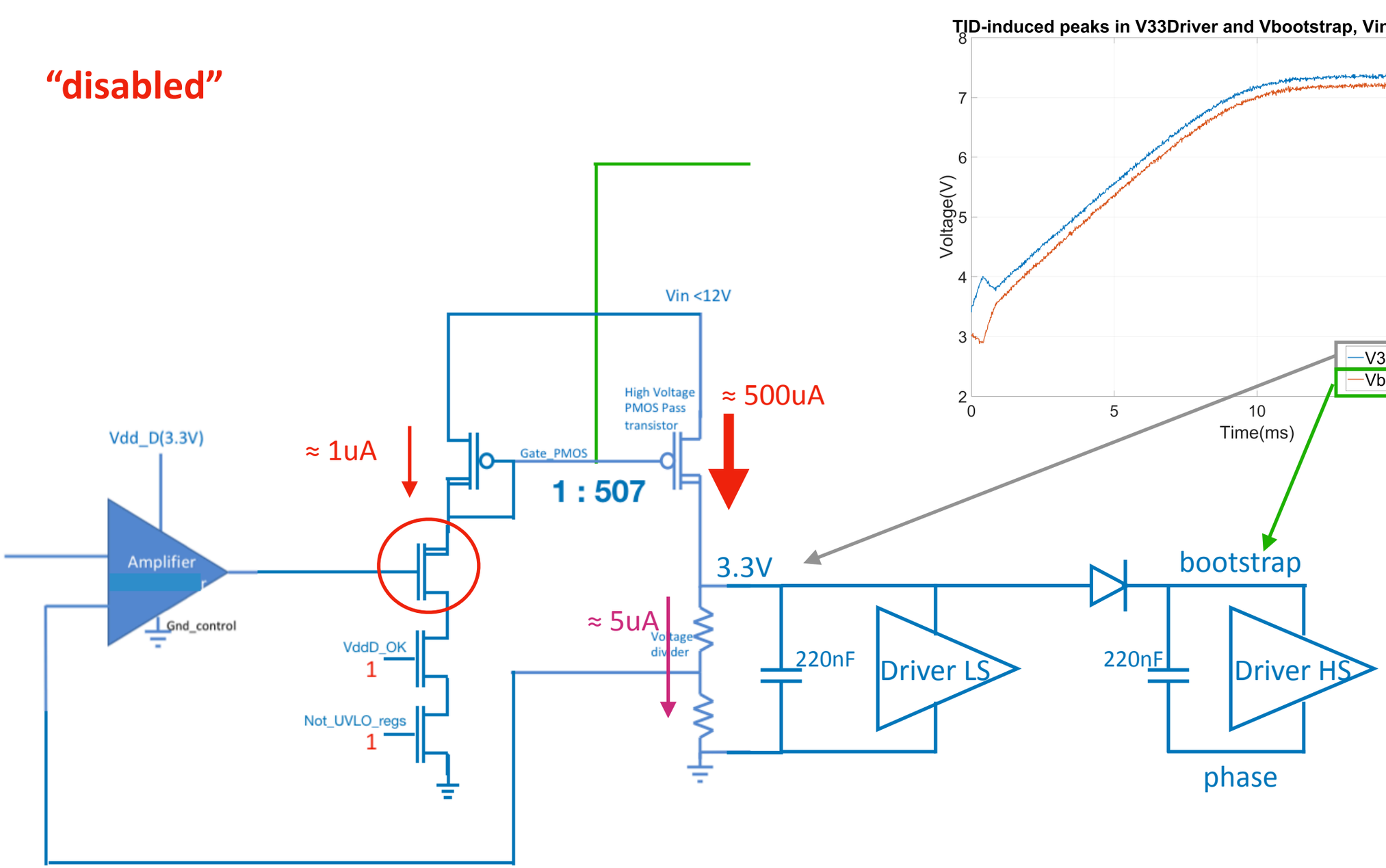
## “enabled”




## “disabled”

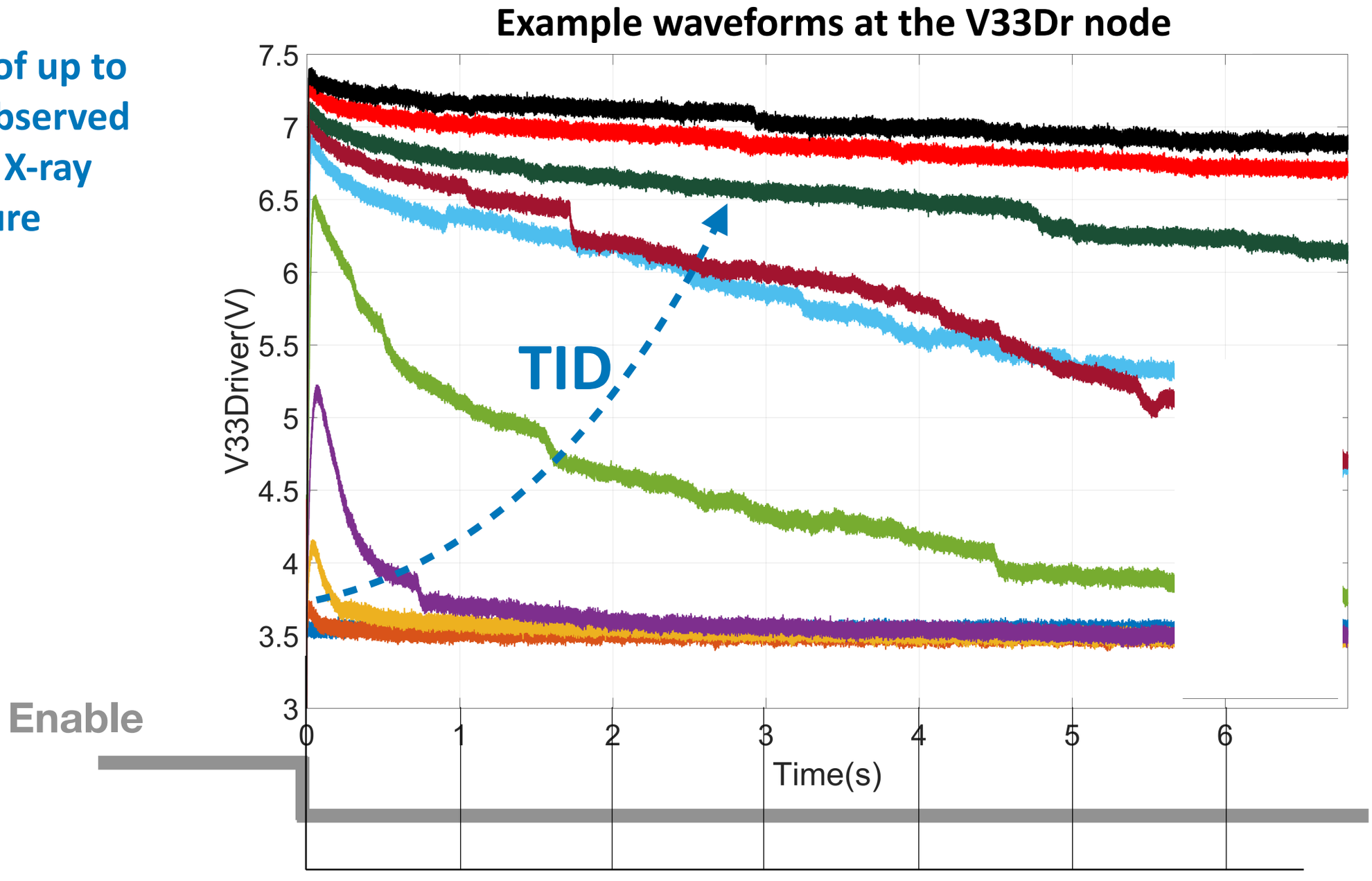


# The integration of the current on the two 220nF capacitors has eventually been observed experimentally in June 2018 on samples exposed to TID at our X-ray facility

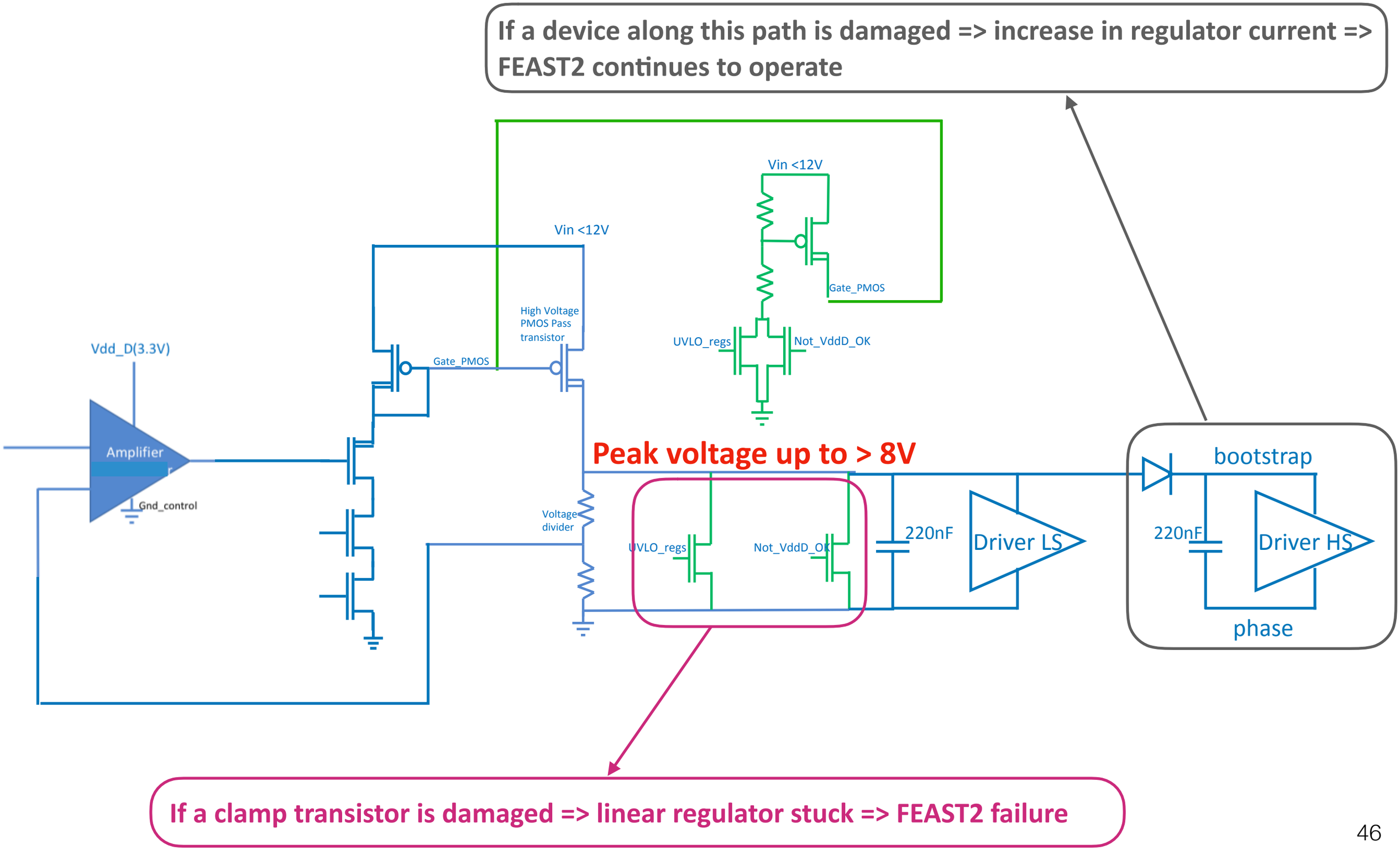


**We observed a “voltage peak” on the V33Dr node when FEAST2 is disabled during X-ray exposures. The voltage peak increases with TID**

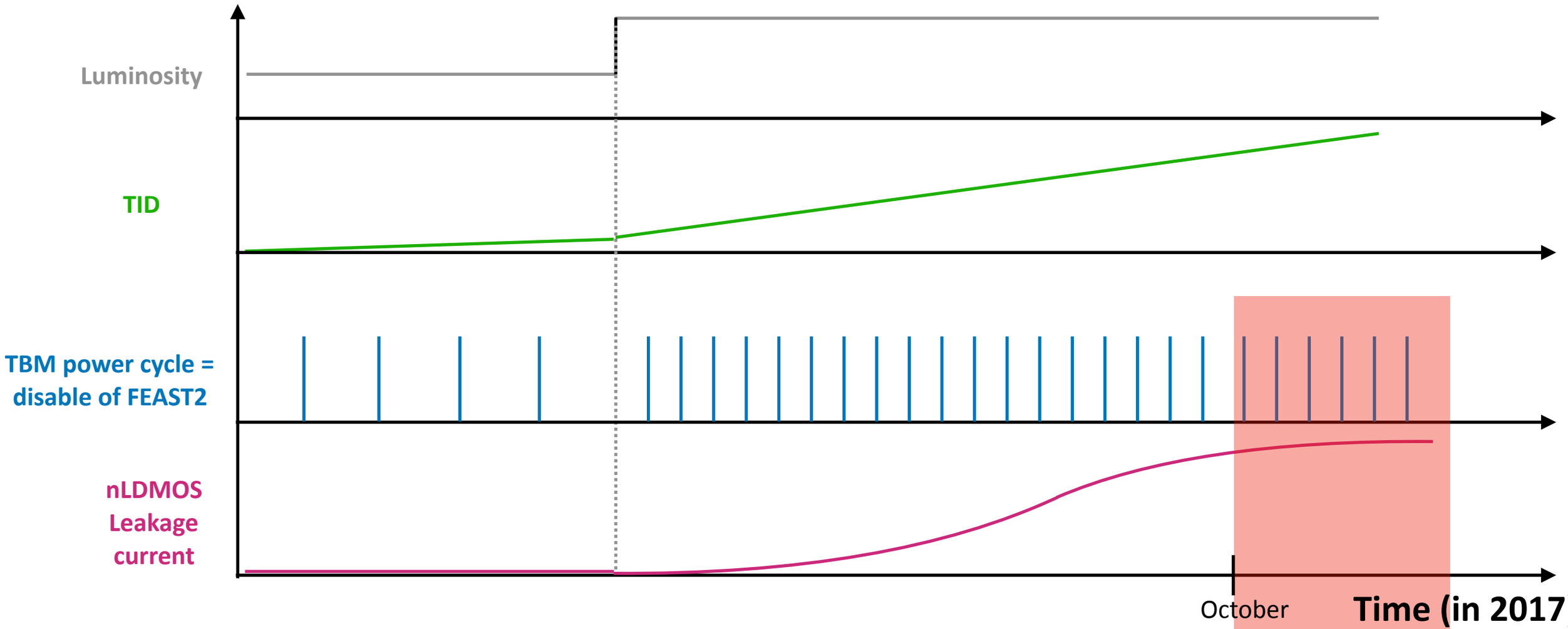
**Peaks of up to 8.5V observed during X-ray exposure**



**The voltage at the V33Dr node goes well beyond the nominal maximum of 3.3V+10%.**
**This voltage stress might end up damaging a device. We have observed 2 damage mechanisms, and Failure Analysis with emission microscopy and OBIRCH have confirmed the current paths.**



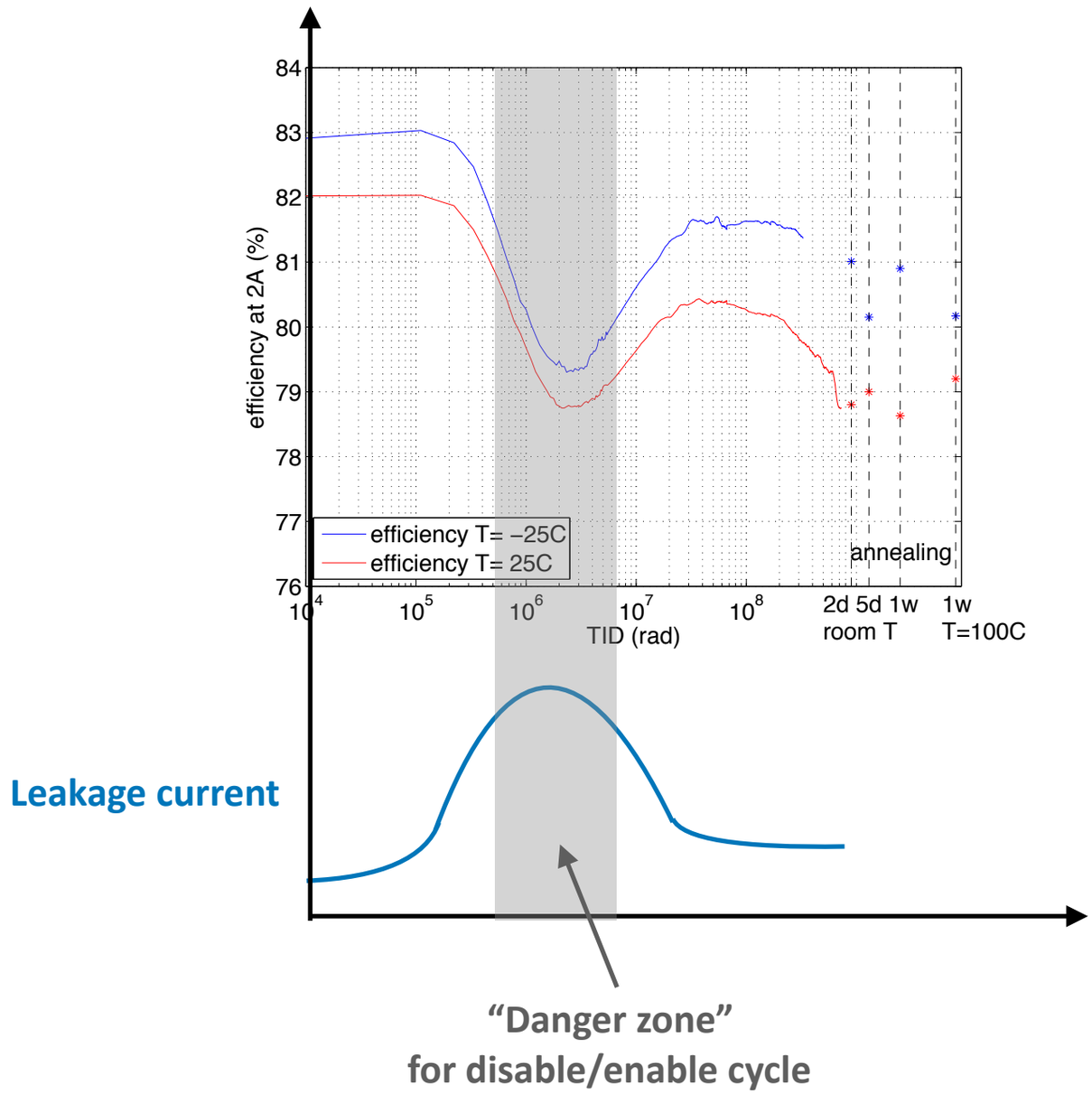
# A graphical representation of the narrative



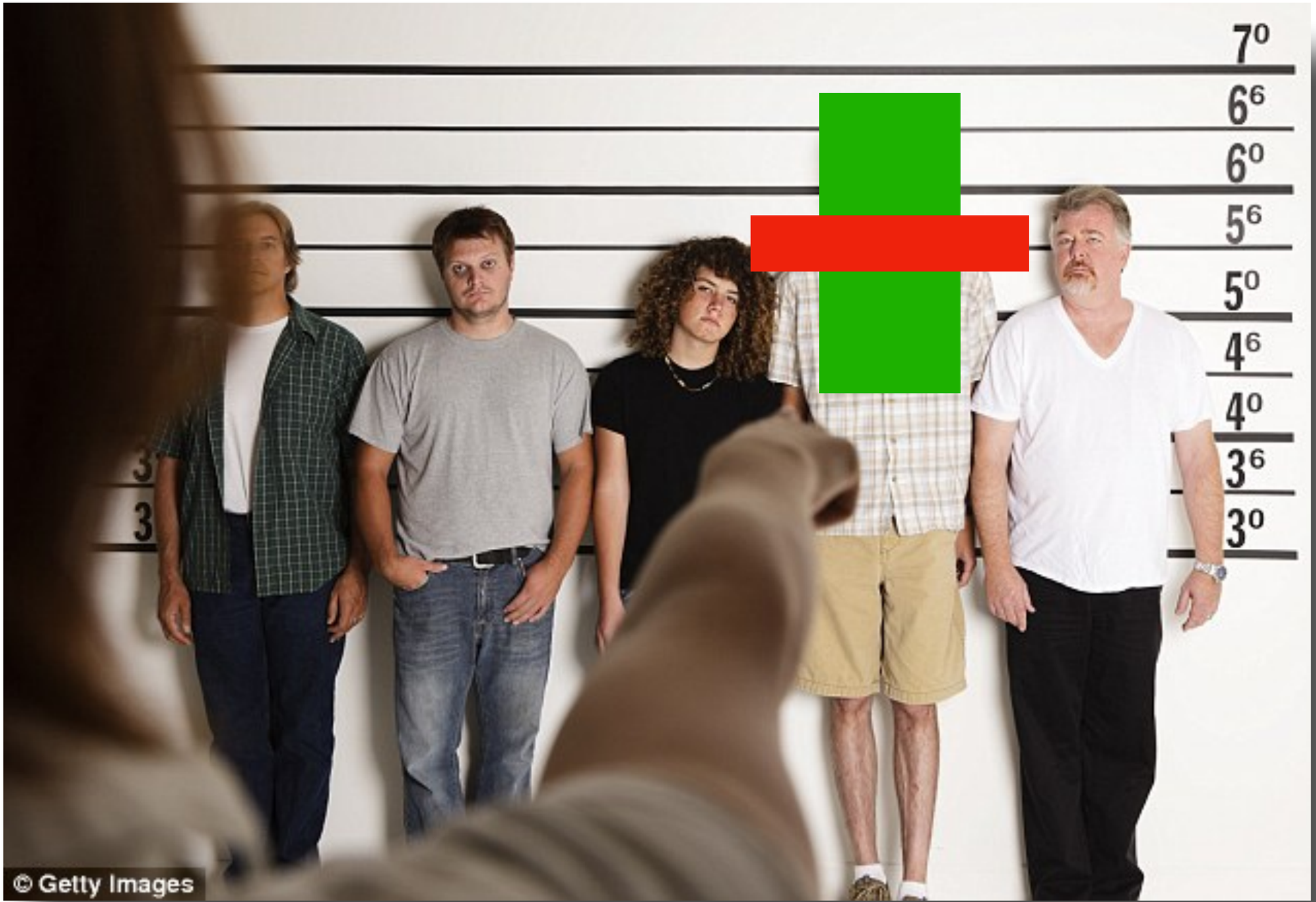

TBM requires a power cycle
=> FEAST2 is disabled while the leakage is large
=> peak voltage at V33Dr
=> damage

## This model for the damage explains why the problem was not observed during the radiation qualification of the FEAST2 ASIC

1. To produce the damage, it is necessary to perform disable/enable cycles at the time when the TID-induced leakage is large
2. To observe the signature of the damage, in the vast majority of the cases (High-current), it is necessary to measure the current consumption below UVLO thresholds



# The perpetrator

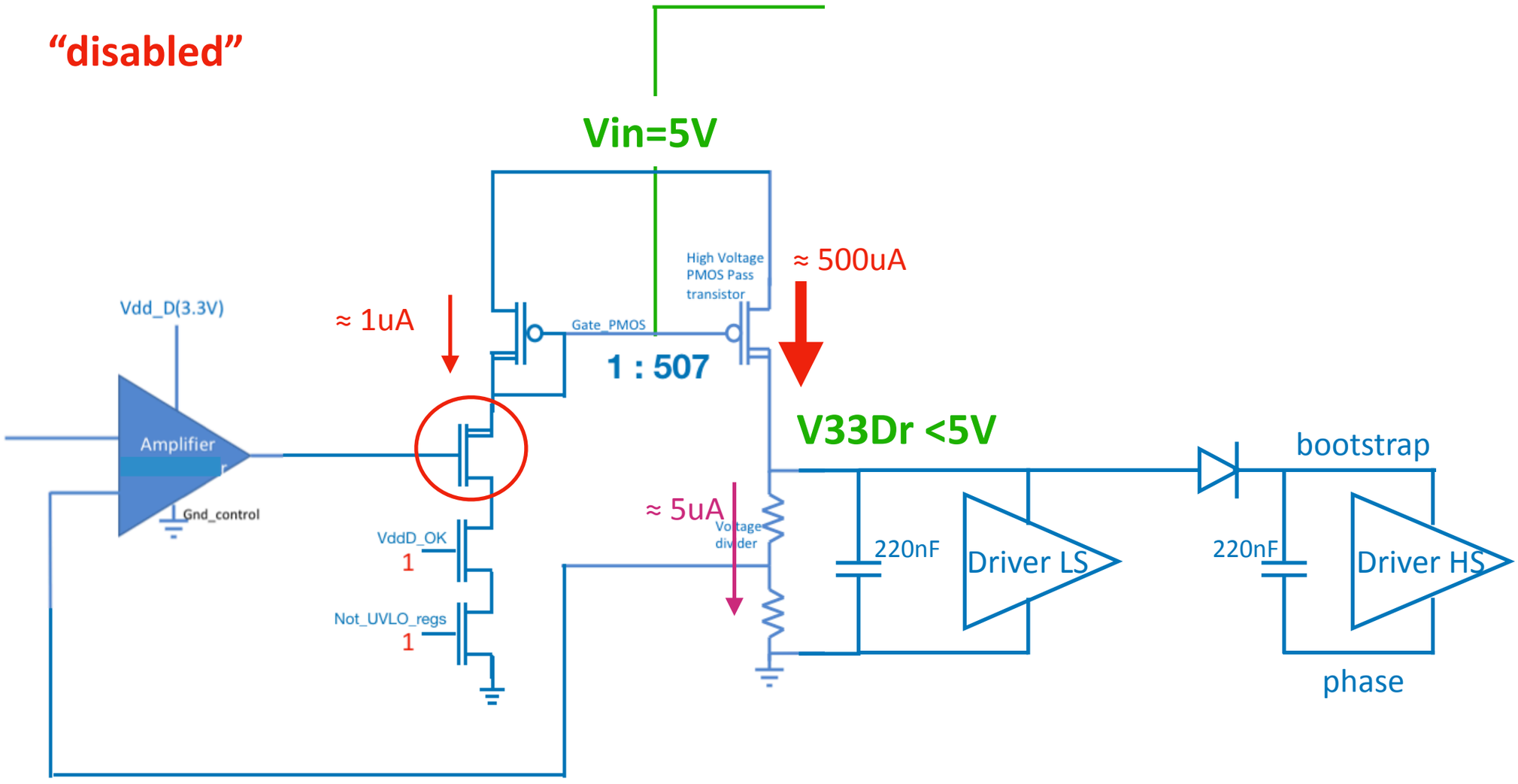


# Patches and long-term solutions

## Patch 1 for FEAST2.1 (only for environments with TID > 500krad):

**The voltage peak can get close to Vin, but not higher**

**Disable the converter at lower Vin**




**In case of a power cycle (Vin down to 0V), the converter is disabled by the UVLO at about 4.4V**

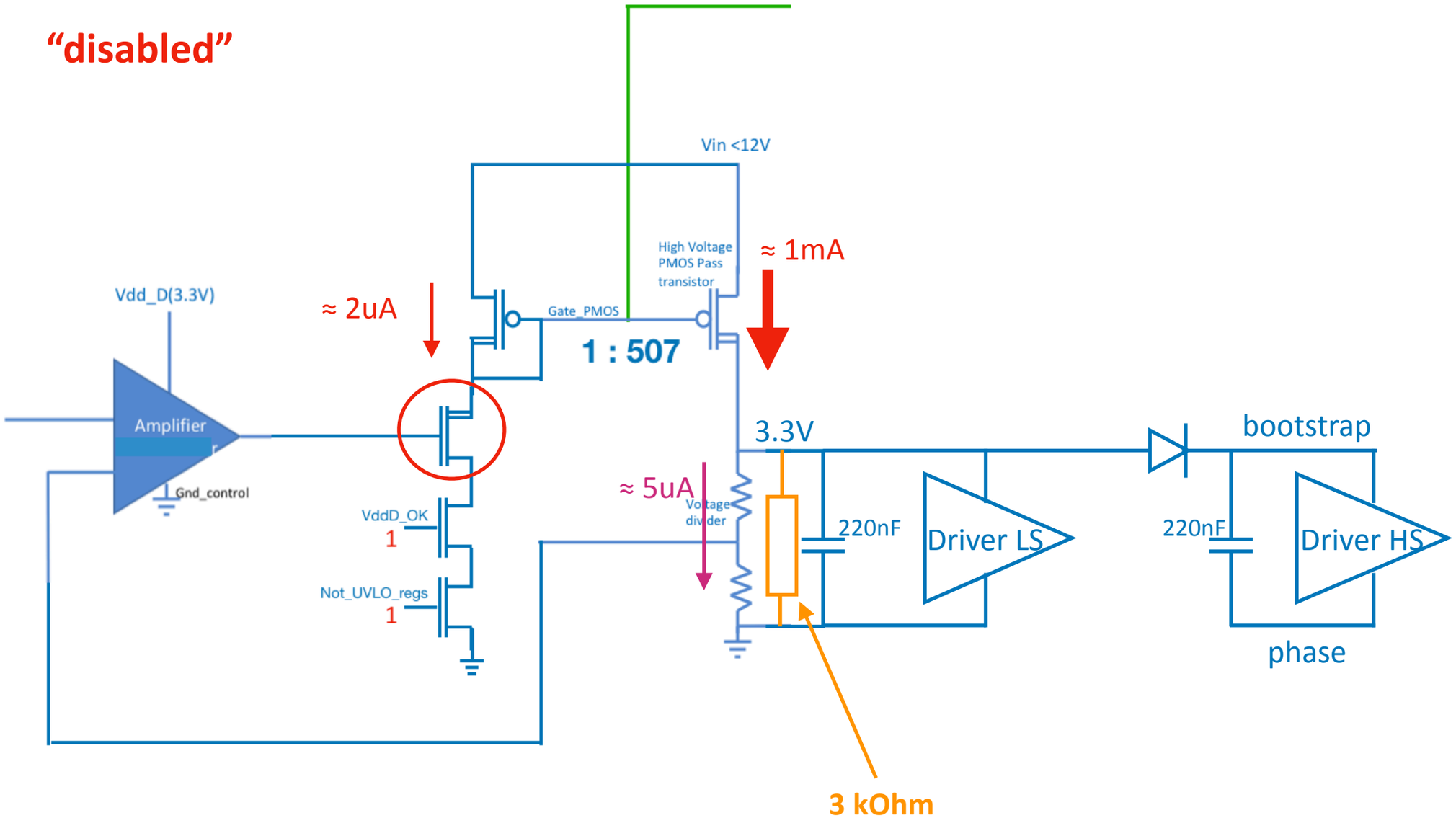
**This strategy was successfully used during the full 2018 run of the CMS pixel detector, and its efficiency was demonstrated in the second IRRAD run and in X-ray testing**

## Patch 2 for FEAST2.1 (only for environments with TID > 500krad):

**Provide a path for the mirrored leakage current**

**A sufficiently small external resistor will do the job**

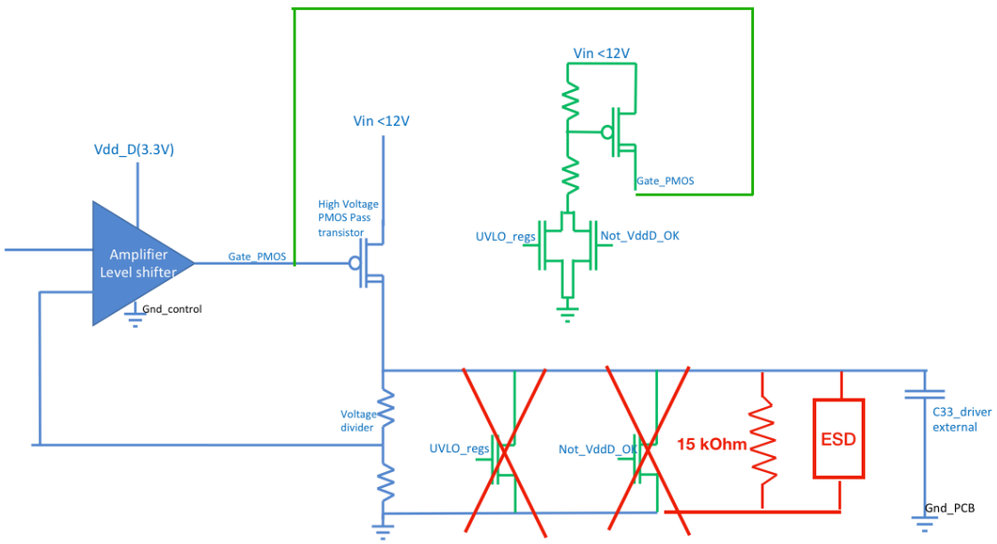
In our tests, a 3 KOhm resistor is OK




**The efficiency of this strategy was demonstrated in the second IRRAD run and in X-ray testing**

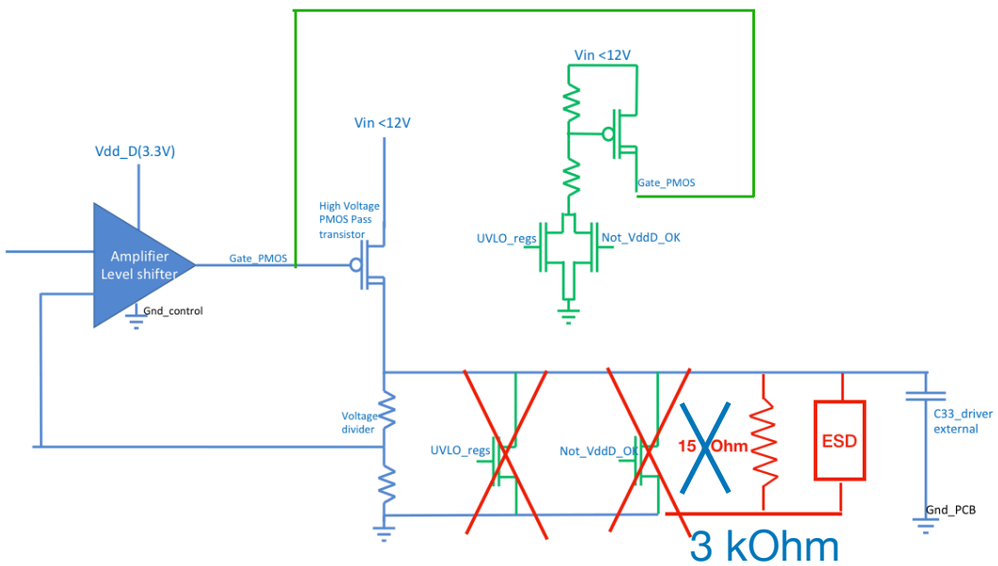
## Long-term solutions:

## FEAST2.2




Used in FEASTMP modules produced in the first half of 2019.
During X-rays testing, no voltage peak on V33Dr event at -30°C if the dose rate is below 180krad/hour

## FEAST2.3

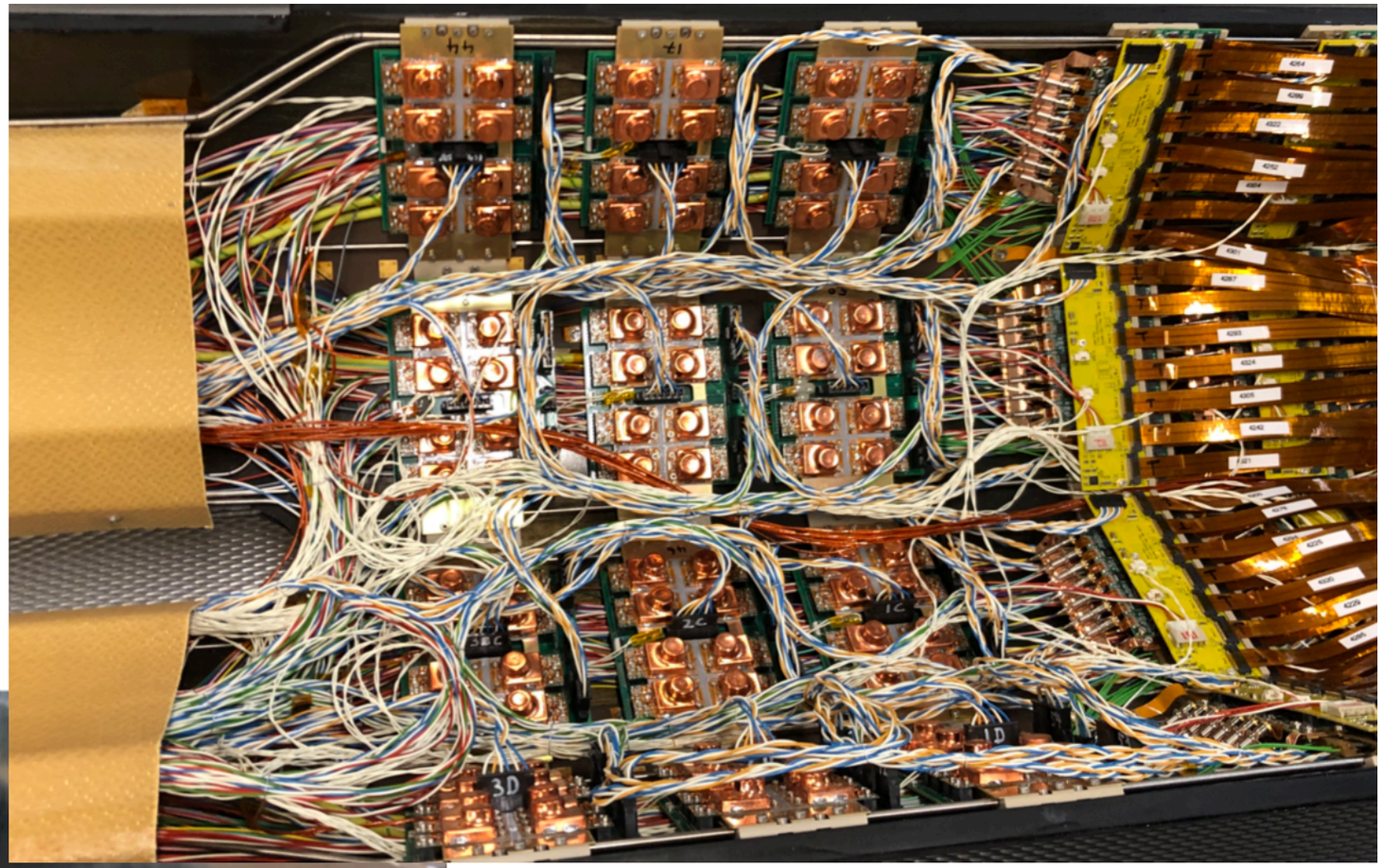


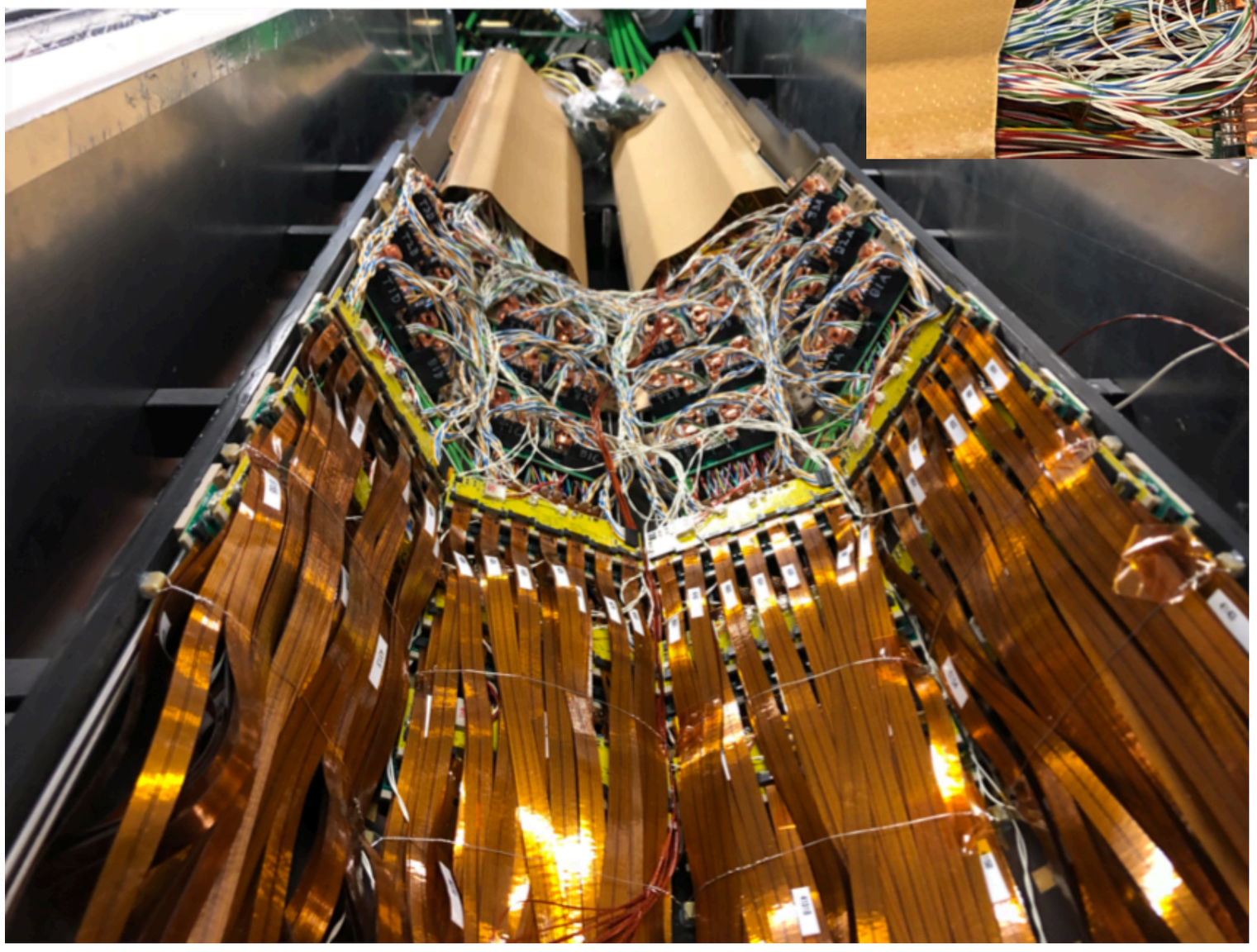

Present default version for all modules

# Final thoughts

**This is a very complex system**

- Assembly of different sub-systems
- Unique “prototype”
- Tested in the real environment only

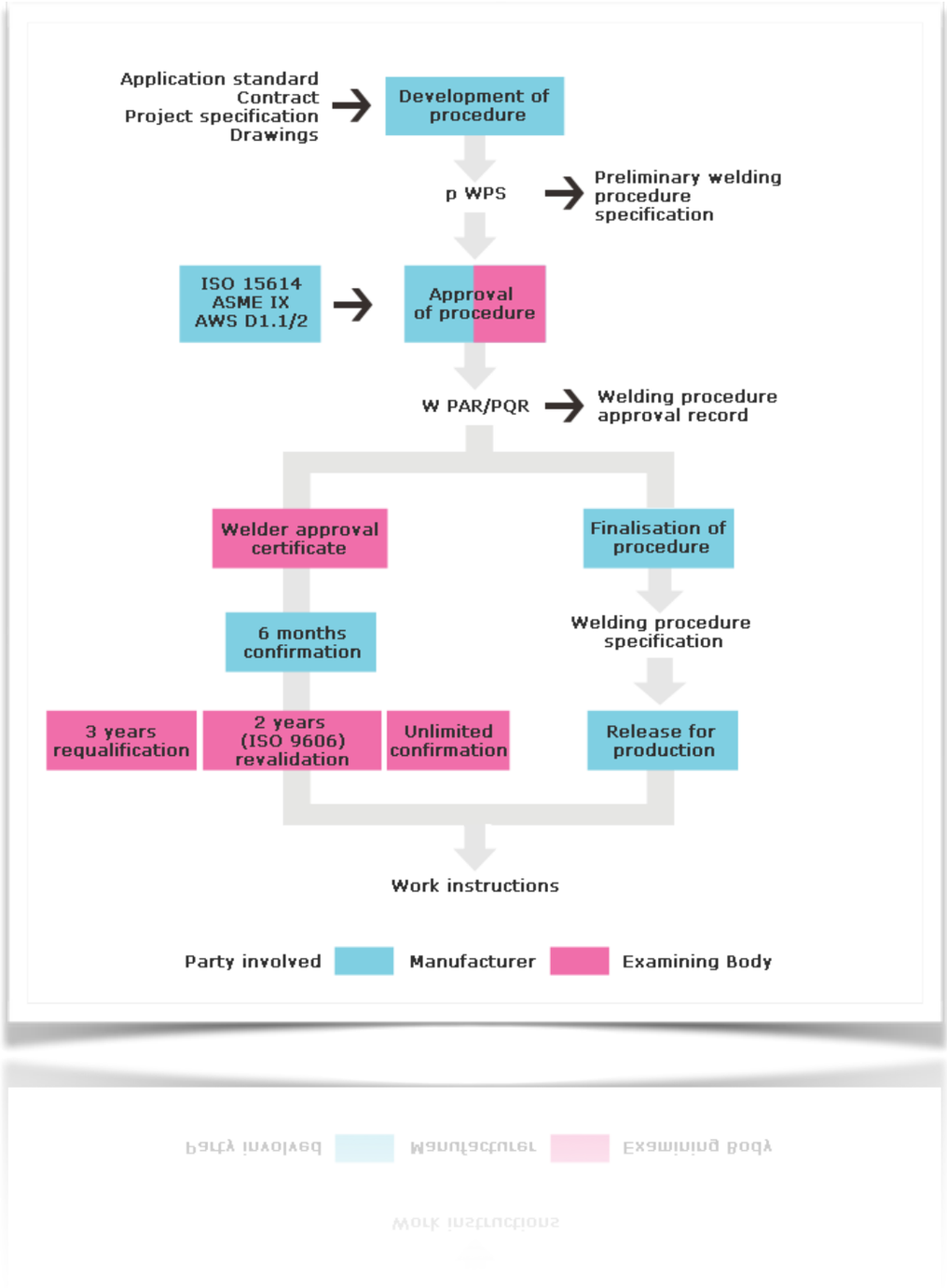




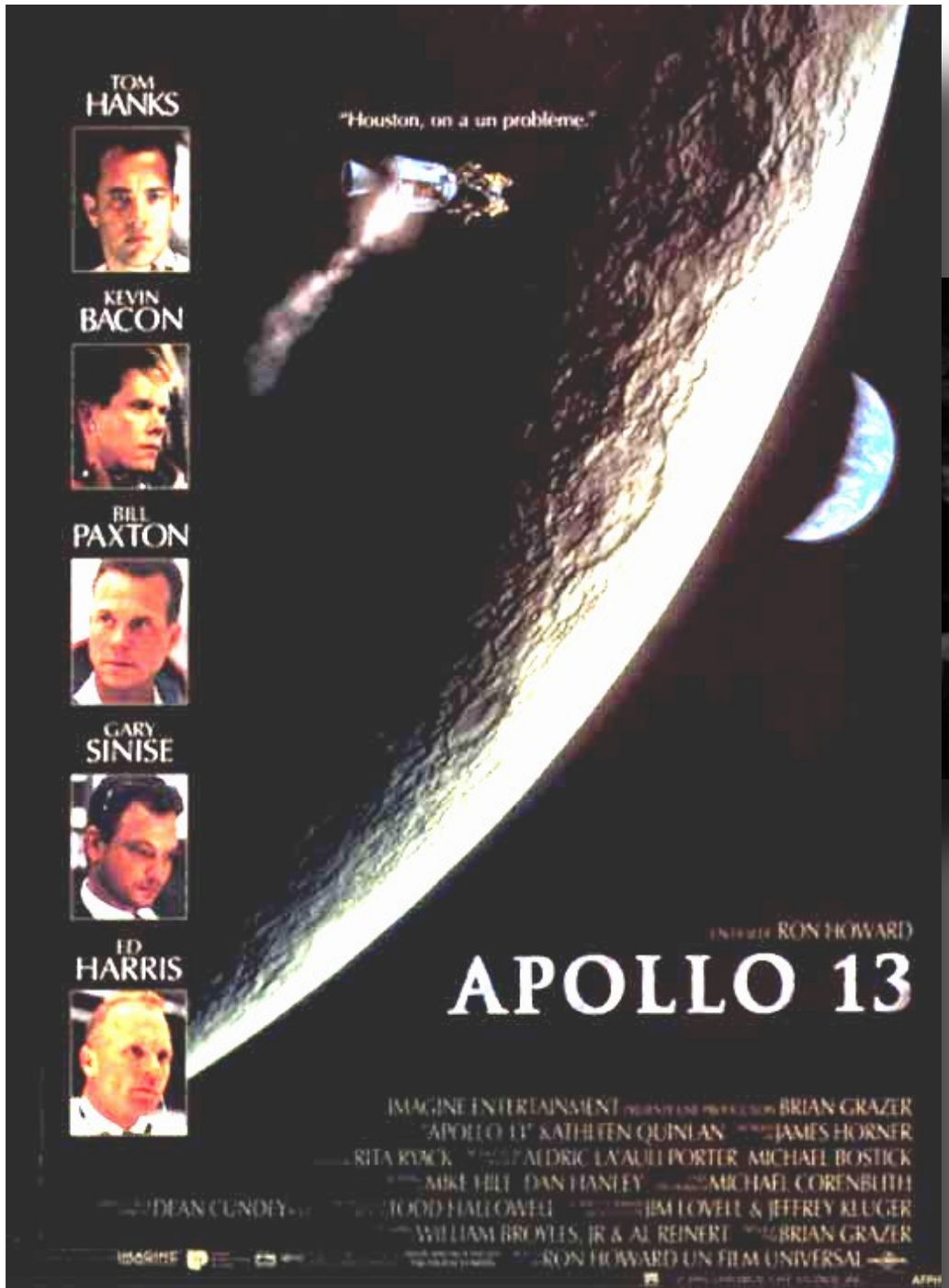
**List of expert EMC recommendations after the observation of the system:**

- **Improve filters for incoming transients on the DC supply lines**
- **Improve capability of system to route high frequency common mode (including connection of cable screens)**
- **Improve system equipotentiality (including cable screens, glued screens of detector and metallic parts of the cooling circuits)**
- **Avoid using twisted pairs for asymmetric signal or power connection**
- **Avoid separated grounds leading to severe lack of immunity against E-fields and transient H-fields**

# How about qualification practices?



# We are not NASA in the 1970s…




## Some reasons to be grateful for our luck

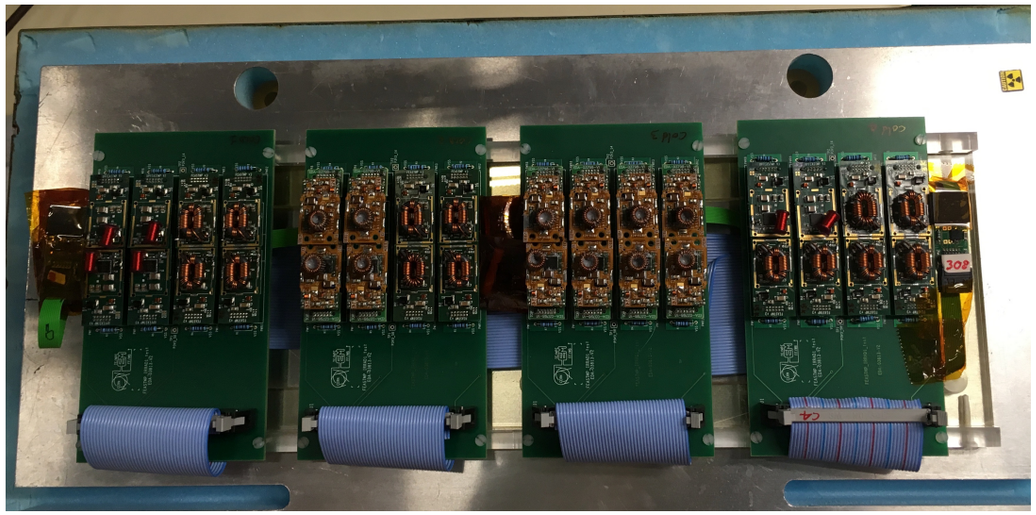
- The designers of the failing component were still around, and at CERN
- The problem happened to a detector that is amongst the easier to open
- Once understood, patches and fixes were easy to implement
- The problem appeared in 2017 and not in HL-LHC trackers

**Personally I'm always ready to learn,
although I do not always like being taught**

**W. Churchill**

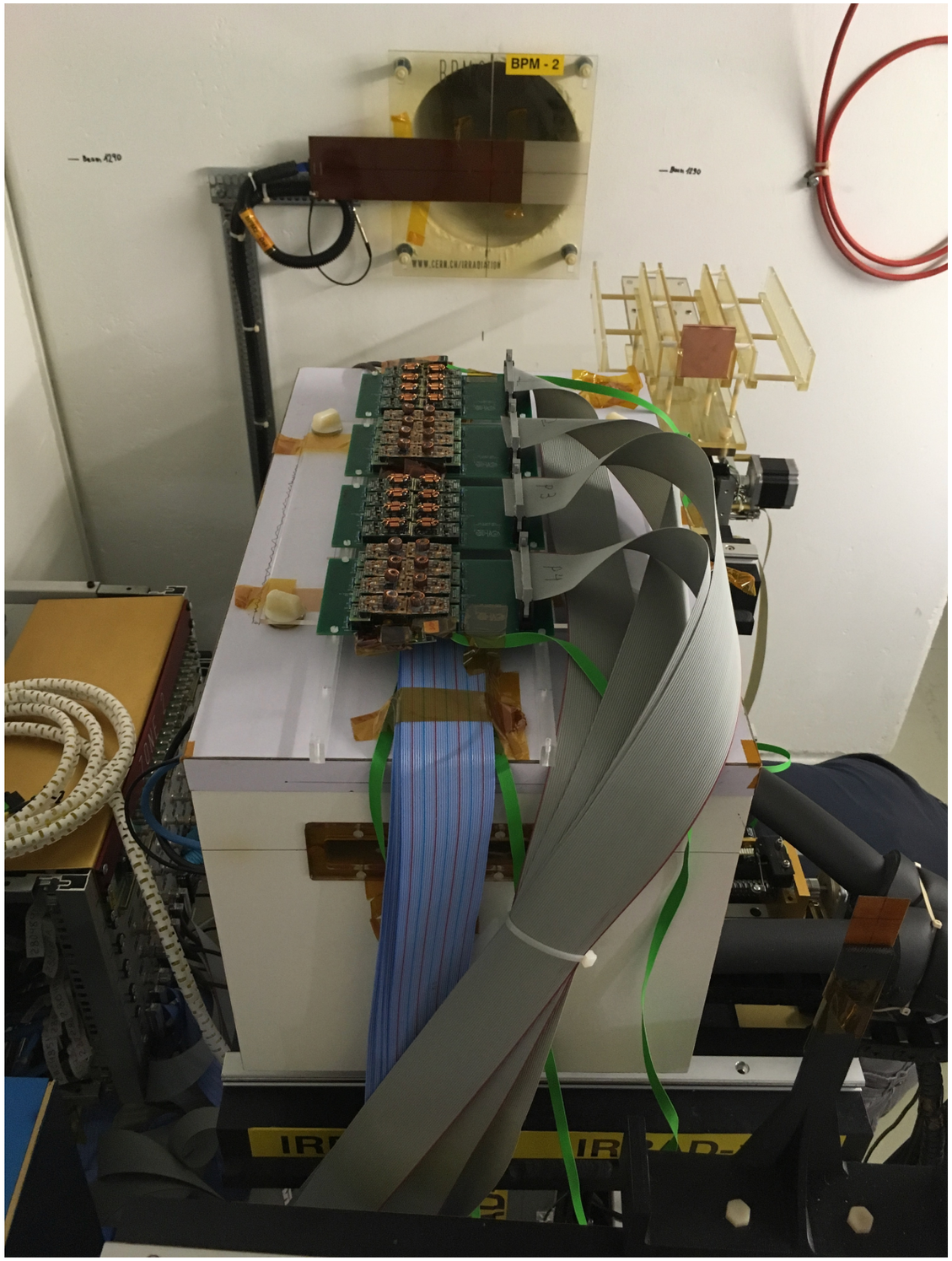
# Experimental confirmation:
# Second run at the IRRAD facility

# A second run in IRRAD used 64 converters

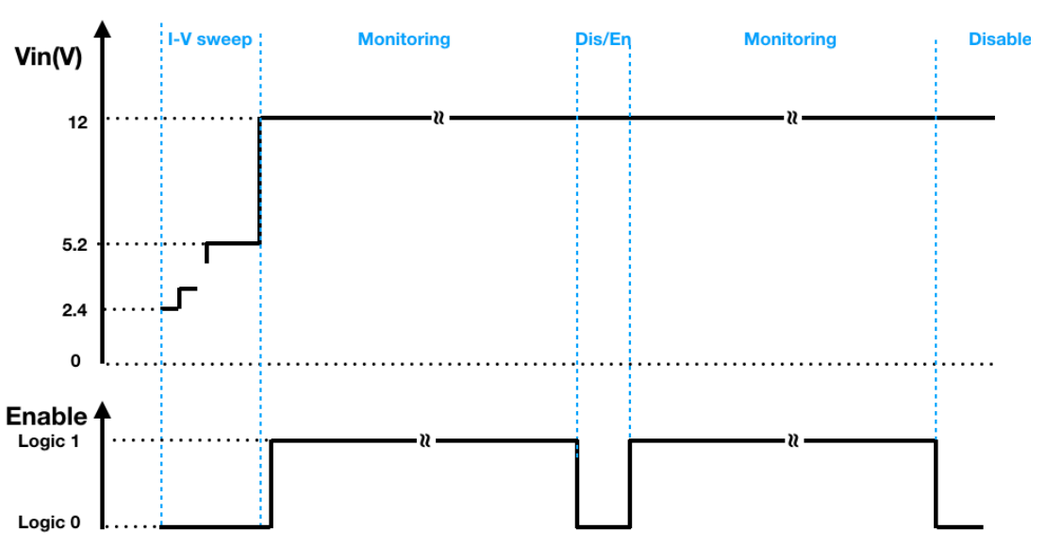


*Samples inside the cold box*

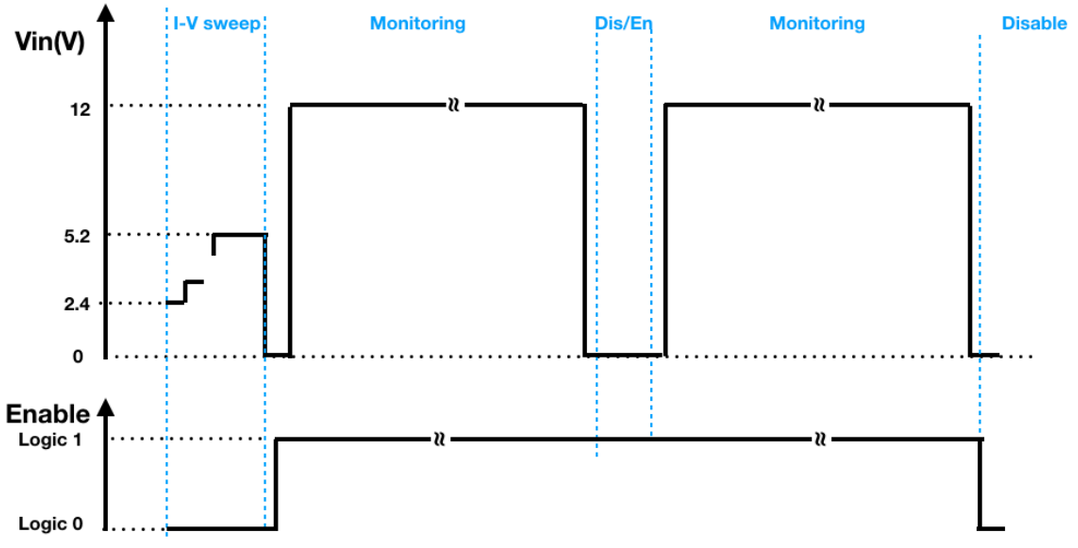
*Samples at room T on top of the cold box*



- Samples at room T and at -25°C
- New samples and samples survived during the first run
- Samples protected with the addition of a 15kOhm resistor
- Samples protected with the addition of a 3kOhm resistor
- Samples biased with a Vin of 8V (versus 12V for all others)
- Samples without disable/enable sequence (turned off decreasing Vin)
- Half of the samples had the enable input protected by an RC filter



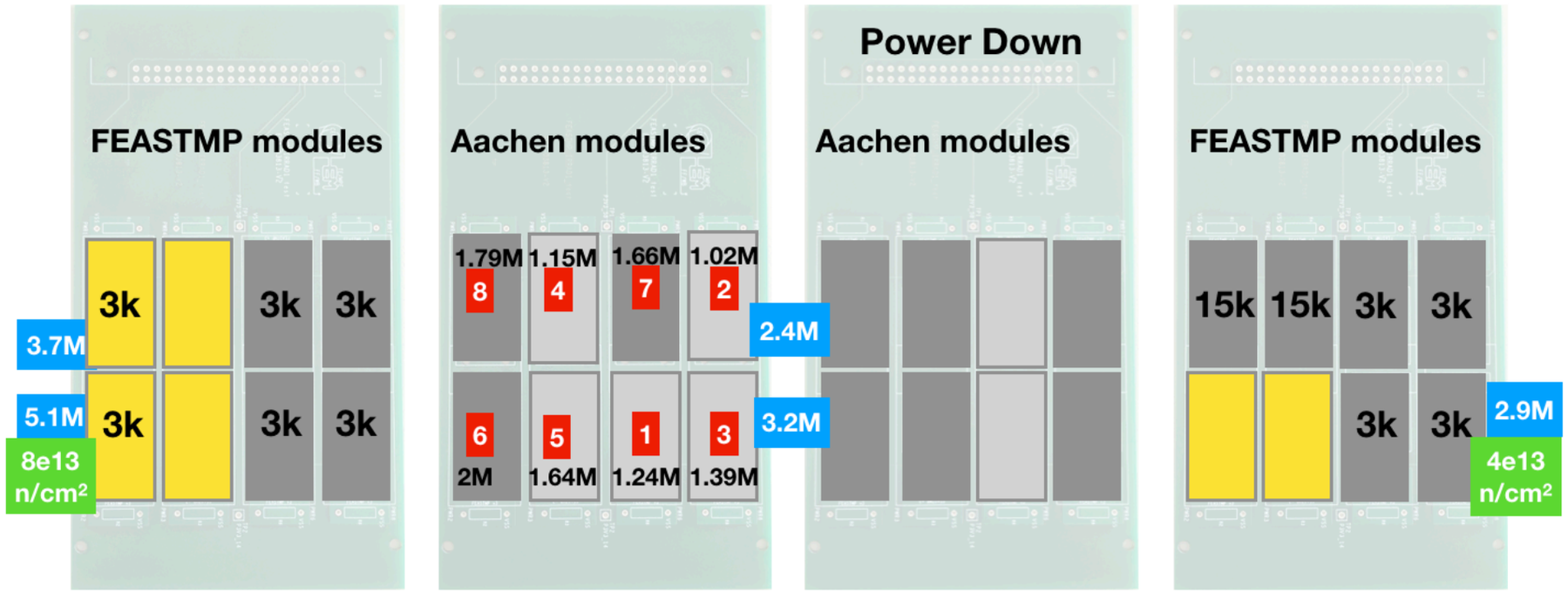

*Sequence used during the first run*



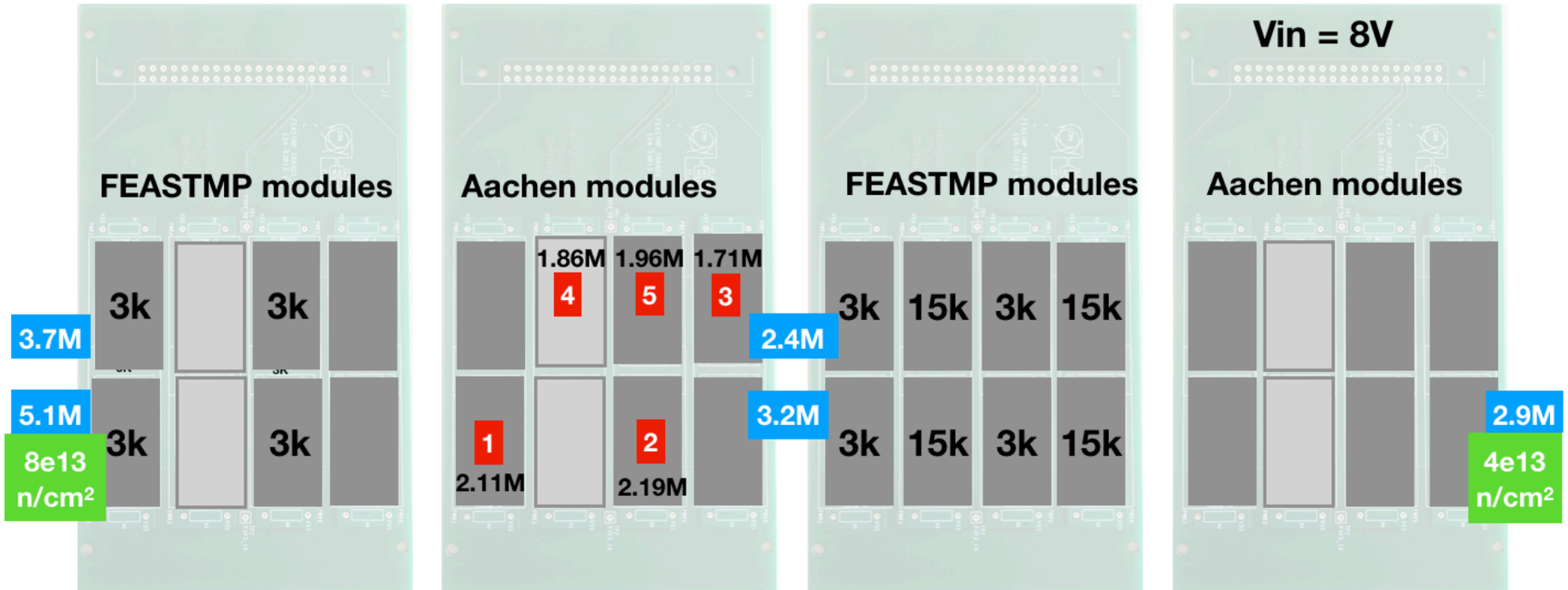

*Sequence avoiding the disable/enable at high Vin*
*Applied ONLY to 8 converters during the second run*

# The results were well in agreement with our expectations

**Color code:**
**Dark grey** = FEAST2.1 new
**Light grey** = FEAST2.1 from run1
**Yellow** = bPOL12V
**Protection resistor if indicated**




*Inside the box, T=-25°C*

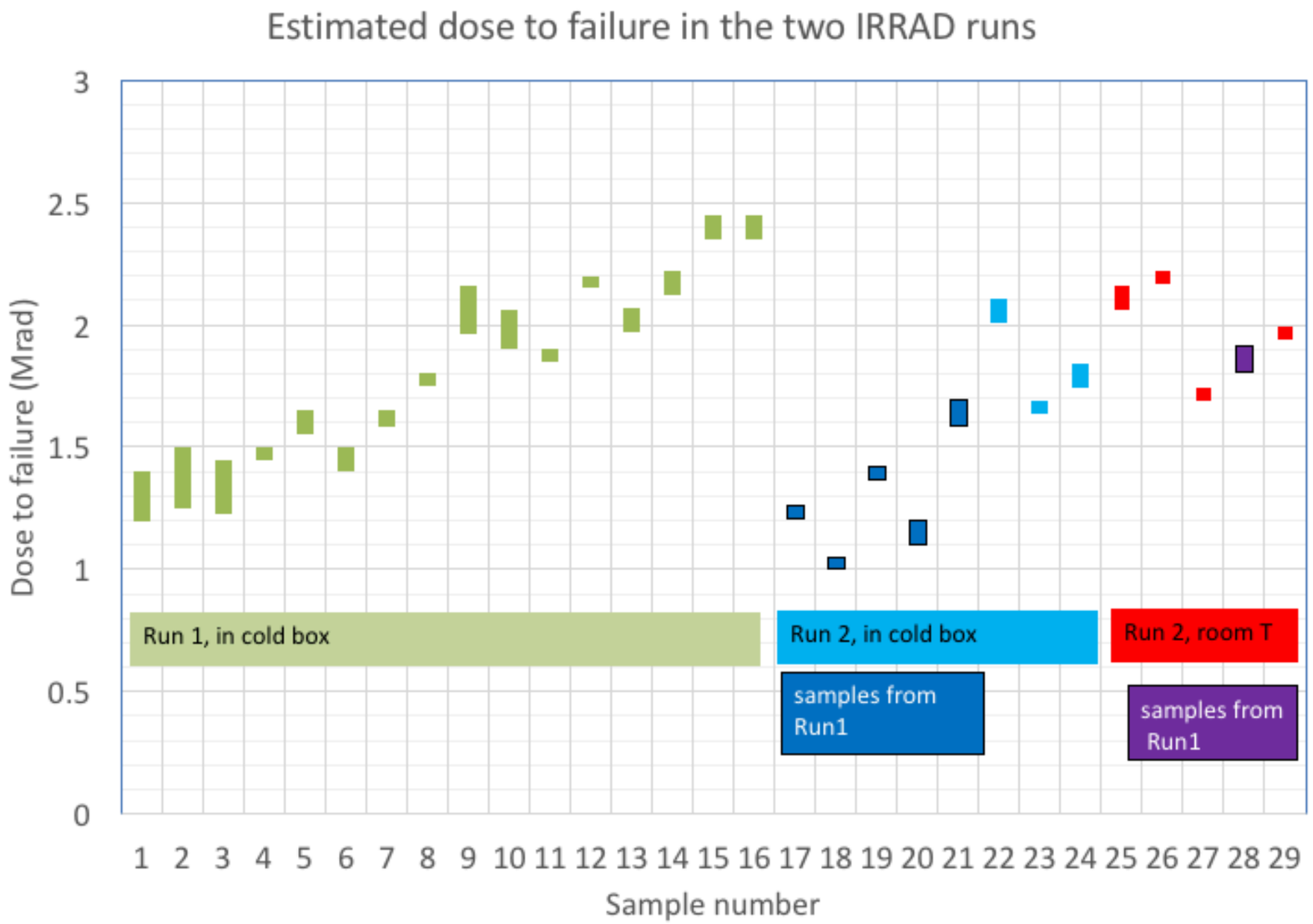



*Outside the box, room T*

**Summary of the observations during the second run**

| | |
|---|---|
| - Samples at room T and at -25°C | - Worse damage when cold |
| - New samples and samples survived during the first run | - Damage earlier if pre-exposed |
| - Samples protected with the addition of a 15kOhm resistor | - No damage |
| - Samples protected with the addition of a 3kOhm resistor | - No damage |
| - Samples biased with a Vin of 8V (versus 12V for all others) | - No damage |
| - Samples without disable/enable sequence (turned off decreasing Vin) | - No damage |
| - Half of the samples had the enable input protected (RC filter) | - No damage |

# Summary of the best estimate for the dose to failure for the two IRRAD runs




**Damage only occurs above 1Mrad in these high-dose-rate (and low-T) experiments**

# A revised version of the ASIC (FEAST2.2) to remove the damaged transistors

**In February 2018 we have modified the design of the ASIC to remove the "weak" low-voltage transistors from the V33Dr node, as well as to add a dedicated ESD protection device to the pad.**

- **this was meant to eliminate the "broken" type of damage (only "High-current" possible)**
- **additionally, this could have helped the node to resist a hypothetical aggression (discharge?)**