TWEPP 2019 Topical Workshop on Electronics for Particle Physics

Report of Contributions

Contribution ID: **1**   Type: **Poster**

Coming challenges for Photon Science detectors: an ASIC designer perspective

Thursday, September 5, 2019 4:55 PM (20 minutes)

Coming developments in X-ray photon sources will increase signal rate and intensity. Similar performance improvements are needed in a new multi-mega pixel imager. Its readout ASIC is to be based on charge-integration, be compatible with different sensor types, include adaptive-gain (to achieve single-photon resolution and high dynamic range), radiation-hard solutions and circuits for rapid characterization. On-chip digital conversion is desirable; readout should happen indefinitely at over 100kfps rate.

It is our intention to present challenges and ideas, to get advantage of the expertise of the HEP community to look for solutions that could be applied to the Photon Science field.

Summary

Coming developments in X-ray photon sources will provide improvements in terms of average signal rate and intensity. Upgrades of Storage Rings to Diffraction Limited operation is expected to increase brilliance by two orders of magnitude. At the same time, upgrade of superconducting-linear-accelerator-based Free Electron Lasers to Continuous Wave operation might slightly reduce burst-bunch-rate, but will speed-up average-bunch-rate up to 10e5~10e6 per second.

Similar performance improvements are needed in detectors to cope with upgraded sources. It is our opinion that these challenges are best answered with the development of a new multi-mega pixel imaging detector (in the form of a Hybrid Pixelated Array), with a frame rate of over 100k frame/sec and a dynamic range from single photon sensitivity to 1e4~1e5 photon/pixel/image.

Its readout ASIC is to be based on a charge-integrating scheme, to cope with the expected high photon flux. Both electron- and hole-collection capability is needed in the readout circuit, to take advantage of the sensor (conventional Si, low gain avalanche, high-Z) most appropriate for a given photon energy range (respectively ~10keV / ~1keV / 60~100keV).

An adaptive gain scheme (operating in real time, independently for every pixel) is needed to achieve single-photon resolution in low flux condition (down to a few keV), while avoiding saturation in highly illuminated pixels, and remaining below Poisson noise.

Correlated Double (and when needed, Multiple) Sampling, low-noise circuitry and Programmable Gain Amplification selection should be included in the pixel architecture; radiation hard solutions (by enclosed gate layout or equivalent) need to be use to harden key circuits against radiation damage, to mitigate performance degradation.

On-chip digital conversion is highly desirable: signal processing and readout should be able to happen indefinitely at a rate exceeding 100k frame/s (rather than being limited by an internal memory as happens today in fast detectors for FEL), with minimal or no dead time (Continuous Read-Write operation). Embedded circuits for rapid characterization and calibration of devices in realistic environments also need to be included, ideally in different points of the readout chain.

A pixel pitch between 50 and 100 um seems a reasonable compromise between spatial resolution and signal-processing needs, as four-side-buttability (prerequisite for modularity and ease-of-replacement) calls for minimization of peripheral insensitive areas.

Power consumption (and heat dissipation), readout line parallelization and efficient ways to deal with the sensor output (which can easily can exceed 100 Gbit per ASIC) need to be considered as

well.
It is our intention to present these challenges and ideas, with the aim of getting advantage of the expertise of the HEP community to look for solutions that could also be applied to the Photon Science field.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **2**   Type: **Poster**

Innovative and Expandable Physical Implementation Method for High-Speed Triple Modular Redundant Digital Integrated Circuits in Radiation-Hard Designs

Tuesday, September 3, 2019 5:20 PM (20 minutes)

We present an innovative and expandable physical implementation method for high-speed Triple Modular Redundant (TMR) digital integrated circuits. The implementation uses a new interleaved placement approach in comparison to a generally used bulk 3-bank constraining method. To optimally constrain the placement of sequential cells as well as combinational cells. The TMR netlist information is used to divide the netlist into banks which do not interact logically and allow SEE charge sharing without compromising reliability. The technique was simulated in a 65 nm CMOS technology and resulted in a reduced total net length of 47 % dynamic power consumption of 25%.

Summary

It has been generally known that ionizing radiation can cause Single Event Effects (SEEs) in CMOS integrated circuits, particularly in scaled technologies. Generally, Triple Modular Redundancy (TMR) is used to overcome errors. Commonly TMR blocks are spaced sufficiently to avoid multi-cell upsets at the cost of difficult routing and increased power consumption. Another strategy for physical usage of TMR in high-speed digital circuits is presented in this paper. The design approach avoids long interconnections between voters by using interleaved placement constraints. A TMR fan-in tracing algorithm is utilized to partition the combinational logic in clusters (A, B, C) corresponding to triplicated branches. Ideally, every cell is guided with a spacing requirement to space them correctly, with maximum freedom. Nowadays such features are accessible in the most recent place-and-route releases. This can be utilized to guarantee the spacing distance between flip-flops, however, the spacing between the combinational logic cells cannot be ensured in the same way since the number of constraints would be too high. In moderate to complex data-paths, constraining flip-flops only is not sufficient.

In the proposed method, a floorplan is made using 6 physical constrain groups (A1, A2, B1, B2, C1, C2), or noted as ABC1 and ABC2. Each group A1-C2 has a height of the required spacing distance and occupies the entire width of the design. Vertically, all groups are subsequently repeated multiple times to fill the vertical design space (e.g. ⋯A1-A2-B1-B2-C1-C2-A1-A2 ⋯). A TMR datapath is placed in either ABC1 or ABC2. As such, one ABC group acts as spacers to each other. To ensure maximal area efficiency, TMR datapaths are balanced between ABC1 and ABC2 if they do not interact logically and thus are allowed to share multi-cell upsets.

The major advantage of this approach is that the place-and-route tool has more freedom to distribute logic across the floorplan. In contrast to the 3-blocks approach, interconnections between voters do not need to cross a big center block that results in major routing complexity and power consumption. With the proposed method, the total net length is drastically reduced since the connected logic can be placed closely together, still ensuring minimal spacing for SEEs. As a consequence, the switching power is also reduced, as a result of the reduction in the total net length. For the tested circuits, the total net length reduced by up to 47% while the switching power consumption is reduced by 25%. Furthermore, the routing complexity was significantly simplified compared to a bulk 3-block physical floorplan. By using the placement balancing between ABC1

and ABC2, there is no area penalty.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **3**   Type: **Poster**

Development of a high bandwidth PCIe card for the ATLAS HL-LHC Upgrade and DUNE experiment

Tuesday, September 3, 2019 5:20 PM (20 minutes)

FELIX, the PCIe based framework has been used in the DAQ system of ATLAS Phase-I upgrade and the APA (Anode Plane Assemblies) readout in Single-Phase ProtoDUNE experiment. For the ATLAS HL-LHC upgrade, the fiber optical links from front-ends will have higher speed. This manuscript introduces a FELIX demonstrator board with PCIe interface designed for the HL-LHC upgrade. In this board, 25+ Gbps optical links will be supported with both optical transceivers and FMC+ mezzanine, in addition to FPGA embedded PCIe hard IP block for high bandwidth interface with the CPU.

Summary

The Front-End LInk eXchange (FELIX) is a novel readout system to interface with front-end electronics and a commodity network in the ATLAS Phase-I upgrade. It has also been used in the neutrino experiment Single-Phase ProtoDUNE. The Phase-I FELIX card has 4 pairs of 12-channel MiniPODs which support 48 bidirectional fiber optical links with speed up to 14Gbps. The interface to the PC is a 16-lane Gen-3 PCIe supporting a throughput up to 101Gb/s.

For the HL-LHC upgrade, the event rate will increase from 100 kHz to about 1 MHz. Meanwhile the event size will increase from ~2 MB to ~6 MB. After the upgrade, the speed of lpGBT links (10.24Gbps) will be about twice of current GBT links (4.8Gbps). The custom lightweight protocol, the FULL mode will use higher link speed than the one (9.6Gbps) implemented for Phase-I upgrade. Since the HL-LHC upgrade will be in 2024, the new generation PCIe Gen-4 or Gen-5 will be considered for the baseline FELIX design. To evaluate various key technologies for the FELIX card in HL-LHC, a demonstrator board is developed. The Xilinx FPGA VU9P is used which has Gen-3/Gen-4 PCIe hard IP blocks. 64 high-speed optical links will be supported by using different modules like the BOA from Finisar, the OBT from Amphenol and the FireFly from Samtec. These optical modules support link speed up to 25 or 28 Gbps. Verification of these modules have been done with a Xilinx evaluation board VCU108 in the lab. The designed demonstrator PCIe card will also be used in the evaluation of DUNE readout, which has one candidate solution to transfer the received streaming APA data to a mezzanine for further data processing. In this design, the FMC+ mezzanine interface is implemented. Besides the data bus with 34 pairs of differential lines, 24 high speed GTY transceivers are also connected from the FELIX FPGA to the FMC+ mezzanine. A timing mezzanine card will be used on this PCIe card to support different timing systems. Four differential clock signals and more than 10 differential data signals will be connected between the FELIX FPGA and timing mezzanine. The board will have a 288-pin DDR4 DIMM slot to support high bandwidth data buffering.

To support the complex design of the FELIX demonstrator, a new 24-layer stack-up will be used which has a thickness of about 2.67mm. To make the PCIe edge connector be compatible with the PCIe specification, the connector area will only have 14 layers for thickness of 1.6mm. Two sub-assemblies will be applied to layers 1-14, and layers 15-24, and sequential lamination will be required for the PCB fabrication. To improve the signal integrity for the high-speed links connected to the GTY transceivers, stubs of these traces should be as short as possible. Several types of back-drills are used for vias on these high-speed traces.

This manuscript will introduce the design considerations and technical implementations of this PCIe card. Preliminary test results will also be presented.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 4   Type: **Poster**

A NEW COMPACT ELECTRONICS FOR CALICE SIW CALORIMETER READOUT

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Ultra-compact electronics is required for the control and readout of the Silicon-Tungsten electro-magnetic calorimeter of the future ILD detector (CALICE collaboration). Prototypes have been designed years ago, comprising the ASUs (Active Sensor Units) located inside the detector Slab and housing the front-end ASICs, and an external part for controlling the system and reading out physics data. Up to now, the latter was not to scale with the reduced space and power available at the Slab extremity. The paper will present the new SL-BOARD which has been designed together with a kapton-based interconnection system in order to fit these stringent requirements.

Summary

The Silicon-Tungsten electromagnetic calorimeter (SiW ECAL) of the future ILD detector (CAL-ICE collaboration) is based on the concept of highly integrated modules internally housing the so-called ASU boards (Active Sensor Units), themselves housing the front-end electronics ASICs (SKIROC). The Slab (up to 13 interconnected 1024-channel ASUs) needs to be configured, supplied with low voltage and read out via the new digital interface which consists of three elements:
- The SLab digital interface board (SL-board) which is connected to the first ASU of the chain.
- The Control & Readout Kapton (C&R Kapton) which connects the SL-boards to the Control and Readout (CORE) module.
- The CORE Module which performs the interface for power, control and readout of detector modules.
In the ILD Detector, the SL-board will be installed between the ECAL and the HCAL which are separated by only 67 mm including 25 mm of mechanical tolerance. In the other dimension, the extension has to be less than 70 mm because of the detector electronics cooling. The SL-board respects these daunting space constraints and is designed for low power consumption and good signal integrity. High versatility for testing and debugging of the system was also taken into account.
The SL-Board handles the Control & Readout of the chained ASUs, therefore communicating with the SKIROC chips, and the interface to the CORE acquisition module through a kapton cable (rigid PCB on the slab side with a flex part on the CORE side). It is designed around an Altera MAX10 mixed CPLD/FPGA low power technology. It is equipped with a 40MHz oscillator and a remote USB interface permitting a standalone control of the Slab and an easy debugging of the full set of interconnections.
In order flexibly deal with the angle of 45° of the C&R Kapton, the SL-Board provides a flex extension of 40 mm in length, holding a 0.8mm pitch connector. Its 40 pins transmit differential pairs for sensitive signals, unipolar signal lines, a few spare lines, and ground. The rigid part of the C&R Kapton can connect up to 15 SL-boards, each of which has its own individual flow control and readout differential lines in addition to the common lines.
The CORE-Module is based on a mother board (CORE-Mother) which provides the interface to the DAQ (USB and Gbit UDP (both copper and optical)), reception and transmission of the DAQ clock, delivery of adequate power supplies. The CORE-Daughter is connected to the C&R Kapton flex via a 100-pin connector. Its role is mainly the transmission of clock and fast signals to the SL boards, the collection of event data, and the control of detector electronics. Event data travels in parallel

on individual differential lines on the CORE Kapton and is grouped on an event by event basis in the CORE daughter, before being transmitted to DAQ.

A powerful software with graphical interface has been developed for controlling the full system. The paper will present the implementation of the system in test beam at DESY during summer 2019.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **5**   Type: **Poster**

The hardware demonstrator of the Phase II ATLAS Level-0 MDT Trigger processor

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The first level (L0) muon trigger of the ATLAS experiment will be upgraded to operate at the High Luminosity LHC.

The selectivity of the current L0 muon trigger is limited by the moderate spatial resolution of RPC and TGC. The MDT chambers currently used for precision tracking will be therefore included to improve the momentum resolution and the redundancy.

A hardware demonstrator of the MDT trigger processor is presented. It consists of an ATCA blade, constructed of two separate modules, and based on FPGA technology. An overview of the explored algorithms for the track finding task will also be shown.

Summary

The first level (L0) muon trigger of the ATLAS experiment will be upgraded to operate at the High Luminosity LHC.

The selectivity of the current L0 muon trigger is limited by the moderate spatial resolution of RPC and TGC. The MDT chambers currently used for precision tracking will be therefore included to improve the momentum resolution and the redundancy.

In the Phase-II scheme, the MDT trigger processors will receive MDT hits from the detectors and match them to the trigger candidates (seeds) from the RPC and TGC+NSW trigger chambers. These seeds provide a region of interest (RoI) and the identification of the bunch crossing from which the muon originated. This is the t 0 for computing the MDT drift time from the arrival time of the hit. MDT hits matched to the RoI are then used by the MDT trigger algorithm to improve the momentum resolution, by forming track segments and joining them together for momentum determination.

A hardware demonstrator of the MDT trigger processor is presented. It consists of an ATCA blade, constructed of two separate modules called the "Command Module" and "Service Module", and based on FPGA technology. An overview of the explored algorithms for the track finding task will also be shown.

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Session Classification: Posters

Track Classification: Trigger

Contribution ID: **6**   Type: **Poster**

Radiation damage of Silicon Photomultipliers by irradiated fast neutrons

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Silicon Photomultipliers (SiPM) are beginning to be actively used in high-energy physics experiments (CMS, LHCb, ATLAS in CERN), therefore careful study of the effect of high radiation fields on the operation of these devices is necessary. This work studies the effect of irradiation with fast neutrons on the work of SiPM (manufacturing: Hamamatsu Photonics K.K.) with an active area of 1 mm^2 (types -010C, -015C, -1325CS) and 9 mm^2 (-015P) with the equivalent fluence 1 MeV neutrons in range from 10^{11} to $5 \cdot 10^{14}$ cm^{-2}.

Summary

The following main parameters of a SiPM were measured and analyzed before and after irradiation: the dependence of the coefficient of multiplication on the overvoltage, current-voltage (I-V) and capacitance-voltage (C-V) characteristics. It was determined that after irradiation a few negative effects appear: an increase of dark current and breakdown voltage. Dark current in non-irradiated SiPM are formed due to the process of thermogeneration of electron-hole pairs in a silicon volume, and value of dark currents depends on effective lifetime for these charge carriers, which decreases in the process of irradiation due to the creation of radiation defects in epitaxial layer (space charge region), which leads to growth bulk dark current in region without gain and breakdown voltage. To use the SiPMs in high radiation fields conditions requires the selection of the optimal type of SiPM taking into account the magnitude of the gain, the dynamic range of the measured signals, temperature conditions, and also the correction of the operating voltage with increasing radiation damage.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **7**   Type: **Oral**

Development of Readout Electronics for a Digital Tracking Calorimeter

Thursday, September 5, 2019 4:30 PM (25 minutes)

Highly segmented digital tracking calorimeters (DTC) consist of multiple layers of high-granularity pixel detector CMOS sensors and absorption/conversion layers. Two separate prototypes are being developed: (1) an electromagnetic calorimeter (FoCal) for a proposed ALICE upgrade (during LS3) and (2) a hadronic calorimeter for medical proton CT imaging (pCT). These prototypes employ the ALPIDE detector chip developed for the ALICE ITS. The ALPIDEs are mounted on intermediate Aluminum/Polyimide-flexible PCB with ultrasonic welding. This contribution presents findings and solutions to the challenging design of high-speed readout electronics with efficient use of FPGA resources for these prototypes.

Summary

Highly segmented digital tracking calorimeters (DTC) consist of multiple layers of high-granularity pixel detector CMOS sensors and absorption/conversion layers. Two separate prototypes are being developed: (1) an electromagnetic calorimeter (FoCal) for a proposed ALICE upgrade (during LS3) and (2) a hadronic calorimeter for medical proton CT imaging (pCT).

The pCT implementation of a DTC consists of 41 layers of 108 ALPIDEs each ($\sim 27 \times 18$cm), where 9 chips are mounted together on a stave. The chips are mounted onto thin flexible Aluminum/Polyimide PCBs with ultrasonic welding. Three flex staves mounted on a thin Al-carrier form a basic module. Identical modules are the building blocks of the high-resolution layers of FoCal. Both prototypes have in common that they generate a large data rate locally due to high occupancy and that the designs are compact, i.e., the readout electronics has to handle a high density of high-speed links. In this contribution we are focusing on the pCT prototype.

The readout unit (RU) is interfacing all 108 x 1.2 Gb/s asynchronous data links in a layer, as well as all control and clock links. The RU consists of a Xilinx Ultrascale+ FPGA that is responsible for controlling the detectors and reliably transferring detector data upstream for processing.

The large density of high-speed links presents a challenge for the readout electronics. Few FPGA's have sufficient multi-gigabit transceivers (MGT) to interface the high number of asynchronous data links. However, newer generations of FPGA's have regular I/O-pins that are able to reliably sample up to 1.6 Gb/s data streams without the use of specialized transceiver pins. The downside of this is that no dynamic phase adjustment is presented to the user automatically and must be implemented manually in fabric logic. Employing Alexander (bang-bang) phase detection along with Xilinx I/O primitives to dynamically adjust the sample phase we achieve a link performance comparable to the MGT I/Os. This enables the use of fewer FPGA's per layer of the DTCs. On a Xilinx Ultrascale FPGA this increases the amount of possible links with at least a factor of 4 while also leaving transceiver pins available for other purposes.

The FPGA has a limited amount of on-chip memory. A high data burst size and rate from the sensors result in the need to offload the data from the RU in a highly efficient manner to avoid back-pressure and buffer overflow. Considering that all transceiver pins are still available, these can thus be employed for this purpose. Using QSFP+ we can implement 4 independent 10GBASE-R Ethernet channels transferring the data. A custom data transfer protocol, implemented in FPGA fabric for transmitting data via UDP without data loss, is under development. In addition, adopting Ethernet Jumbo frames will allow for a theoretical transfer efficiency of ~99% and thus, a total data

rate of 39.6 Gb/s. This rate allows reading out up to a maximum ˜ 105 Gpixels/s per layer, and up to ˜ 4 Tpixels/s for the entire DTC.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **8**　　　　　　　　　　　　　　　　　　　　Type: **Poster**

FELIX –Commissioning the new detector interface for ATLAS trigger and readout

Thursday, September 5, 2019 4:55 PM (20 minutes)

During the current major LHC shutdown (2019-2021), the ATLAS experiment at CERN is moving to the Front-End Link eXchange (FELIX) system as the interface between the data acquisition system and the trigger and detector front-end electronics. FELIX functions as a router between custom serial links and a commodity switch network, which uses industry-standard technologies to communicate with data collection and processing components. This presentation will describe the FELIX system design as well as report on the installation and commissioning of the full system in summer 2019.

Summary

After the current LHC shutdown (2019-2021), the ATLAS experiment will be required to operate in a significantly harsher collision environment. The LHC will deliver luminosities up to three times the original design value, with a commensurate increase in the number of interactions per bunch crossing. To maintain physics performance in this new regime, the ATLAS experiment will undergo a series of upgrades during the shutdown. Among the upgraded components will be the Trigger and Data Acquisition (TDAQ) system, which in the new environment will have to process significantly more complex events while maintaining selection performance. At the same time, the TDAQ system will have to interface with new on-detector readout technologies for the new Muon Small Wheel detector, the Liquid Argon (LAr) Calorimeter and Calorimeter Trigger upgrades. In total, the new readout paths will require approximately 2000 new optical links to be serviced by the TDAQ system.

The upgraded ATLAS systems will make use of newer readout link technologies. These include the high bandwidth FULL mode ˜FPGA-to-FPGA protocol, running at 10 Gb/s, and the radiation-hard Giga Bit Transceiver (GBT) protocol, running at 5 Gb/s. GBT links provide aggregation for up to 42 slower serial electrical links, making them critical for data collection from the front-end ASICs within the new systems. GBT links will also be used for the propagation of control and configuration data back to the front-end. To connect the new systems, and handle the significantly increased data volumes in a detector agnostic and easily scalable way, a new readout architecture named the Front-End LInk eXchange (FELIX) has been developed.

FELIX receives and identifies different information streams on its incoming optical links and routes packets to client processing applications via a commercial switched network. In the opposite direction, FELIX receives packets from the network and forwards them to specific on-detector modules. FELIX also handles input from the Timing, Trigger and Control (TTC) system to recover the LHC clock and forward synchronous trigger information to on-detector electronics over low- and-fixed-latency GBT links. FELIX supports multiple different data encoding formats, including 8b/10b and HDLC, to satisfy the requirements both of primary dataflow and experimental slow control.

The final implementation of FELIX makes use of a custom built PCIe board with a Xilinx Kintex UltraScale FPGA, a 16 lane Gen3 PCIe (128 Gb/s) interface and 48 bidirectional optical interfaces in the form of eight Mini-POD transceivers (max. link speed 14 Gb/s). TTC decoding circuitry is hosted on a custom mezzanine board to enable future upgrades of the TTC system to be supported with minimal hardware changes. The optical links, PCIe interface, and TTC decoding circuits have been verified to function well in the final hardware.

The FELIX system is due to be installed and commissioned in summer 2019. This presentation will report on the status of this installation, and the results of ongoing commissioning work.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **9**   Type: **Poster**

Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments

Thursday, September 5, 2019 4:55 PM (20 minutes)

The KINTEX-7 FPGA is to be used in the new digital readout of the upgraded LHCb-RICH sub-detectors. This summary presents the measurements done to evaluate the reliability of this FPGA under ionizing radiation exposure with different types of particle beams: ions, protons and X-rays. Single-event effect cross-sections for critical resources - such as Flip-Flops, RAM blocks, configuration memory, and I/O blocks - have been evaluated for multiple values of total ionizing dose, linear energy transfer, proton energy, and particle flux. A list of firmware constrains for this RICH application was deduced based on extrapolation to upgraded LHCb and 50 fb-1.

Summary

Following the Long Shutdown 2 of the LHC, the LHCb single arm forward spectrometer will be upgraded to operate at higher luminosity and at a higher trigger rate. The LHCb-RICH sub-detectors were redesigned to allow operation for higher HEH fluence –close to 1012 cm-2. Multi-anode photomultiplier tubes (MaPMTs) are RICH photodetectors and the triggered signals from their frontend electronics are read by DAQ through dedicated digital boards controlled by a KINTEX-7 FPGA. These FPGAs are widely used in high energy physics experiments due to their lower price and high logic density. Due to the large integrated dose - 200 krad (Si) total ionising dose (TID) - it was needed to qualify the viability of KINTEX-7 when operating in the LHCb-RICH environment. Several test beams with different particle were used: ions at the LNL in Italy and at the Cyclotron Resource Centre in Louvain Belgium; 200 MeV protons at the Paul Scherrer Institute from Switzerland and 35 MeV protons at the Nuclear Physics Institute in Juelich Germany; and an X-ray facility from the University of Padova.

Different firmware versions have been designed to test individual FPGA critical resources: user Flip-Flops, block RAM, configuration memory and the I/O blocks. Mitigation techniques were included in each of the firmware versions: triple modular redundancy (TMR) architectures for user Flip-Flops, and Soft Error Mitigation IP Core to detect and correct errors in configuration memory. To monitor and control the FPGA test board, a custom DAQ system has been designed.

Using ions, within a broad range of linear energy transfer (LET) from 1.3 ± 0.26 to 32.4 ± 6.48 MeV cm2/mg, the FPGA was tested for single-event effects. Attention was given to the single-event latch-ups and single event upsets (SEUs) in user Flip-Flops and configuration memory. The threshold for SEUs in the configuration memory has been found to be below 1.3, though we estimate it is very close to this value.

The proton beam test was used to estimate the possible TID or other cumulative effects, as well as for proton-induced single-event effects in FPGA resources. SEU cross-section (σ) values of order of 10-7 cm2/device have been extracted for the configuration memory and the BRAM blocks. This device has been proven resilient against TID up to 1 Mrad (Si). The X-Ray beam test confirmed the TID effect absence in this device.

Several failures have been seen in the I/O blocks, induced either by ions or protons. The cross-section for 35 MeV proton-induced I/O failures has been found to be lower than 10-11 cm2/device. We give qualitative conclusions and cross-section values for each critical resource tested, as function of total ionizing dose, proton energy and LET. As an example, we extrapolate these testing

results for an LHCb-RICH system with thousands of FPGAs, operating in the first Phase of an LHCb Upgraded detector with 50 fb-1 integrated luminosity.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **11**   Type: **Poster**

A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector

Thursday, September 5, 2019 4:55 PM (20 minutes)

The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade. The innermost part will be a pixel detector. A new Detector Control System (DCS) is being developed to provide control and monitoring of the ITk pixel detector. The DCS Controller is a CANopen based Application Specific Integrated Circuit foreseen to independently monitor a serial power chain. The final chip is required to be radiation hard up to an ionizing dose of 500 Mrad. In this talk, the functionality of the chip will be discussed and also results from the first test chip will be presented.

Summary

The Large Hadron Collider (LHC) will be upgraded to the High Luminosity LHC which also requires experiments to be upgraded. The ATLAS experiment will get a new full silicon inner tracker. The innermost part of the ATLAS experiment is the pixel detector. After the upgrade, the pixel detector will have 5 times more modules than the present state. A serial powering scheme has been proposed to reduce the number of services inside the detector volume. There are multiple serial powering chains and each chain can have a maximum of 16 modules connected in series. The Detector Control System (DCS) provides control/monitoring capability and also ensures the safety of the experiment.

The DCS system has three independent paths which are diagnostics, control & feedback, and safety. The diagnostics path provides high granularity data generated by the Front-End (FE) chips for debugging and fine-tuning of the system. The control & feedback path provides the main user interface to operate the detector. Power supplies provide control per serial power chain whereas the DCS controller provides information per detector module. The DCS controller must provide monitoring information even when the detector is not running. The Safety path is the hardwired interlock path which directly acts on the power supplies and has the highest reliability.

The DCS Controller is an ASIC foreseen to be used in the control & feedback path and has the same radiation tolerance requirements as the FE chip. The DCS Controller chip will have an ADC with a resolution of 12 bits and up to 40 channels to read voltages and temperatures of each module in the serial powering chain. The voltage across an individual module is read using a voltage divider circuit. The temperature of the modules is given by reading NTCs available on each module. This NTC is connected via an external pull-up resistor to the reference voltage provided by the chip.

The DCS controller communicates to the main server over Controller Area Network (CAN) bus using an integrated CAN controller and a physical layer. The core logic of the DCS Controller chip is the bridge controller to implement the hardwired version of the application layer CANopen protocol which is normally implemented in software. Both of these protocols are being implemented in a 2x2 mm2 chip which is also required to be radiation hard up to a total ionizing dose of 500 Mrad. Other components in the chip include CAN physical layer, Power-on-Reset, band-gap circuit, voltage regulators and an oscillator. This chip is designed using TSMC 65 nm technology and implements 5V circuits using core transistors.

The first test chip includes voltage regulators and the physical layer for the CAN bus while the first prototype of the digital logic has been implemented on an FPGA. In this talk, we present the devel-

opment of the DCS Controller, the results from the first test chip and the FPGA implementation.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **12**   Type: **Oral**

The lpGBT PLL and CDR Architecture, Performance and SEE Robustness

Friday, September 6, 2019 9:00 AM (25 minutes)

This paper presents the design, architecture and experimental results of the ljCDR (Low Jitter CDR) in the lpGBT (Low Power Gigabit Transceiver). The chip includes a low noise radiation-tolerant integrated LC-oscillator with a nominal frequency of 5.12 GHz to support a 10.24 Gbps uplink and a 2.56 Gbps downlink CDR. The CDR employs a novel loop architecture with a high-speed feed forward loop stabilization. The circuit was fabricated in a 65 nm CMOS technology and has been tested experimentally with heavy ions from 10.0 MeV.cm²/mg up to 62.5 MeV.cm²/mg.

Summary

Future upgrades in high-energy physics experiments such as the ATLAS, CMS, ALICE or LHCb detectors at CERN require ever-increasing data throughputs to collect tremendous amounts of data, leading to exciting discoveries in fundamental physics. In this work, the design and testing of the timing generator for the lpGBT chip are discussed. As the lpGBT will be installed close to the inner detectors, it is designed and tested for a radiation tolerance up to 200 Mrad.

In serial communication modules, the timing reference is generated by a high-speed phase-locked loop (PLL) for uplinks. For downlinks, a Clock and Data Recovery circuit recovers the high-speed clock from the data stream. The ljCDR, which is included in the lpGBT, supports both operation modes with an integrated oscillator at 5.12 GHz. For data transmission, double data rate is used to generate 10.24 Gbps data. The CDR has a dedicated frequency detector to enhance the pull-in range of the CDR loop and features gear-shifting to enhance the lock-time. The VCO was hardened by-design by using a varactor tuning topology at the cost of a reduced frequency modulation bandwidth, which can potentially destabilize the loop, especially in CDR mode. However, this was overcome by including a dedicated feed-forward cancellation that stabilizes the CDR loop and reduces the limit cycle jitter of the PLL. TID tolerance of the design was ensured by using enclosed layout devices (ELT) and/or large devices in analogue blocks. High-speed digital blocks were implemented with CML logic. Triple Modular Redundancy was employed in all digital circuits where state machines are present such as the feedback divider or the phase-frequency detector to protect against SEUs.

The lpGBT test system was used to characterize the prototypes. The LC-oscillator phase noise performance is -110 dBc/Hz at 1 MHz offset. With a low-noise reference clock, the ljCDR provides RMS jitter performance of better than 1 ps in PLL mode and 2 ps in CDR mode. During operation, the circuit power consumption is 50 mW (PLL mode) and 70 mW (CDR mode), respectively.

During a test campaign at the Heavy Ion Facility in Louvain (Belgium), the circuit was characterized for sensitivity to single event effects at different LETs. To understand the root cause of the observed effects a further test campaign using Two-Photon-Absorption laser scanning was completed. Detailed results will be presented at the conference.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **13**   Type: **Oral**

First experimental results on TOFHIR readout ASIC of the CMS Barrel Timing Layer

Wednesday, September 4, 2019 9:50 AM (25 minutes)

The CMS Detector will be upgraded for the HL-LHC to include a MIP Timing Detector (MTD). The MTD will consist of barrel and endcap timing layers, BTL and ETL, respectively, providing precision timing of charged particles. The BTL sensors are based on LYSO:Ce scintillation crystals coupled to SiPMs with TOFHIR ASICs for the front-end readout system. A resolution of 30 ps for MIP signals at a rate of 2.5 Mhit/s per channel is expected at the beginning of HL-LHC operation. We briefly overview the design of the MTD BTL and present first measurements with silicon samples of the TOFHIR ASICs.

Summary

The MIP Timing Detector (MTD) will provide timing of charged particles with high precision allowing to extend to the time domain the association of charged particles to the ˜200 concurrent proton collision vertices occurring at each bunch crossing in the High-Luminosity LHC (HL-LHC). In the barrel section, the Barrel Timing Layer (BTL) is a thin standalone detector based on LYSO:Ce crystals read-out with silicon photomultipliers (SiPMs). The individual cell consists of a crystal bar associated to two SiPMs in both ends. The full BTL detector has about 330 thousand SiPM channels.

The readout the SiPMs uses the new TOFHIR chip optimised for timing performance at high rate with low-power dissipation. Each ASIC channel contains independent amplifiers, discriminators, time-to-digital converters and charge-to-digital converters. The input pre-amplifier provides a low impedance input to the sensor's current signal. The input current is replicated into three branches for timing, energy discrimination and charge integration. Pulse filtering in the TOFHIR chip was developed to mitigate the deterioration of time resolution due to the large SiPM dark noise induced by radiation.

A preliminary evaluation of the ASIC prototypes has been made. Digital communication with the chip was established, the configuration cycle was validated, as well as event triggering and data transmission using external test pulses. The assessment of the 10-bit 10 MHz SAR ADC developed in TOFHIR was made using a dedicated test input to scan the ADC input voltage. Good linearity of the ADC is observed. The measured ADC noise is 0.8 LSB. The TDC assessment was made using external test pulses shifted in time in steps of 300 ps. The timing scan shows the expected linearity of the TDC. The TDC time quantization bin size was confirmed to be 20 ps. The TDC time resolution was estimated by measuring the time difference between two channels triggered by a common digital test pulse. From these measurements, we estimate a TDC time resolution of 15 ps.

First tests with SiPM signals at TOFHIR1 input have been performed. Using the SiPM HPK S12572 operated at over-voltage 4 V and laser pulses with about 1000 p.e., the measured time resolution of the full channel is 20 ps, consistent with the expected timing performance of the ASIC. A total static power consumption of 220 mW was measured in TOFHIR1 (16 channels) corresponding to 13.8 mW per channel, which compares well with the simulation expectation (13 mW).

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **14**   Type: **Poster**

ATLAS Level-0 Endcap Muon Trigger for HL-LHC

Thursday, September 5, 2019 4:55 PM (20 minutes)

The design of the Level-0 endcap muon trigger system for the ATLAS experiment at HL-LHC and the status of the development are presented. The new system reconstructs muon candidates with an improved momentum resolution by combining signals from various subdetectors. The trigger efficiency is estimated with Monte-Carlo simulation to be >90%. The trigger rate is also estimated with proton-proton collision data overlaid with one another to account for a pileup condition at HL-LHC. Track reconstruction hardware based on pattern matching is demonstrated with Virtex UltraScale+ FPGA. The bit error ratio of the data transmission and the power consumption are evaluated.

Summary

The design for the Level-0 endcap muon trigger of the ATLAS experiment at High-Luminosity LHC (HL-LHC) and the status of the system development are presented. HL-LHC is planned to start the operation in 2026 with an ultimate instantaneous luminosity of 7.5 x 1034 cm-2s-1. In order to cope with
the proton-proton collision rate higher than that of LHC, the trigger and readout systems need to be replaced. The new Level-0 endcap muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping the efficiency. That
can be achieved by exploiting the evolution of data transmission technologies to collect signals from various subdetectors in the counting room and form more offline-like tracks. The subdetectors include thin gap chambers, resistive plate chambers, micromesh gaseous detectors, and scintillator-steel
hadronic calorimeters. The combined muon track reconstruction is demonstrated with Monte-Carlo simulation samples produced with the condition at HL-LHC. The efficiency is estimated to be greater than 90%, which is a few percent higher than the current system. The trigger rate is evaluated with proton-proton collision data taken with random trigger overlaid with one another in order to account for a pileup of 200, which is expected at HL-LHC. The obtained value for momentum threshold of 20
GeV, the primary threshold assumed for single muon trigger, is about 30 kHz, which constitutes only about 3% of the assumed total Level-0 trigger rate of 1 MHz. The hardware implementation is planned with ATCA blades. Each blade is designed to have a Virtex UltraScale+ FPGA with approximately
hundred pairs of GTY transceivers, which can be used to receive the detector signals, and with huge memory resources suited for the track reconstruction. The track reconstruction is based on a pattern matching algorithm using the detector hits and the predefined lists of hits corresponding to tracks. A
memory resource of UltraRAM integrated in the FPGA is exploited to store the predefined lists of hits. An initial test with the evaluation kit VCU118 shows a high efficiency and angular resolution better than the requirement. The bit error ratio of the data transmission with GTY transceivers is evaluated
with transfer rates up to 25 Gbps. The power consumption of hundred pairs of transmitter and

receiver of GTY running with 10 Gbps, which is an average transfer rate assumed for the system, is evaluated to be about 30 W.

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Session Classification: Posters

Track Classification: Trigger

Contribution ID: **15**   Type: **Poster**

A custom FPGA mezzanine card for crosstalk measurements of low-mass cables for the high luminosity upgrade of the ATLAS Pixel detector.

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The ATLAS Inner Detector will be completely replaced by an all silicon tracker for the LHC upgrades in the mid 2020s. The increased resolution and data output rate of the innermost layers of the upgraded detector will require more cables that are low-mass and capable of multi-gigabit transmission.

An FPGA Mezzanine Card (FMC) was developed to interface with an FPGA and a cable bundle to measure crosstalk and bit error rate. We present the design of the cable bundle and the FMC, as well as the firmware used to drive the data and measure bit error rate.

Summary

The LHC will undergo upgrades in energy and luminosity in the mid 2020s. The ATLAS Inner Detector will be completely replaced by an all silicon tracker, and a new Pixel readout chip will be developed with decreased pixel size in the innermost layers to increase resolution, as well as an increase in data output rate from 160 Mbps to multi-gigabit transmission.

More readout channels in the detector will require more cables to transmit data on- and off-detector. The cables must be low-mass to fit in the limited space of the detector, as well as to minimize material within the volume. The high radiation environment precludes the use of optical links within the innermost layers. Twisted pair is being explored as an option for electrical data transmission in this region.

Multi-gigabit transmission on small gauge cables was tested previously at the Santa Cruz Institute for Particle Physics [1]. Electrical pickup was measured on a single 36 gauge twisted pair cable as a function of distance from an aggressor cable. A promising performance of 5 Gbps transmission was observed. One cable was driven at a time and a nearby cable probed for pickup. In a cable bundle, many cables are transmitting data that is not necessarily coherent. Confirmation is required that significantly more cross-talk does not result. The response of a differential configuration to crosstalk under these conditions is also of interest. Thus a testing scheme involving FPGA driven LVDS transmission across of bundle of 8 cables is presented in this poster.

An FPGA Mezzanine Card (FMC) has been developed to interface with an FPGA and a bundle of eight 36 gauge cables with drain wire and aluminum foil shield. This poster presents the design of the hardware for this test setup including the cable bundle and the FMC, as well as the development of the firmware to drive data streams along cables and to measure bit error rate introduced by crosstalk.

[1] https://indico.cern.ch/event/357738/contributions/848863/

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **16**   Type: **Oral**

Versatile firmware for the Common Readout Unit (CRU) of the LHC ALICE experiment.

Thursday, September 5, 2019 2:50 PM (25 minutes)

For the next upgrade, the ALICE experiment will use a Common Readout Unit (CRU) at the heart of the data acquisition system. The CRU, based on the PCIe40 hardware designed for LHCb, is a common interface between front-ends, computing system and the trigger and timing system. The 475 CRUs will interface 10 different sub-detectors with 3 sub-systems and reduce the total data throughput from 3.5 TB/s to 635 GB/s. The ALICE common firmware framework is under development. It supports data taking in continuous and triggered mode, clock, trigger and slow control delivery. The architecture and results will be presented.

Summary

The CRU will be located in the data acquisition farm and installed in dedicated computers, namely the First Level Processors (FLP) that are part of the online/offline system (O2).
Each CRU is read out via PCIe gen 3 16 lanes, connected to the front-end electronics with up to 24 bidirectional optical fibers operating at 4.48Gb/s and to the Trigger and Timing System (TTS) with a 10Gb/s Passive Optical Network.

The common firmware of the CRU copes with the various interface requirements of the sub-detectors. The front-ends are read out via GBT in standard or wide bus, and with different protocols: streaming or packet mode. Additionally, some front-ends receive the trigger and timing information from the CRU via the GBT downstream direction, while others have a direct connection to the TTS. The detectors use the GBT downstream connection to relay the Detector Control System (DCS) commands.. These commands are transmitted through the O2 framework, which uses the FLP to send these to the front-end, via the CRU.

In its core, the common firmware performs the detector readout, either in continuous or in triggered mode. The continuous mode differs from the triggered mode, in the sense that all data are transferred unfiltered through the CRU to the FLP memory where it will be further processed and shipped to the event building nodes. The readout system is designed for continuous readout. However, during commissioning or non-nominal operation conditions, quick recovery from eventual data loss is ensured by performing data stream consistency checks in the CRU and transmission of real time status information to the Central Trigger Processor (CTP). The CTP, which has a full detector view, can then request the CRUs to temporarily throttle the data taking to allow recovery.

For commissioning, but also for long term support during operation, many testing and emulator tools are delivered with the common firmware (fake-data generators, pattern player, trigger emulator).

Apart from the common firmware framework that offers raw readout, the possibility is offered to each detector to integrate its own user logic for pre-processing the data and thus reducing the data throughput. This user logic can be quite demanding in terms of logic resources, especially in the case of the Time Projection Chamber (TPC). Consequently, the resource usage of the common firmware must be minimized to allow user logic to fit in the FPGA.

The common firmware framework provides validated solutions for all these use cases and requirements. The chosen architecture, the various solutions implemented and the results obtained will be presented.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **17**   Type: **Poster**

COLDATA Architecture, Design and Verification

Tuesday, September 3, 2019 5:20 PM (20 minutes)

COLDATA is the third of three chips designed for operation within the Liquid Argon cryostat of the Deep Underground Neutrino Experiment (DUNE). It is the point-of-contact between the warm, external DUNE DAQ system and the cryogenically-cooled Front-end Boards. All information from warm-to-cold and from cold-to-warm passes through COLDATA. As such, it implements data concentration and frame formation, slow control communication and relay, fast control communication, clock distribution and readout. With so much communication, extensive verification was essential. The following will present the complete COLDATA architecture as well as its unique Verification Plan accomplished following the Universal Verification Methodology.

Summary

The Deep Underground Neutrino Experiment (DUNE) intends to place its front inside a multi-kiloton liquid argon tracking calorimeter located more than a kilometer underground at the Sanford Underground Research Laboratory in Lead, South Dakota. Such an ambitious endeavor required considerable design effort in every area from lifetime and reliability to data transmission and cable mass. Signals from the Time-Projection Chamber are amplified and shaped by the LARASIC, a front end consisting of 16 channels per chip and then digitized by coldADC, a 12 stage pipelined Analog to Digital Converter.

The purpose of COLDATA isS act as the gatekeeper and data concentrator for the front-end chips. As it is immersed in LiAr, the chip is operating at a cryogenic temperature of ~87k. It communicates with the external DAQ system through a minimal set of copper wires, including a differential pair for a 64MHz clock (shared between two COLDATA chips), a differential pair for a fast command (shared between two COLDATA chips), three differential pairs for I2C slow control (SCL, SDAin and SDAout), and two differential pairs for data readout.

The principle responsibilities of the COLDATA are as follows:

1. To generate and distribute 2MHz Sample clocks and 64MHz clocks to each of the coldADC chips.

2. To relay I2C commands and responses to and from the coldADC chips under its jurisdiction and to a neighboring COLDATA chip. It must also respond to I2C commands if those commands are directed at the COLDATA chip itself.

3. To respond to a limited set of fast commands (e.g. reset, calibrate, etc) in a time-sensitive manner.

4. To act as a cryogenic repository for all data to be programmed to the LARASIC chips and to download that data to the LARASIC chips when required by the DAQ system.

5. To capture all data from the coldADC chips and frame that data by sample period in one of several user selectable frame types.

6. Finally, to deliver the captured data to the DAQ system through the two differential readout lines at a rate of 1.28Gbps. The readout frequency is generated from MEMS oscillators located on the front-end boards and a PLL integrated on the COLDATA chip. The data readout signals are driven across 25+ meters of copper cable by CML drivers also integrated on the COLDATA chip.

The development of COLDATA comes after extensive transistor cryogenic lifetime analysis of available technologies and the design of complete libraries based on design rules extracted from the lifetime analysis. The verification of the COLDATA chip was quite extensive, simulating all man-

ner of changing, real-life scenarios. This was made possible through the Universal Verification Methodology and System Verilog Assertions. In particular, since the COLDATA must communicate with coldADCs and other COLDATA chips, the novel approach was taken to treat the entire front-end board as the device under test and simulate genuine communication between all of these chips rather than verifying a single COLDATA chip as would by more typically done.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **18**   Type: **Poster**

VMM3a, an ASIC for tracking detectors

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The VMM3a is a System on Chip (SoC) custom Application Specific Integrated Circuit (ASIC). It will be used as the front ASIC for both Micromegas and sTGC detectors of the ATLAS Muon New Small Wheels upgrade at CERN. Due to its highly configurable parameters, it has been proposed a variety of tracking detectors and another experiments. It is fabricated in the 130nm Global Foundries 8RF-DM process. The ASIC integrates 64 independently configurable channels each providing amplitude and timing measurements, in digital or analog format. The design aspects and performance of the VMM3a as a production ASIC will be presented.

Summary

he VMM front-end ASIC is being developed since 2012 by Brookhaven National Laboratory for the upgrade of the ATLAS Muon Spectrometer. The 4th version, VMM3a, has been validated to fulfill the upgrade requirements for both sTGC and resistive MicroMegas detectors of the New Small Wheel upgrade which is a 2.4 Million channel system featuring two detector technologies providing trigger and tracking data. ATLAS has submitted the production of 70,000 chips for the upgrade of its Muon Spectrometer. The ASIC features an amplifier which can operate with a wide range of input capacitances, has adjustable polarity, gain and peaking time. It features 64 channels with 160,000 Mosfets each, providing charge amplification, discrimination, neighbour logic, analog-to-digital conversions, and either direct output for trigger or multiplexed readout within a data-driven readout system. Three readout modes have been developed allowing the ASIC to be used in several applications. The ASIC has been tested with resistive MicroMegas and sTGC production modules as well as prototypes in test beam campaigns at CERN. The architecture of the ASIC will be presented along with its performance. Results with detectors from the test beam campaigns will be presented along with results from the production. Moreover highlights of the integration of a 2.4 Million channel system upgrade will be shown.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: 19   Type: **Oral**

Upgrade of the ATLAS MDT Readout and Trigger for the HL-LHC

Wednesday, September 4, 2019 2:25 PM (25 minutes)

The luminosity increase of the LHC in Phase-II calls for an in-depth redesign of the entire MDT readout chain. While the high rate of primary detector signals requires increased bandwidth at each level of the data path, the MDT readout must, in addition, supply accurate coordinate information to the trigger system, leading to more reliable identification of high-pT tracks. The pre-selection of muon hits in the presence of large backgrounds from ⬚ and neutron conversions requires high-speed processing power as well as fast data links, capable to supply the relevant information to the MUCTPi inside the latency of 10 micros

Summary

The upgrade of the MDT readout electronics for the Phase-II of LHC operation must improve the present readout architecture with respect to two main requirements. First, the data path of the readout from the MDT front-end up to permanent storage has to be tailored to the increased data rates at HL-LHC. Second, the MDT readout has to act as a secondary data source for the Level-1 trigger system, providing accurate track coordinates to improve the final Level-1 trigger decision. In the new readout architecture, as presented in the Muon TDR, bandwidth and performance have been increased at all stages of the readout chain. At the front-end, new ASICs have been developed for ASD and TDC. Due to newer chip technology, the ASD performance could be improved with respect to peak time, noise and equality of thresholds among the 8 channels; the architecture of the TDC has been optimized for high data throughput by implementing separate FIFOs for each channel and the bandwidth of the data link to the on-chamber data concentrator (CSM = Chamber Service Module) has been increased from 80 to 320 Mbit/s. At the next level of readout, communication and data transfer between CSM and processors in USA15 now go via GBT.

At the rear-end, the data stream is split, one going to final storage (FELIX), the other to the Level-1 trigger system, where MDT data are used to refine the selectivity for high-pT muons. This refinement is based on the much higher accuracy of the MDT hit coordinates (~0.1 mm) compared to the ones supplied by the primary trigger chambers (20-30 mm), leading to a more accurate pT-estimate and a reduction of the single muon triger rate by about a factor 3.

The selection of muon hits out of a vast majority of background hits from converted ⬚s and neutrons must be performed inside the available latency and requires considerable high-speed processing power. The low-resolution coordinates supplied by the trigger chambers are used as seed for Regions of Interest (RoI). Only hits in a RoI are considered, which leads to a large reduction of the relevant data volume. Hits in a RoI are tested for alignment with the coarse track direction supplied by the trigger chamber. If consistent, the corresponding precision coordinates are sent back to the trigger logics, where a better pT-definition of the muon candidate is derived.

The exchange of information between MDT, trigger logics and RPC/TGC requires fast links, while the identification of tracklets in the RoI needs fast processors and firmware, which is robust against all possible hit patterns.

The present muon trigger could not benefit from the accuracy of the MDT coordinates, because data transmission and processing could not be executed inside the available latency (3 micros). With the 3 times longer latency in Phase-II and with the speed increase for processors and data

links, achieved in the last two decades, this concept can now be put into reality and will be described in more detail in the presentation.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: **22**   Type: **Poster**

A Fault-tolerance Readout Network for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

Thursday, September 5, 2019 4:55 PM (20 minutes)

A high-density electrode array is being developed for Neutrinoless Double-Beta Decay search in high-pressure gaseous TPC. A sensor, Topmetal-S, is designed to have mm-sized electrode, followed by an amplifier and an ADC based on a 0.35um CMOS process. The Topmetal-S array can collect charge directly without gas avalanche gain to achieve high energy and spatial resolution simultaneously. To realize a ton-scale TPC, approximately one hundred thousand Topmetal-S need to be laid on a meter-sized plane. The greatest challenge is a reliable high-density channels readout. A distributed, self-organizing and fault-tolerance readout network is implemented and will be integrated into the Topmetal-S.

Summary

Among the current and planned experiments of neutrinoless double-beta decay (0νββ), the high-pressure gaseous TPC stands out for its excellent energy resolution, very low radioactive background level and good scalability. Moreover, high position resolution can be maintained with an appropriate charge readout scheme for gaseous TPC to further suppress the background through ionization imaging. A pixelated charge readout plane without gas-electron avalanche is desirable. Based on a 0.35um CMOS process, a low noise sensor, Topmetal-S, is being developed which, even without gas gain, the energy resolution requirement could be met. Since 0νββ tracks are extended to tens of cm in length in high-pressure gas, Topmetal-S is designed to have mm-sized charge collection electrode, followed by a charge sensitive amplifier and an ADC in the first prototype. However, to realize a ton-scale high-pressure gaseous TPC, approximately one hundred thousand Topmetal-S sensors need to be laid on a meter-sized plane. The greatest challenge is a reliable high-density sensor readout and sensor control. It is practically impossible to route data channels and control channels directly from each sensor to the edge of the plane. It is also difficult to guarantee air tightness by draw high density channels out of the TPC.

This paper proposed a distributed, self-organizing and fault-tolerance readout network. As a node of the network, each Topmetal-S integrates a router. The scheme establishes local connection between nearby sensors to form a sensor network. Each sensor not only generates and transmits their own data, but also forwards data from nearby sensors, and data packet is finally received by a computer that is connected at the edge of the network. In order to simplify the complexity of router, 2D-Mesh is chosen as the topology of the network. A distributed routing algorithm, Fault-Tolerance-XY (FT-XY), is implemented. The distributed routing algorithm relies only on local information, which makes it possible to integrate the router into the sensor, thus no additional radioactive material will be introduced into TPC. The routing algorithm is also fault-tolerant, so that failed sensors will not disable a large section of the network. Faulty node detection is implemented by sending test packets by the computer. After fault detection, through configuration the computer will form a set of rectangular region called faulty blocks to contain detected faults. The FT-XY routing follows the regular XY routing until the packet reaches a boundary node of a faulty block. At that point, the packet is routed around the block clockwise to pass through. We first completed the logic design of the router using verilog. The simulation shows that the throughput

of the readout network reaches 11641 Mbit/s and the latency of the network is less than 120 us. Then we verified and tested the design on the FPGA. We are now implementing the router on a 130 nm CMOS process and expected to be submit it in June 2019. The details of the routing algorithm, the fault detection scheme, the micro-architecture of the router,will be presented.

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Presenter: XIAO, Le (Central China Normal University)

Session Classification: Posters

Track Classification: ASIC

Contribution ID: **23**   Type: **Oral**

Implementation of a RD53A readout chain using FELIX system and the PiLUP board

Thursday, September 5, 2019 11:30 AM (25 minutes)

RD53A is the first prototype of RD53, the pixel detector front-end chip that will be used by the AT-LAS and CMS experiments at CERN during HL-LHC, starting operation in 2026. It is implemented using 65 nm technology and it transmits data using up to four lanes running at 1.28 Gbps each. This presentation will describe the implementation of a first readout chain of the RD53A using the ATLAS FELIX card. The readout chain features a third card, called PiLUP, as a protocol converter between RD53A and FELIX, with direct communication planned in future revisions.

Summary

To improve physics reach and overcome the challenge of the increasing luminosity of High Luminosity LHC (HL-LHC), the ATLAS experiment will undergo a major upgrade programme. For the Pixel Detector there are three key factors required: the increase of spatial resolution, the ability to withstand a very high radiation dose and to transmit at high bandwidth. A research programme aimed at fulfilling all the aforementioned requirements led to the development of RD53, a pixel detector front-end chip realized using 65 nm CMOS technology. While the final implementation of the chip has not been completed a first prototype, called RD53A, has been produced and is currently being tested.

To maximize chip testing efficiency and to drive development of the Data AcQuisition (DAQ) chain to be used by ATLAS at HL-LHC, it is extremely important that, even for the first prototypes, the DAQ chain is as similar as possible to the final intended design. For the ATLAS experiment, the HL-LHC readout chain will be implemented using the Front-End LInk eXchange (FELIX) card as the first layer of off-detector electronics. This presentation describes the implementation of a first DAQ structure for the RD53A chip using the FELIX system. At this early stage, the FELIX and RD53A cannot be interfaced directly. The currently FELIX implementation, aimed in the first instance at upgrades to be installed earlier than HL-LHC, communicates via optical fibers through either a 4.6 Gbps GBT protocol or a custom 9.8 Gbps protocol known as FULLl Mode protocols. RD53A communicates via Display Port (DP) connectors through 160 Mbps GBT E-link (input) and four lanes 1.28 Gbps Aurora 64/66 protocol (output).

In order to bridge the two systems for the purposes of the demonstrator another board, called PIxel detector high Luminosity UPgrade (PiLUP), is therefore used in the chain. The PiLUP handles both the FELIX-to-RD53A data-path (downlink) and the RD53A-to-FELIX path (uplink). This is done through different firmware blocks: the GBT_FPGA block, the TTC_Encoder, the Aurora Decoder, the Protocol Converter block and the Full_Mode encoder. The GBT FPGA block decodes the GBT-formatted data from FELIX, containing the configuration commands for the RD53A chip, and also synchronizes to the FELIX clock, recovering it from the data-stream. Both configuration commands and clock are then propagated to the TTC Encoder firmware block, which is in charge of converting the commands to a RD53A compatible format and of encapsulating them in a single 160 Mbps serial line, connected to one of the DP connector data lanes. Concurrently the PiLUP receives and decodes Aurora 64/66 data from the RD53A chip, coming from the other four data lanes of the DP connector. Those four lanes of 1.28 Gbps data (resulting in a total throughput of 5.12 Gbps) are then passed to the Protocol Converter firmware block, which merges them into a single FULL Mode stream that is transmitted to Felix via optical connection.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **24**   Type: **Poster**

A High Speed Programmable Analog-to-Digital Conversion System Based On System in Package

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The nEXO project is designed to search for the 0νββ process of 136Xe. It requires high reliability and small volume in the readout electronic system. This research is to improve the integration and the reliability of the circuit. The core chip of the system is a highly integrated programmable chip based on SIP which include two ADC dies and a FPGA die. The complete system is constructed by adding the corresponding circuit, and it has the functions of dual-channel high-speed data sampling, data assembly, communication, and real time data processing.

Summary

The search for the 0νββ process is one of the most important experiments in the field of neutrinos. The purpose of Enriched Xenon Observatory (EXO) experiment is to find the 0νββ process of 136Xe. EXO-200TPC is the prototype detector of EXO experiment. Since June 2011, 136Xe has been discovered for the first time. On the basis of EXO-200TPC, the EXO cooperation group is actively promoting the nEXO project and continuing the search for the 0νββ process of 136Xe. nEXO experiment puts forward high requirements for the reliability and volume of electronic design. The purpose of this research is to improve the integration and the reliability of the circuit design by packaging two ADC dies and a domestic FPGA die together based on SIP technology. The high-speed ADC chip and the domestic FPGA chip are both developed in China, and they are both very high performance chips. We first made a testing board to make sure that the domestic FPGA has the ability to receive the 14 channels'high speed data stream. And it was confirmed that the ISERDES of the domestic FPGA is qualified for this data receiving task. And then here's some details of how to package these two high-performance chips into a small one, we used eight layer substrates with the material of BT HL832NX, and interconnected in any layer of the structure. The flip chip pad pitch is 203um while the diameter of the flip chip pad is 150um. Then the methods of the packaging are SMT + FLIP CHIP + WIRE BONDING. The size of the final module is 35mm*35mm, and the thickness is 2.9mm. With this chip as a core, a complete front-end data sampling system can be constructed by adding the Front-End amplifier Chip (FEC), the back-end serial communication network port and the corresponding power supply module. The details of the system and performance test result will be contained in the article. Overall, compared with traditional PCB design, the SIP-based design reduces the volume of the whole system and increases the reliability of the circuit design. From this research, first we provide a new design way of the readout system for nEXO, and second we can get a highly integrated high speed programmable ADC chip which can be used in any other situations.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **25**   Type: **Poster**

Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase-II upgrade

Tuesday, September 3, 2019 5:20 PM (20 minutes)

A serial power scheme will be used for the new inner tracking detector for the Phase-II upgrade of the ATLAS experiment. New elements are required to operate and monitor a serially powered detector, including a detector control system (DCS), constant current sources and front-end electronics with shunt regulators. A demonstrator for the outer barrel is built at CERN to verify the concept and operate multiple serial power chains. This includes all required elements from an interlock system to in-situ monitoring with the new DCS. In this talk we present how serial chains with up to 16 modules can be operated.

Summary

A new full-silicon tracker is in development for the ATLAS Phase-II upgrade which will be installed for operation at the High-Luminosity LHC. The pixel part will have about 10 times more modules than the current detector. The modules will be powered in series to reduce material and power loss in the services. The serial powering requires new approaches for powering and monitoring of the pixel modules. A demonstrator for the outer barrel part is being built and tested at CERN. This demonstrator includes all elements from pixel modules, the detector control system (DCS) and interlock, to power supplies and readout systems. It will include multiple serial power chains with up to 16 modules in one chain. The Front-End (FE) chips used for the demonstrator are the ones currently in use at the innermost layer of the current ATLAS pixel detector. They include the required shunt low drop out regulator (SLDO) to be operated in a serial power chain. In total 78 FE chips will be installed in the demonstrator with 14 quad modules and 32 double modules. In this talk we will focus on the operation and monitoring of the serial power chains in the demonstrator. The interlock system is a hardwired system that acts directly on the power supplies in case of an undetected failure. The DCS is used to supervise the detector and includes the Pixel Serial Power Protection (PSPP) chip. The PSPP is located parallel to the modules and monitors the temperature and voltage of the modules. It digitizes locally the monitored values and can be read out through an independent communication path. Furthermore a bypass included in the PSPP allows deactivating a single module in the chain while the remaining chain remains operational. This is used as a protection in case a single module should fail. The DCS computer runs a WinCC application, which collects the data from the PSPP and monitoring of the interlock signals. Also the power supplies are controlled through the same application. WinCC is the supervisory control and data acquisition (SCADA) system used for the common ATLAS DCS. Constant current sources are required to operate the serial power chain. A prototype for such a source is developed by an industry partner. The system is operated in as realistic conditions as possible, including the cable length of 100m. As a last element, the DCS interacts also with the cooling system. We will present the building, the system and the challenges faced in operation.

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Session Classification: Posters

Track Classification: Power, Grounding and Shielding

Contribution ID: **26**   Type: **Oral**

Module and System Test Development for the Phase-2 ATLAS ITk Pixel Upgrade

Tuesday, September 3, 2019 4:30 PM (25 minutes)

The ATLAS Inner Detector will be replaced by an all-silicon system, the
Inner Tracker (ITk) and its innermost part will consist of a pixel detector.
Different silicon sensor
technologies will be employed in its five barrel and endcap layers. Components for structures with multiple modules based
on FE-I4 front-end chips were produced and are in assembly and evaluation.With the arrival of the first readout chip prototype, the RD53A chip, the development of hybrid detector modules is starting to address numerous production issues, understanding of which will be crucial for the layout and production of the final ITk pixel detector modules

Summary

For the high luminosity era of the Large Hadron Collider (HL-LHC) it is foreseen to replace the current inner tracker of the ATLAS experiment with a new, all-silicon detector to cope with the occurring increase in occupancy, bandwidth and radiation damage. It will consist of an inner pixel and outer strip detector aiming to provide tracking coverage up to $|\eta|=4$. The layout of the pixel detector is foreseen to have five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward region. This results in up to 14 m. of silicon depending on the selected layout.

Detector requirements in terms of radiation hardness and occupancy, as well as thermal performance depend strongly on the distance from the interaction region. Therefore, the innermost layer will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from 100μm to 150μm. All hybrid detector modules will be read out by novel ASICs, implemented in 65nm CMOS technology and thinned to 150μm, which will be connected to the silicon sensors using bump bonding. With about 4 104 pixels per cm. the bump bond density is a much higher than in previous hybrid detectors.

With the recent availability of the first prototype readout chip, the RD53A, module development for the ITk Pixel Detector is entering a new phase. Numerous modules will be assembled to test the performance of bump bonding of objects of realistic area, very small thickness and high bump bond density, as well as to finalize studies of the module performance with pixel pitches of 50x50μm. and 25x100μm. on the sensors. Flex circuits are glued on top of thenmodules for connection and routing of services which have to be qualified too. Moreover, tests of the new serial powering scheme for low voltage supply of the modules will be done
as part of the prototyping program. The quality assurance criteria for the production of the final detector modules are verified, including mechanical properties like module flatness as well as electrical tests of the functionality of the modules and the bump bond quality.

In addition, a large prototyping programme on system test level is ongoing within the ITk pixel detector community. Components for larger structures with multiple modules based on the FE-I4 front-end chips were produced and are in assembly and evaluation. By this the

system integration and design is prototyped and validated.
The paper will present the latest results from the assembly and characterization of the prototype modules. Important qualification steps of the module design will be discussed. Moreover, latest evaluation and results of thermo-mechanical prototypes and fully electrical prototypes are presented and the system-relevant aspects highlighted.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **27**   Type: **Poster**

Triggering on electrons, photons, tau leptons, jets and energy sums with the CMS Level-1 trigger

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Results from the Phase 1 Upgrade of the CMS Level-1 Calorimeter Trigger are presented. The upgrade was completed before the 2016 data-taking and the system served until end of Run II in 2018. The hardware uses Xilinx Virtex-7 690 FPGAs and 10 Gbps optical links and operates in microTCA chassis. Innovations are introduced, such as embedded linux on trigger processing boards and simultaneous eye-scans on data links. The final stage architecture is time-multiplexed. The focus will be on calorimeter trigger algorithm design and their firmware implementation. Precise FPGA floorplanning allows placing of all calorimeter trigger algorithms in a single board.

Summary

The LHC has resumed operations since the spring of 2015. During Run II, the instantaneous luminosity is already exceeding the design parameters of the machine. To maintain acceptance for proton and heavy ion collision events of interest without exceeding the 100 kHz limit, the CMS Level-1 (L1) trigger has been upgraded. The L1 calorimeter trigger, which finds electrons, photons, tau leptons, jet candidates and computes energy sums, has been upgraded. In these intense conditions, dedicated pile-up mitigation techniques have been implemented in order to reach acceptable performance. Modern technologies offer an effective solution to achieve these goals. The upgraded system makes use of new Xilinx Virtex-7 based AMC cards form the microTCA technology.

The final stage of the upgraded architecture implements an innovative approach called the Time-Multiplexed-Trigger (TMT). Higher granularity inputs, algorithms operating on a wider field of view allow for improved position and energy resolution of regional and global quantities. Calorimeter trigger primitive data is transmitted on 1,152 optical links running at either 4.8 Gbps or 6.4 Gbps. This is pre-processed at Layer-1 before being time multiplexed to Layer-2 where each node processes data from the entire calorimeter. Optical interconnects are via 10 Gbps optical links, which allow easy reconfiguration or expansion as required. This has been made substantially easier with the early adoption of Molex Flexplane technology. Data is then de-multiplexed before sequential transmission to the Global Trigger.

Calorimeter Trigger Processor, Virtex-7 (CTP7) AMC cards serve as the Layer-1 pre-processors, and MP7s serve as the Layer-2 Master Processor nodes. This approach is designed to allow for a high processing clock speed of 240 MHz and thus efficient use of logic resources. The fully pipelined firmware approach of the TMT provides an efficient way to localize the processing, reduce the size and number of fan-outs, minimize routing delays and eliminates register duplication. All calorimeter object algorithms are placed and routed into a single board using a precise FPGA floorplanning. The High Level Trigger model inspired the design of the upgraded Level-1 system.

The poster will cover the technological aspects of the Run II calorimeter trigger system emphasizing the many challenges of its implementation and in particular the innovative algorithms proposed. Results of its performance during the 2016–2018 data taking of proton collisions of the LHC will be presented and used to illustrate the experience gained in terms of implementation of complex electronics systems for triggering in HEP. These systems are now used as a baseline for future trigger design. They also rely on the deployment of high-speed optical links and large FPGA processing. The AMC boards designed for this project are aiming towards a standardization of the data processing required for the future LHC electronics systems.

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Session Classification: Posters

Track Classification: Trigger

Contribution ID: **28**   Type: **Poster**

A multi-channel trigger and acquisition board for TDC-based readout: application to the cosmic rays detector of the PolarQuEEEst 2018 project.

Thursday, September 5, 2019 4:55 PM (20 minutes)

In the 2018 summer the PolarQuEEEst experiment accomplished a measurement
of cosmic rays flux in the Arctic. The detector, installed on a sailboat, was based on
scintillation tiles read by a total of 16 SiPM.
A multi-channel board (called TRB) has been designed to process the discriminated SiPM signals providing self-trigger capability and
time-to-digital conversion. It was based on a Cyclone-V Intel FPGA. TDC
conversion has been implemented in FPGA and in a HPTDC chip (as a backup). The board will be described, main
features and performance will be enlightened and, lastly, future
improvements and potential application will be discussed.

Summary

The PolarQuEEEst 2018 expedition have been accomplished in the last summer: a sailboat that
circumnavigated the Svalbard archipelago was equipped with specific instrumentation in order to
perform a set of scientific measurements in the Arctic region. In particular, a cosmic rays detector
have been designed to properly run in those harsh environmental condition so as to measure flux
at
the sea level beyond the 70°N lat. The detector was based on
scintillation tiles read by a total of 16 SiPM, each of them is digitized by applying discrimination
over
a programmable thresholds. Signals are sent, as LVDS standard, to a FPGA-based custom board
aimed to self-triggering and event readout purposes, which is called TRB. The trigger logic is
configurable and implemented within the FPGA. The trigger signal is used as a reference for time-to-
digital conversion of both leading and trailing edges of the 16 inputs, thus measuring time-over-
threshold. TDC conversion is implemented both into FPGA and with Cern HPTDC chip. The latter
was
initially foreseen as a backup solution in case of either excessive power consuption or high FPGA
resources utilization. Afterwards, because of the satisfactory operation of the TDC into FPGA,
HPTDC
has been kept to profit from for calibration and redundancy purposes during the expedition as
well.
TRB is interfaced to GPS navigation system to provide precise time stamp of the events. Trigger,
TDC
and GPS information are packed in formatted event and sent to a commercial RaspPI3+ single
board
computer, aimed to data recording, TRB configuration and detector monitoring using a set of sen-
sors
(pressure, humidity, temperaure, position, etc...). Main hardware elements are: the Cyclone V In-

tel

FPGA, the piggy board hosting the HPTDC, the off-the-shelf piggy board to interface the RaspPi3+ via

USB.

In this document we are going to describe the hardware, major highlights of the FPGA firmware, performances achieved by the system and future possible improvements.

Three features can be outlined as example. First, the FPGA TDC sensitivity which has been restricted

to about 30 ps by or-ing 4 delay steps together and that can be pushed over if needed. Second, the sustainable output data rate, now limited at 60 Mbit/s by the USB connection with the RaspPi3+ that

can be increased by implementing on firmware the already foreseen high-speed transceiver port, runnign at a maximum of about 6 Gb/s. Last, the number of available input channels in this first TRB

version are 32, common to FPGA and HPTDC (only 16 implemented in the FPGA firmware so far); In a

future PCB version channel number could be increased by distinguish among readout-only channels

(via HPTDC) and the ones that should provide self-triggering too (via FPGA).

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Session Classification: Posters

Track Classification: Other

Contribution ID: **29**

Type: **Oral**

The OBDT board: A prototype for the Phase 2 Drift Tubes on detector electronics

Wednesday, September 4, 2019 9:00 AM (25 minutes)

We present here the design and performance of the OBDT board, which is the new prototype built to substitute the CMS DT muon on-detector electronics. The OBDT is responsible of the time digitization of the DT signals, allowing further tracking and triggering of the barrel muons. It is also in charge of the slow control tasks of the DT chamber systems. A prototype of this board has been produced and is being tested both in the laboratory and also in test stands with real DT chambers. The full functionality in real conditions is being evaluated, showing very satisfactorily results.

Summary

The on-detector electronics of the CMS (Compact Muon Solenoid) DT (Drift Tubes) chambers will need to be replaced for the HL-LHC (High Luminosity Large Hadron Collider) operation due to the increase of occupancy and trigger rates in the detector, which cannot be sustained by present system. The OBDT (On Board Electronics for DT) is the new prototype of the electronics that will be attached to the DT chamber, inside the CMS volume. It will be in charge of performing the 1 ns time digitization of the DT chamber signals and the multiplexing for further transmission to the readout and trigger backend electronics. This board is also in charge of the slow control tasks needed by the full DT chamber system.

The OBDT board has been built around a Microsemi Polarfire FPGA which is responsible of the time digitization of up to 240 input signals. It implements a deserialization method which runs at a clock frequency of 600 MHz and allows obtaining a time bin of 0.833 ns. The input data is multiplexed according to certain criteria and forwarded to the output optical link for data transmission to the readout and trigger chains. This prototype of the OBDT board contains two different optical link bidirectional chains. One that goes to a QSFP+ transceiver to the gigabit transceiver embedded on the Microsemi FPGA and is used mainly for outputting the timing data from the OBDT to the backend system. The protocol implemented so far follows the GBT protocol. Another optical link goes through a SFP+ transceiver to the GBTx chip in the OBDT board and is in charge of performing the slow control tasks, serving also as a backup transmission protocol.

The GBTx chip plus a SCA chip in the board allow clock and synchronization reception as well as e-link implementation for the configuration and monitoring of the Microsemi FPGA. Through this link it is also possible to implement the different slow control functionality of the barrel system, such as setting the front end discriminators thresholds and bias values, implementation of the I2C links for temperature monitoring and channel masking, communication to the RPC and Alignment slow control chains and finally, implementation of the test pulse generation mechanisms that allows to perform the DT chamber time measurements calibration.

A prototype of this board has been produced and is being tested both in the laboratory and also in different test stands with real DT chambers. The different functionality of the OBDT board has been verified and the overall architecture has been validated both through specific tests and through cosmics ray data-taking integrated with the rest of the DT systems. The OBDT architecture together with its performance results will be presented in this contribution, showing the goodness of the design for the expected functionality during HL-LHC.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **30**   Type: **Poster**

Readout and Trigger Electronics for the Triple-GEM Detectors of the CMS GE2/1 System

Thursday, September 5, 2019 4:55 PM (20 minutes)

Triple-GEM has been adopted for the GE2/1 upgrade of the forward ⬚muon detector at CMS for the High Luminosity LHC. GE2/1 chambers are segmented in 4 modules. Each module is equipped with the Optohybrid (OH) interfaced to 12 VFAT3 ASICs. The OH uses GBTs for the readout path and is equipped with a Xilinx Artix-7 FPGA for the trigger data processing.

In this presentation we report on our initial developments of the GE2/1 electronics.
We also discuss the hardware, firmware and software developments, results of measurements with the first ⬚demonstrator and outline our production plans.

Summary

Triple-GEM technology has been adopted for the upgrade of the forward muon detector system at CMS for the future
High-Luminosity phase of the Large Hardon Collider (LHC).
GE2/1 subdetector comprises 72 chambers that will be installed after the second LHC Long Shutdown. The main goal of these chambers is to improve muon momentum
measurements and triggering capabilities in the $1.6 < |\eta| < 2.4$ pseudo-rapidity region. GE2/1 chambers are segmented in 4 modules with 12 sectors in each module, and each
sector is composed of 128 radial strips. The strips are read out by the front-end VFAT3 ASIC. It has 128 channels, each with a charge sensitive preamplifier, shaper and a discriminator. Each module is equipped with the Optohybrid
(OH) board that provides the readout and trigger interfaces for 12 VFAT3 ASIC. The OH board uses CERN designed GigaBit Transceivers (GBT) for the readout path. VFAT3 ASICs also provide trigger information that allows OH to build trigger clusters using Xilinx Artix-7 FPGA and transmit them to the back-end Trigger Processor and to the local Cathode Strip Chamber Trigger Motherboard to improve local trigger
efficiency at an early stage of the trigger processing. The back-end electronics will use the ATCA Trigger Processor farm; it will send the data to the Endcap Muon Track
Finder and to the CMS DAQ system.
In this presentation we report on our initial developments of the GE2/1 electronics: the VFAT3 pluggable cards: the Readout (ROB) and GEM Electronic (GEB) boards; and
the OH board. Initial tests of all electronics components with the GE2/1 prototype chamber have been successfully performed in 2019 at CERN. We discuss the hardware,
firmware and software developments, results of measurements with the first demonstrator and outline our production plans.

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Session Classification: Posters

Track Classification:　Optoelectronics and Links

Contribution ID: **31**   Type: **Poster**

Automated assembly of large double-sided microstrip detectors of the CBM Silicon Tracking System at FAIR

Thursday, September 5, 2019 4:55 PM (20 minutes)

The detector module of the Silicon Tracking System (STS) of the Compressed Baryonic Matter (CBM) experiment at FAIR (GSI) consists of large double-sided silicon microstrip sensors with a size up to 124 mm x 62 mm. Due to material budget constraints, the sensors are connected to the read-out electronics by long flexible microcables. As the manual assembly of the modules is time-consuming and difficult, a fully customized in-house bonding machine has been developed which allows for a highly automated detector module assembly. We present the bonding machine together with the electrical characterization of the first modules built with it.

Summary

The CBM experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany, aims to explore the quantum chromodynamics (QCD) phase diagram for high baryon densities. One of the core detectors of CBM is the Silicon Tracking System (STS). It consists of eight tracking stations of double-sided silicon microstrip detectors. Each sensor contains 2048 strips, 1024 strips for n- and p-side, respectively. Sixteen STSXYTER readout ASICs with 128 channels each are connected to one sensor. Because of the very low material budget requirements, the front-end electronics are located far from the sensitive sensor region and are therefore connected by low-mass copper flex microcables. With the help of this double-layered microcable, a novel interconnection technology involving a gold stud –solder paste flip chip process has been developed. It combines low cost and high parallelization capability with good mechanical and electrical reliability and has been presented last year at TWEPP 2018.

The first step in module assembly is the connection of the microcables with the readout ASICs which can be done by a commercial flip chip machine. In the following, eight microcables to ASICs structures are placed side-by-side on the p-side of the sensor. After bonding the p-side of the sensor, the complete structure has to be flipped to allow the bonding of eight more microcables on the n-side. To achieve this much more challenging sensor-side interconnection with high accuracy and high throughput, a fully customized in-house bonding machine is under construction.

In this bonding machine, four highly precise step motors are combined with a dual-camera (top and bottom) pattern recognition system for detecting the sensor and microcables with sub-μm accuracy. In the end, the goal is to achieve a bonding accuracy in the range of a few microns. Additional features of the bonding machine are temperature regulated heating of the bond head as well as the sensor plate, an automated vacuum control system, a camera calibration procedure, and the possibility for automated application of the underfill glue for spark protection between the HV sensor and the LV microcables.

The bonding machine setup, its bonding performance and electrical test results of the first assembled detector modules will be presented.

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **32**   Type: **Oral**

Electronics system of the CMS GE1/1 Muon upgrade and performance of the Slice Test during the 2017-18 LHC Run

Tuesday, September 3, 2019 9:25 AM (25 minutes)

In this contribution, we present the status of the electronics system of the triple-GEM detectors for the CMS GE1/1 upgrade which is being installed in 2019-2020, as well as the performance of ten prototypes which have been operated in CMS during 2017-18. ⬚For this new CMS muon sub-detector, a new front-end chip, the VFAT3, has been designed. The VFAT3 communicates with the back-end microTCA electronics through the GBTx chipset and the versatile link. Each of the 144 triple-GEM detectors has 24 VFAT3s, 3 GBTx chipsets as well as a Virtex-6 FPGA. All powered by 9 FEAST DCDC converters.

Summary

In this contribution, we will present the status of the readout electronics system of the triple-GEM detectors of the GE1/1 system which is being installed into CMS in 2019-2020 (LS2), as well as the performance of the ten "slice test" detectors which were operated in the CMS muon endcap during the 2017-18 LHC run.⬚⬚Ten "slice test" detectors were installed into the CMS endcap in January 2017. These detectors are read out on the front-end using 24 VFAT2 chips and a corresponding v2 optohybrid board, and from the back-end utilizing a microTCA crate containing CTP7 and AMC13 boards. Two of the ten detectors also include temperature sensors, and are powered via a multichannel power supply, as the final GE1/1 detectors will be. Data was recorded throughout the 2017 and 2018 LHC runs. In February 2018 two of these detectors have been replaced by final GE1/1 detectors equipped with the final (called v3) electronics. The overall performance of the slice test detectors recorded over these two years of data taking will be reported in this contribution.⬚⬚Using the lessons learnt from this slice test allowed for the further development of the final GE1/1 v3 electronics which will be used in the LS2 installation. The new detectors are now read out by the VFAT3 chip, which runs at 320 MHz, four times higher than the frequency of the VFAT2 chip, as well as the v3 optohybrid board which is equipped with a Xilinx Virtex6 FPGA and three CERN GBT chipsets. The on-detector electronics is powered via nine CERN FEAST DC-DC converters. In February 2018 two of such v3 detectors have replaced two of the v2 "slice test" detectors. This contribution will report on the improvements made to the electronics in view of the installation of GE1/1 and on the very first results of the final GE1/1 v3 electronics obtained in CMS. We will also report on the performance recorded with GE1/1 production chambers in a large test bench where up to 30 chambers are recording cosmic events during several weeks before being installed in the CMS muon endcap.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **33**   Type: **Poster**

Key Building Block Upgradation and Optimization for High-performance Transceivers: Multimode Interferometers from Conventional to Sub-wavelength Regime

Thursday, September 5, 2019 4:55 PM (20 minutes)

Multimode interferometers (MMI) are key components for high-bandwidth transceivers in upgrading the data transmission of future detector systems. We present 2 conventional high-performance MMIs fabricated on a 250nm SOI platform with different splitting ratios which operate as 50:50 power splitter for Mach-Zehnder modulators and as 86:14 power splitter for loop control in future transceiver designs, respectively. Besides, we present novel MMIs based on sub-wavelength gratings. By engineering the refractive index of relevant sections with sub-wavelength structures, fabricating many-port MMIs with low phase error becomes feasible and also the on-chip footprint of 50:50 MMIs can be decreased dramatically.

Summary

In this paper, we present the complete design process of MMIs starting from theoretical calculation to numerical simulation. According to the phase difference and the power splitting ratio between output ports, MMIs can be used in different scenarios. We fabricated two conventional 2 × 2 MMIs using e-beam lithography on a 250nm SOI platform at IMS Stuttgart. They are used in a p-n depletion Mach-Zehnder modulator (MZM) design and a feedback control circuit design, respectively. The on-chip footprint of 50:50 MMI in our MZM is 4.5 μm × 24.5 μm and the footprint of the 86:14 MMI is 2.8 μm × 14.1 μm. For either device, there is very good agreement between measurement and simulation results with a power splitting ratio deviation of less than 3 percentage points over the entire C band, and the measured maximum insertion loss is 0.7dB.

A conventional symmetric 50:50 MMI with the same width of the asymmetric MMI would require a length of 28.6 μm. By engineering the refractive index of the central part of MMI, the modal phase of even modes is altered while odd modes remain unaffected, by which the required length of the MMI can be shortened dramatically. The refractive index is engineered by using a sub-wavelength structure consisting of 56 square holes etching down to the substrate with a dimension of 60 nm × 60 nm. The resulted footprint of the subwavelength MMI is 2.8 μm × 14 μm, only 36% of our fabricated conventional 50:50 MMI. The simulated insertion loss of the subwavelength MMI is less than 0.15dB in the C band and the power splitting ratio is 50:50 with a power splitting ratio deviation of only 1 percentage points.

As the modal phase error increases quickly with mode number, the output images are not perfectly focused for MMIs with more than 4 output ports. We design subwavelength gratings at the lateral cladding region to lower the refractive index contrast between the core and the lateral cladding and therefore decreasing the modal phase error. The simulated 2 × 4 MMI has a footprint of 7.2 μm × 96 μm and phase error is as low as 16°. This high-performance device enables constructing compact receivers for advanced modulation formats with very high data transmission bandwidths.

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Session Classification: Posters

Track Classification: Optoelectronics and Links

Contribution ID: **34** Type: **Oral**

Downlink Equalization and Eye Opening Monitor in the lpGBT

Thursday, September 5, 2019 11:05 AM (25 minutes)

The architecture and experimental results for the downlink Equalizer (Eq) and Eye Opening Monitor (EOM) circuits in the lpGBT ASIC are presented. The 2.56 Gbps downlink NRZ data is received by a line receiver that is followed by a Continuous Time Linear Equalizer (CTLE) with programmable transfer function. The EOM circuit scans the output of the Eq with a time resolution of 6.1 ps and a voltage resolution of 40 mV allowing to monitor the quality of the data transmission over the channel. Both circuits have been evaluated and detailed test results will be presented at the conference.

Summary

The lpGBT ASIC is a radiation hardened gigabit transceiver. It is used to transmit data, timing and control to the detectors in the LHC experiment. The lpGBT downlink (counting room to the detectors) is typically comprised of a short optical fiber (up to 300 m) transmitting NRZ data at 2.56 Gbps. The light is converted to an electrical signal by a PIN-diode and then amplified by Transimpedance Amplifier (TIA). The length of the electrical link between the TIA and the lpGBT can be from a few centimeters to a few tens of centimeters. To be able to compensate for the bandwidth of the transmission line between the TIA and the lpGBT, a line receiver with programmable equalization (EQ) is used. The Eye Opening Monitor circuit (EOM), that follows the EQ, allows to control the quality of the signal at the output equalizer and to adjust its transfer function for optimum performance. Both circuits are fabricated as part of lpGBT in a 65 nm CMOS process.
The line receiver consists of a programmable attenuator, four equalizing stages and a buffer. As the amplitude of the input signal might be ranging from a few tens of millivolt to 1 V, the programmable attenuator which acts as the first stage of the line receiver allows for the following stages to operate linearly under all conditions. The attenuator is implemented with a passive network, providing three attenuation setting, 0 dB, 3.5 dB and 9.5 dB. A 100 Ohm termination resistor is integrated in the attenuation network. To compensate for the channel loss, each of the equalizer stages is a continuous time linear equalization (CTLE) structure in which the position of the zero is programmable by adjusting the value of resistance and capacitance. The equalizing stages are sized for low power consumption. Enclosed layout transistors (ELT) are used to minimize performance degradation under radiation. The size of the line receiver is 300 X 180 μm2, including the line receiver core circuits, ESD circuits for input and power supply, and decoupling capacitance. The simulated power consumption is below 1.8 mW in nominal condition.
The EOM follows the equalizer and allows to monitor the NRZ signal quality after equalization. It scans the equalizer output signal both in amplitude and time. A reference voltage is used to measure the signal amplitude using a differential comparator with 40 mV resolution. The time sampling resolution is of 6.1 ps and is achieved by interpolation between in-phase and quadrature clocks at 2.56 GHz. The integration of EOM allows to probe the equalizer output and serves three purposes. First, the channel losses vary from case to case making the choice of a fixed equalization non-optimal. Second, since the line receiver is integrated in lpGBT the direct monitoring of the eye diagram is not feasible. Third, the EOM can work together with the line receiver to act as an offline adaptive decision-feedback equalization. Both circuits will be detailed and experimental

results presented at the conference.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **36**   Type: **Oral**

FPGA implementation of a histogram-based parent bunch-crossing identification for the Drift Tubes chambers of the CMS experiment

Wednesday, September 4, 2019 11:30 AM (25 minutes)

The first running implementation on FPGA of a histogram-based trigger primitive generator for the CMS Drift Tubes at the HL-LHC is presented. This project is driven by the need to generate a trigger by processing the charge collection times, acquired by means of a TDC, and asynchronously shipped to the back-end. We review the design of the bunch crossing evaluation, its implementation on FPGAs of the Xilinx UltraScale family by means of High-Level Synthesis (HLS), and the performance of a demonstrator board of such a trigger.

Summary

Here we present the first running implementation of the bunch-crossing identification block of a proposed histogram-based Level 1 Trigger Primitives Generator (L1 TPG) on FPGA for the Drift Tubes (DT) chambers of the Compact Muon Solenoid (CMS) Experiment at the High Luminosity-LHC. The planned upgrade of the front-end foresees an asynchronous data shipping to the back-end, and then requires a novel approach to the generation of the trigger primitives, being the current one directly sampling the detector signals. We designed a Hough Transform-based trigger which features, as a first step, the identification of the parent bunch crossing, followed by the track parameter estimation. The bunch crossing identification algorithm is based on a statistical selection among several parent bunch crossing hypotheses by means of the evaluation of the most voted one in a real-time built histogram.

The bunch crossing identification block was deployed and run on FPGAs of the Xilinx UltraScale family. Our approach in the design was compliant to High-Level Synthesis tools in order to minimise the effort on hardware implementation of the algorithm while closely matching its software emulation within the official framework provided by the experiment. The design was optimised balancing between the large area required to implement high-granularity multi-dimensional histograms and the processing time, by implementing a highly parallelised processing of input data multiplets and reducing to one-dimensional histograms.

We evaluated the performance of the implemented algorithm in terms of required area and latency. The minimal processing unit groups together 18 read-out channels: for such a unit, called macro-cell, the amount of resources needed is approximately 16000 Look-Up Tables (LUT), and the best obtained latency so far is approximately half a microsecond, corresponding to 20 LHC bunch crossings, when covering about a full CMS DT super-layer (21 macro-cells), exploiting a Xilinx VCU440, speed grade -3, clocked at 200 MHz. Hence, the current design, yet provisional and open to improvements, requires an amount of resources comparable to the ASIC processors of the current L1 DT TPG and is compatible with the L1 decision latency budget. The very same design has been tested also on a Kintex KU115, speed grade -2, clocked a 160 MHz, requiring 57% of LUTs and no hard-wired multiplier blocks (DSP) at all. The precision used throughout the algorithm is 3.125 ns, slightly better than the single hit resolution obtained in offline reconstruction, and 4 times better than the current L1 DT TPG.

The comparison between the software emulation of the algorithm and the results of the hardware execution gives negligible mismatch on the very same set of realistically simulated muon tracks, including inefficiencies and pile-up. We also report on the results of a test with cosmic muons collected with a clone of a DT chamber available at the INFN National Laboratories in Legnaro,

and on future improvements of this project.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: **37**   Type: **Poster**

Hardware production quality control for the ATLAS Phase-I readout upgrade

Thursday, September 5, 2019 4:55 PM (20 minutes)

The upcoming upgrade of the readout system of the ATLAS experiment at the LHC at CERN is based on the Front-End LInk eXchange (FELIX) system. As part of this upgrade, approximately 120 custom PCIe cards are being produced by an industrial partner, based on a hardware design developed within the collaboration. Such a large production requires detailed Quality Assurance/Quality Control procedures (QA/QC) to ensure the hardware being produced is fully functional and robust.

Summary

The Front-End LInk eXchange (FELIX), will form a cornerstone of the upgraded readout system of the ATLAS experiment for the newly installed trigger and detector components after the 2018-2021 shutdown. These systems include the new Muon Small Wheel, Liquid Argon Calorimeter digital readout plus Calorimeter and Muon trigger electronics. The FELIX system is composed of approximately 120 custom PCIe cards hosted by a cluster of commodity servers, with point-to-point connections to detector front-ends at the input stage and an output to a high bandwidth ethernet network. The PCIe card itself hosts a Xilinx Kintex Ultrascale FPGA, up to 8 MiniPOD optical transceivers and a high performance 16 lane PCIe Gen 3 interface. The production of the 120 cards is being undertaken by an industrial partner based on designs developed within the ATLAS collaboration. Each card must undergo a rigorous set of QA/QC tests at the production side, and at CERN, before being accepted for operational use. In order to maximuse production yield and minimise hardware faults, the process has been split into two parts. A 20-board 'pre-series' has been produced, and subjected to the full suite of production tests. This step gives the opportunity to refine the production process and iron out any issues, before initiating the final production run for the remaining 100 cards. In this presentation we will detail the development of the testing platform used to validate the pre-series (which will also be used for the final production).

In more detail, the specific tests used to validate the quality and performance of the cards include:
- verification of the operating temperature of the FPGA,
- measurement of power supply and distribution across the card,
- confirm PCIe bus performance and throughput
- confirm ability to program all on-board devices,
- verify quality of the optical connections via Bit Error Rate tests and Eye Diagram inspection,
- synchronization tests via loop-back configuration using all the optical channels (48 fibers) at high bandwidth.

These measures and more have been specified and a full validation suite prepared, making use of scripting and automation to optimise test time and accuracy.
This full suite has been made available to the contractor in a dedicated test server, with the same setup replicated at CERN. By using these two test benches in tandem it will be possible to rapidly and accurately validate and commission the FELIX cards for use in ATLAS operations.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **38**   Type: **Oral**

Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration

Tuesday, September 3, 2019 2:00 PM (25 minutes)

A prototype chip named RD50-MPW2 in the 150 nm High-Voltage CMOS (HV-CMOS) technology from LFoundry has been designed and submitted for fabrication within the CERN-RD50 collaboration. The chip contains a matrix of depleted CMOS pixels with monolithically integrated readout electronics. The focuses of the chip are on improving the readout speed that is achieved by designing high-speed, low-noise readout electronics, and minimising the leakage current and increasing the breakdown voltage of the sensor by optimising the chip layout. The design and initial measured results of RD50-MPW2 will be presented in this contribution.

Summary

The industry standard High-Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments that require sensors with small pixel size, good timing resolution, excellent radiation tolerance and low material budget, such as the Mu3e experiment, future upgrades of the Large Hadron Collider (LHC) and the Circular Electron Positron Collider (C EPC).

As opposed to traditional hybrid silicon sensors that require bump-bonding to assemble the sensing element and the readout chip together, depleted CMOS sensors allow integrating all parts onto one single piece of silicon, thus making this technology efficient in material, production time and cost. A high voltage used to bias the sensor substrate brings the benefits of fast charge collection by drift and high radiation tolerance up to a few 10^{15} 1 MeV neq/cm2.

The CERN-RD50 collaboration is developing depleted CMOS sensors to further improve their performance to meet the requirements of future particle physics experiments. In this work, we present the design of a new prototype chip in the 150 nm HV-CMOS technology from LFoundry, named RD50-MPW2. The chip contains a matrix of pixels with monolithically integrated readout electronics. The focuses of the chip are on improving the readout speed, minimising the leakage current and increasing the breakdown voltage of the sensor, which are achieved by designing high-speed, low-noise readout electronics and optimised chip layout. The RD50-MPW2 also acts as a necessary step for developing a large demonstrator of depleted CMOS sensors that is foreseen within CERN-RD50.

The depleted CMOS matrix includes two flavours of 60 um x 60 um pixels that use different methods to reset the sensing diode. These methods are named the continuous-reset and the switched-reset. Pixels with continuous-reset use a continuous current to reset the Charge Sensitive Amplifier (CSA) after a particle hit, resulting in a processing time (rise plus fall time) that is proportional to the number of electrons collected by the sensor. With this pixel flavour, it is possible to process a particle hit that generates 10k electrons within 90 ns only. Pixels with switched-reset use the output of the discriminator to switch on and off a larger reset current. The switched current resets the CSA in 15 ns and shortens the processing time to 45 ns, independently of the number of collected electrons. As the larger reset current is active for a very short time only, the power consumption is kept low.

The continuous-reset pixel is able to provide both rising and trailing edge time-stamps to obtain the Time over Threshold (ToT). In contrast, the switched-reset pixel can only provide the time of arrival. Post-layout simulations show that both pixel flavours have time resolution better than 15 ns, Equivalent Noise Charge (ENC) around 100 e- and pixel power consumption less than 25 µW.

RD50-MPW2 has been submitted for manufacture and the fabricated dies that will be in 10, 100, 1.9k and 3k Ωcm resistivity substrates are expected in July 2019. The design and initial measured results of the chip will be presented in this contribution.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **39**　　　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

New Quench Detection System to Enhance Protection of the Individually Powered Magnets in the Large Hadron Collider

Tuesday, September 3, 2019 5:20 PM (20 minutes)

To further improve the existing Quench Detection System (QDS) of individually powered magnets installed in the Large Hadron Collider (LHC), a new radiation tolerant electronic board was developed. The board provides three signal acquisition channels able to acquire with different and configurable signal resolution and acquisition rate the analog signals of different properties. These enhancements enable the application of different quench detection algorithms depending on the protected magnet. Additionally, the board can be used with newly developed current derivative sensors for reliable detection of symmetric quenches. The board flexibility allows as well using both open and closed loop current sensors.

Summary

The Large Hadron Collider (LHC) consists of a large number of magnets to steer and focus the beam of particles.
The used magnets are made out of superconducting materials. During their operations with currents, it might happen that one part of the magnet changes its state from the superconducting to the resistive one.
This transition phenomenon is known as a quench.
Due to the often large amounts of stored energy in the magnets, a quench has to be detected by highly reliable Quench Detection Systems (QDS) to trigger appropriate protection actions for the magnet circuits and the removal of the particle beams.
To improve the existing quench detection systems of Individually Powered Quadrupoles (IPQ), Individually Powered Dipoles (IPD), Inner Triplets (IT) and 600 A corrector magnets towards higher availability and reliable detection of aperture symmetric quenches, a new, more generic detection board was designed and built.
To protect the magnets of the LHC, different quench detection algorithms are in use today, depending on the available magnet signals. The classical approach for protection is the measurement of the voltages across the two magnet coils and applying a pre-defined threshold and discrimination time to detect a resistive voltage component. This approach is currently used for quench detection of IPQ, IPD and IT magnets.
To detect quenches of the 600 A corrector magnets only one global voltage and one circuit current measurement is available. For quench detection, the current derivative is therefore calculated numerically to allow for the compensation of the inductive component in the measured voltage signal. To measure the current, an open loop sensor has been used to date. As this sensor type exhibits high noise values, new sensor candidates were selected and evaluated. Out of the evaluated types, a closed loop sensor was identified as the most promising candidate.
Therefore, the new board was designed to allow the use of both sensor types depending on the requirements of the protected magnet and circuit.
To allow for a reliable and fast detection of symmetric quenches in individually powered magnets, a new detection method based on a current derivative sensor was recently developed. This sensor is based on a current transformer approach and is faster than detection methods based on numer-

ically calculated derivatives. The output voltage can be directly read with one of the channels of the new detection board.

To allow for the combination of all the mentioned detection mechanisms and new sensors, the new developed electronic board has three fully independent acquisition channels to acquire three different voltages with different signal levels, bandwidth, resolution and readout speed. Because of the flexibility of the system, a wide range of magnets can be protected.

As the board will be exposed to elevated doses of ionizing radiation of up to 10 Gy/y, all used components were qualified in radiation and can withstand the radiation environment of the LHC over their entire lifetime.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **40**   Type: **Oral**

Realization of a state machine based detection for Track Segments in the Trigger System of the Belle II Experiment

Wednesday, September 4, 2019 2:50 PM (25 minutes)

The Belle II Experiment relies on an online level 1 trigger system to reduce the background and achieve the targeted frequency of 30 kHz. Here the basis for all trigger decisions based on data from the Central Drift Camber is the track segment finding. To improve both efficiency and maintainability we restructured the original combinatorial approach to finite state machines. The new implementation is saving about 20 % of FPGA slices. To achieve high test coverage an automated test framework was developed for design time validation. Operational correctness is achieved by integration in cosmic ray tests.

Summary

The upgraded SuperKEKB collider is designed to achieve a luminosity of $L = 8*10^{(35)}$ cm^{-2}s^{-1}. As a result higher machine background is expected in the attached Belle II experiment compared to its predecessor Belle. The estimated event rates exceed the targeted trigger rate of 30 kHz. One of the major trigger systems employed to achieve this rate is the trigger system of the central drift chamber at the Level 1. Here the basis for all present trigger algorithms is the track segment finder. Its task is to detect regions of active wires in the detector and combine them into track segments, arrangements of neighboring wires that conform to a predefined geometrical shape. The track segment finder is implemented on XC6VHX565T Virtex 6 FPGAs and integrated close to the detector readout. It has to be efficient and operate in low latency to fullfill the requirements of the entire Level 1 trigger system. An combinatorial approach was in operation for the first phases of the experiment. To increase efficiency and maintainability we decided to restructure this implementation to use finite state machines.

The advantages of the new state machine implementation are the easier expandability as well as the lower resource consumption. By reducing resources, we are able to ease the achievement of timing closure for further iterations of the firmware. Additionally we added a mechanism to reduce transmission of redundant data and thus improve operation by employing suppression of neighboring hits. The overall design is reworked to provide a higher degree of flexibility during design time. We incorporated an approach to adjust track segment finding for predefined regions of the central drift chamber by allowing to load partial special finding configurations. This will allow to easily adjust to geometrical regions with broken wires. As this finding mechanism is based on BRAM, we developed an automated dual and single port inference to keep resource consumption to a minimum. In average the new implementation is capable of achieving a reduction of used Slice LUTs of about 20 \%. To validate the new implementation we developed a test framework that allows to generate testbenches that either support target high test coverage or dedicated detector data patterns to investigate special cases. Correctness within the trigger system is shown by cosmic ray tests.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: **41**   Type: **Oral**

High-Precision Luminosity Instrumentation for the CMS Experiment at the HL-LHC

Thursday, September 5, 2019 11:05 AM (25 minutes)

The High Luminosity upgrade of the LHC (HL-LHC) is foreseen to increase the instantaneous luminosity by a factor of five over the present LHC nominal value. The resulting, unprecedented requirements for background monitoring and luminosity measurement create the need for new high-precision instrumentation at CMS, using radiation hard detector technologies. This contribution presents a system using the Tracker Endcap Pixel Detector (TEPX) with an additional 75 kHz of dedicated triggers for online measurement of luminosity and beam-induced background. Real-time implementations of algorithms such as pixel cluster counting on an FPGA are explored for online processing of the resulting data.

Summary

The expected high level of pile-up events at the HL-LHC imposes challenging requirements for the online measurement of luminosity and beam-induced background at the CMS experiment. A new instrumentation system is necessary given the extreme radiation and increased precision goals. Additionally, the space presently used for luminosity instrumentation and background monitors will be occupied by the extension of the Inner Tracker. Thus, in order to provide high precision luminosity and background measurement, the Tracker Endcap Pixel Detector (TEPX) will be employed with 10% of dedicated luminosity triggers in addition to the Level-1 trigger. In particular, the innermost ring of the outermost TEPX disk will have a central role in beam monitoring, as it will be operated as a standalone instrument, independent from the rest of the CMS tracker. Studies have been conducted to simulate the expected luminosity data rates for TEPX, based on a model of the RD53B data encoding and stream building. The results are presented for different readout modes, trigger rates and pileup to account for various operational scenarios. The data corresponding to luminosity triggers will be forwarded from the Inner Tracker Data, Trigger & Control boards (DTCs) to a dedicated luminosity back end. The envisaged system architecture and its implications for the CMS DAQ system are explained. Since luminosity and beam background information are crucial for CMS as well as LHC operations, a prompt and reliable measurement must be provided. This not only implies special demands on the TEPX servicing, but also requires real-time processing of the corresponding data. Therefore, an online implementation of a pixel cluster counting algorithm on an FPGA or System-on-Chip is under investigation, as this algorithm has been proven to give a reliable offline luminosity measurement throughout previous LHC runs.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **42**
Type: **Oral**

CLICTD: A monolithic HR-CMOS sensor chip for the CLIC silicon tracker

Wednesday, September 4, 2019 2:25 PM (25 minutes)

The CLIC Tracker Detector (CLICTD) is a monolithic pixelated sensor chip produced in a 180nm HR-CMOS Imaging Process. The chip, designed in the context of the CLIC tracking detector study, comprises a matrix of 16×128 detector channels, each measuring $300 \times 30 \mu m^2$. To ensure prompt charge collection, each channel is segmented in eight collection diodes, each containing a separate analog front-end. A simultaneous time and energy measurement is performed in the on-channel digital logic. Simulations show a minimum detectable charge of $93e^-$ for 210mW/cm^2 (continuous operation). The main design aspects, as well as the first results from laboratory measurements are presented.

Summary

A novel monolithic pixel sensor chip, the CLIC Tracker Detector (CLICTD) chip, is presented. The chip was designed according to the requirements for the silicon tracker at the future Compact Linear Collider (CLIC). These requirements include an 8-bit Time of Arrival (ToA) measurement with 10ns time bins and a 5-bit Time over Threshold (ToT) measurement for time walk correction and precise hit spatial allocation. Other requirements involve a single point resolution of 7um along the transverse plane, a total material budget of 1-1.5% X0 per detection layer (allowing for ˜200um for the silicon layers) and an average power consumption below 150mW/cm^2. Taking advantage of the low duty cycle of the CLIC beam, the analog front-end can be set to a standby power mode between bunch trains to minimise the average analog power consumption (power pulsing). The digital power consumption is minimised by means of clock gating. The resulting average power consumption over the CLIC cycle is 5mW/cm^2 for the matrix, plus 70mW for the periphery (for 3% occupancy).

The design was implemented in a 180nm High-Resistivity (HR) CMOS imaging process, where a deep P-well is used in order to shield the on-channel electronics from the collection electrode [1]. The signal is collected with a small N-well on the P-type high resistivity epitaxial layer. The small detector capacitance helps to minimise the analog power consumption and the noise in the front-end. The epitaxial layer is fully depleted by including an additional deep N-type implant. Using a process split, additional wafers are produced with a segmented deep N-type implant to increase the lateral field and thereby to reduce the charge collection time.

The CLICTD matrix comprises 16x128 detecting cells of 300x30um^2. Each cell is segmented in eight collection diodes each read out by its own Charge Sensitive Amplifier (CSA) to ensure prompt charge collection. The diodes are therefore spaced by 37.5um along the long direction. Every front-end includes a CSA, a discriminator and a 3-bit local threshold tuning DAC. Simulations show a minimum detectable charge of 93e-, an in-time charge of 720e- (where the time walk remains below 10ns) for 210mW/cm^2 (continuous operation, without power pulsing). Binary hit information is stored for each diode, while the simultaneous 8-bit ToA and 5-bit ToT measurement is performed in the on-channel digital logic for the combined output (by means of an "OR" gate) of all eight discriminator outputs.

The slow control is based on the I2C protocol, while a serial readout at 40 MHz, with a zero suppression algorithm, is employed. The chip was verified using the Universal Verification Methodology (UVM).

Along with the main design aspects, the first laboratory measurement results with the CLICTD

chip will be presented. Measurement results will include a scan of the sensor I-V characteristics, DAC scans and a test of the slow control and readout logic. In addition, the first results on the pixel performance, using internal test pulses as well as a radiation source, will be presented.

[1] W. Snoeys et al., NIMA 871 (2017) 90-96

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Presenter: KREMASTIOTIS, Iraklis (KIT - Karlsruhe Institute of Technology (DE))

Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **43**   Type: **Poster**

CaRIBOu –A versatile data acquisition system based on programmable hardware

Thursday, September 5, 2019 4:55 PM (20 minutes)

CaRIBOu is a flexible data acquisition system for prototyping silicon pixel detectors. The core of the system consists of the Control and Readout (CaR) board, a versatile module providing the hardware environment for various target ASICs, including powering and slow-control infrastructure and high-speed full-duplex GTx links up to 12.5 Gbps. The CaR board connects to a Zynq system-on-chip board, which runs a fully featured Yocto-based Linux and a data acquisition framework (Peary). Using the CaRIBOu system significantly reduces the time required to test and debug detector prototypes by providing ready-to-use peripheries and re-useable software interfaces for a variety of detectors.

Summary

Developing new detectors requires the design of an adequate readout and control system. Such a system typically consist of hardware in form of a readout board containing programmable logic to provide an interface to the chip, power supplies for biasing the detector chip, as well as DACs and ADCs for setting and measuring operation parameters, generating test pulses, etc. One also needs to write software for controlling the detector and hardware peripherals and for data readout. This process needs to be repeated for each new chip developed, which requires different voltage levels or different number of data lines. The CaRIBOu system, on the other hand, provides a robust, versatile DAQ system, which can be easily adjusted to the needs of different detectors. Using such a system therefore saves development cost and reduces the time needed to get first data from the detector. CaRIBOu is a combination of hardware and software modules that forms a stand-alone readout and DAQ system for detector prototypes. It was initially developed for testing newly developed pixel-detector chips for ATLAS and for a future CLIC detector. Adding support for a new chip is a matter of writing a piece of code performing an interface between the chip-specific features and the standard data and control interface of the CaRIBOu system. The system is based on a Xilinx Zynq System-on-Chip (SoC) architecture combining the power of a programmable hardware (FPGA) and a full Linux operating system allowing to run software in a high-level programming language. It can run either stand-alone, storing data to a local filesystem, or connected via network interface to a data storage or a superior control system. The data decoding and analysis can be done either directly in the system both in software and in FPGA-based hardware, or the data can be stored in a raw format and analysed offline.
The talk presents the structure and capabilities of the DAQ system and shows example applications and future plans.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 44
Type: **Oral**

Prototyping of Hybrid Circuits for the CMS Phase Two Outer Tracker Upgrade at the HL-LHC

Wednesday, September 4, 2019 11:30 AM (25 minutes)

High Density Interconnect hybrids are being developed for the CMS Tracker Phase Two Upgrade for the HL-LHC. These hybrids are flexible circuits with flip-chips, passives and connectors laminated to carbon fibre composite stiffeners. The wirebonding of sensors and the soldering requirements for these components requires an almost perfectly flat surface. A lamination process is proposed, focused on the compatibility with lead-free reflow process. The stack-up of the hybrid was optimized to balance the forces induced by the Coefficient of Thermal Expansion (CTE) differences in the assembly. The proposed lamination process was applied to the 8CBC3 hybrid circuits.

Summary

Components for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) are currently under development. The upgraded Tracker is based on two main types of modules, the strip-strip (2S) and the pixel-strip (PS). The modules contain two parallel sensors and two front-end hybrids interconnected with different service hybrids. These modules require state of the art HDI front-end hybrids hosting the fine pitch flip-chip front-end ASICs and connectors.

The modules will be operated at low temperature: a liquid CO_2 cooling circuit, integrated in the supporting structures of the modules, will bring the temperature down to -35 ºC. The active components of a 2S front-end hybrid circuit will dissipate up to 1.5 W and an effective cooling path is required. However, this cooling path must contribute as little as possible to the equivalent radiation length of the module. A highly thermally conductive carbon fibre stiffener was selected for this purpose. In addition to its good thermal properties, the carbon fibre material has also a CTE value close to zero. This is desired for a good pitch matching of the hybrid with the silicon sensors at the level of the wirebond interconnecting pads. Moreoverit closely matches the CTE of the module support structure that is made also of a low CTE (4 ppm/ºC) aluminium-carbon fibre composite. However, a major thermal mismatch remains with the flexible circuit itself that has a CTE of 16 to 18 ppm/ºC.

The hybrid stack-up is also exposed to at least one lead-free reflow soldering cycle for the assembly of dies, passives and connectors. The adhesives used for the gluing of the flexible circuit to the carbon fibre stiffener must remain compatible with this process, up to at least 240 ºC, avoiding delamination. Several adhesives were evaluated. The use of rigid adhesives prevents the risk of delamination but results in a bow of the hybrid once it is cooled down. A thermal compensator, added on the other side of the stiffener, with an adequate material and a tuned thickness eliminates the bow for all the temperature range, enabling soldering on a flat hybrid and also minimising the mechanical stress induced by the hybrid once it is glued on its module and cooled down.

Furthermore, the carbon fibre stiffener, which is nearly fully enclosed between the hybrid circuit and its compensator, must be free of any outgassing during the reflow. A post-cure process, combined with sand scrubbing and strict drying just before the gluing provides a suitable lamination process without outgassing.

8CBC3 hybrid circuits were laminated with hard adhesives to post-cured and dried carbon fibre

stiffeners and to CTE compensators. The resulting hybrid configuration outperformed all the others in terms of flatness and stability. It remains flat during the reflow process and at low temperatures. However, secondary effects resulting from the compressive stress along the stiffener need to be considered for the soldering process. All the lamination issues and the solution adopted for the CMS hybrids will be presented.

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Presenters: BLANCHOT, Georges (CERN); RASEVIC, Nikola

Session Classification: Packaging and Interconnects

Track Classification: Packaging and Interconnects

Contribution ID: **46**   Type: **Oral**

An lpGBT sub-system for environmental monitoring and control of experiments

Friday, September 6, 2019 9:50 AM (25 minutes)

In this paper, an lpGBT sub-system for environmental monitoring and control of experiments is presented. The monitoring part contains an 8 external and 8 internals inputs followed by a 16-to-1 multiplexer, instrumentation amplifier with selectable gain and a 10-bit ADC. A constant current source can be enabled on each external input to facilitate resistances measurements. Internal channels are used to monitor power supplies and the output of the temperature sensor. The control part includes a precise 1V voltage reference and a 12-bit voltage DAC. All the blocks were prototyped in 65nm CMOS technology, fully characterized and measurement results are presented.

Summary

In detector systems of modern particle physics experiments environmental monitoring and control system is indispensable.

This work presents the design and measurements results of such system implemented in the lpGBT ASIC. For monitoring of analog signals, a fully differential instrumentation amplifier with three selectable gains (x2, x8, x16) and fully differential 10-bit SAR ADC were developed. Such a solution allows single-ended and differential mode measurements. The selectable gain enables measurements for input voltage differential range from +/-500mV down to +/-70mV (in highest gain) in a wide range of input common mode voltage from 0.4V to 0.9V. Each of the voltage inputs is equipped with an internal current source (0-1mA), controlled by an 8-bit DAC which can be used to supply current to resistive sensors like PT1000 or to bias analog circuits.

The ADC reference voltage is 1V scaled up from ˜0.3V provided by the bandgap circuit. A PTAT branch from the bandgap circuit is used as an internal temperature sensor. The reference voltage can be also used to bias external circuits and guarantees stable voltage with capacitive loads up to 10nF.

A 12-bit voltage DAC delivers precise voltages in the 0-1V range.
All blocks will be calibrated during production testing to cancel the effects of process variations. The calibration constants will be stored in a dedicated on-chip non-volatile memory.

Performed measurements confirmed the full system functionality and very good agreement with simulations. In particular, the ADC channels achieves good performance with DNL and INL linearity errors around 1 LSB and effective resolution of around 9 bits. Very good linearity has been measured for all gain configurations. Detailed measurement results for all the circuits will be presented at the workshop.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **47**   Type: **Poster**

Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade

Thursday, September 5, 2019 4:55 PM (20 minutes)

The pixel-strip modules for the CMS Tracker Phase Two Upgrade for the HL-LHC integrate a readout hybrid (PS-ROH) for the control and data acquisition link. This hybrid is based on the new, low power and compact gigabit transceiver (lpGBT) and the Versatile Transceiver VTRx+ specifically designed for the upgrade. A characterization board was first designed to qualify the design rules and the achievable timing performance of the gigabit block. This design enabled the development of the PS-ROH hybrid for the CMS Tracker PS modules. A testing setup was also developed to verify the PS-ROH performance before its integration in modules.

Summary

Two new front-end module types (2S and PS) are currently under development for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High Luminosity Large Hadron Collider (HL-LHC). These 2S modules on a double strip-strip (2S) sensor configuration with an active area of 10 × 10 cm2. The PS modules contain a strip sensor and a macro pixelated strip sensor of 5 × 10 cm2 and two front-end hybrids interconnected with a power hybrid and with an optical readout hybrid. The readout hybrid enables the optical transmission of clock, control and data at transmission speeds up to 10.24 Gbps in the cold and radiation environment of the tracker.

The optical readout hybrid interfaces the two front-end hybrids with the new low power gigabit transceiver lpGBT. This new ball grid array chip provides various operation modes, high-speed differential ports (e-links), digital input and output control ports and eight analog to digital converter inputs. It provides an enhanced clock distribution and phase alignment features.

A characterization board enabling all possible configurations was designed in the first step on a six layers rigid printed circuit board. It provides 100 Ω matched impedance routing with test connectors for lpGBT Phase Shifted Clocks, some of the e-links and with high data rate SMA connectors to interface with an external optical module (VTRx+). The differential pair topologies were verified with signal integrity simulations. Two decoupling scheme configurations on the top and on the bottom layer are proposed and were characterized by power integrity simulations. This board is in production and will be tested in May 2019.

The lpGBT was later on integrated into the PS-ROH, on a four layers flexible circuit. Suitable differential topologies were defined for an achievable impedance of 90 Ω for the e-links. A specific differential pair topology for the gigabit lines connecting to the VTRx+ was also defined. The decoupling scheme is here only possible on the top layer, and power integrity simulations allowed comparing the expected performance with respect to the characterization board implementation. This board is also under production and will be tested in July 2019.

The performance of the characterization boards will be measured with laboratory instrumentation. However, because the PS-ROH is a tracker specific integration, a dedicated test bench is under development and will be assembled in June 2019. This specific infrastructure allows verifying the PS-ROH performance; it can be scaled in a multiplexed testing infrastructure for production phase quality control tests.

The proceeding will present the design parameters for rigid and flexible circuit integrations, the optimal differential pair implementations, and the data transmission properties. The PS-ROH im-

plementation on a flexible circuit and the testing method are proposed as an application example.

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Presenter: RASEVIC, Nikola

Session Classification: Posters

Track Classification: Packaging and Interconnects

Contribution ID: **48**
Type: **Oral**

A multi-channel multi-data rate circuit for phase alignment of data in the lpGBT

Friday, September 6, 2019 11:30 AM (25 minutes)

The design and test results of a multi-channel multi-data rate circuit for phase alignment of data in the lpGBT ASIC fabricated in a 65 nm CMOS technology are presented. The circuit is composed of 4 delay lines regulated by a Delay-Locked Loop followed by logic responsible for phase selection and multi-mode deserializer. The circuit is able to handle up to 4 serial data streams with a data rate of 160, 320, 640, or 1280 Mbit/s. The test results show that all blocks are functional in all modes of operation.

Summary

The presented phase-aligner is a building block of the lpGBT chip, a low power gigabit transceiver for the high energy physics experiments. The phase-aligner is responsible for delaying the input data stream to ensure that it can be properly sampled by an internal clock. Each channel incorporates a delay line with 14 equally-spaced taps controlled by a DLL. Based on signal transitions, the phase selection logic determines the optimum sampling point and decides which tap should be used as an input to multi-mode deserializer.

The DLL has 16 delay cells and is locked to clock period equals 2Tbit. Its control voltage is distributed to 4 replica delay lines ensuring that the unit delay is the same. Each line is made of 28 identical delay cells, but only fully used in the data rate of 160 Mbit/s. In other data rates, the first 14 delay cells are activated, while the remaining are powered down. Delay of one cell has been set to Tbit/8, which is 97.7, 195.3, 390.6, or 781.3 ps for a bit rate of 1280, 640, 320 or 160 Mbit/s respectively. The overall length is 7Tbit/4 enabling the delay line to store more history of data and thus to track the phase in more situations. In 160 Mbit/s, all 28 cells are delayed by 390.6 ps, while two delay cells are joined together to form a delay of 781.2 ps, and only even taps are output to phase selection logic. The delay line of the DLL is located in the center of four replicas to ensure the best matching.

The symmetrical delay cell consists of two half-cells which are based on the current-starved inverter. The half-cell has an inverter cascaded by an active NAND and a dummy NAND. Only the active NAND in the second half-cell can output to the phase selection logic. Active and dummy NANDs are controlled by complementary signals keeping the load of half-cell always the same.

The phase selection logic determines the optimal phase based on the edge detection basis. It has three modes: static phase selection mode in which the tap is selected upon user configuration, training with learned static phase mode in which the phase is automatically selected after power-up, and automatic phase tracking mode in which the logic continuously monitors input data phase and selects the optimum sampling point. While the automatic phase tracking mode is the most robust, it requires that the whole delay line is always active and therefore the power consumption in this mode is the highest. For the other two modes, when the phase is determined, the delay cells after the selected cell can be disabled, so do the output buffer of previous cells.

The radiation resistance of the phase-aligner is enhanced by means of Enclosed Layout Transistor (ELT). The phase selection logic is fully triplicated to ensure robustness against SEU. The phase-aligner has been tested as part of the lpGBT and it is fully functional in all modes of operation.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **49** Type: **Oral**

First lpGBT-based prototype of the End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade

Wednesday, September 4, 2019 9:25 AM (25 minutes)

The central building blocks of the ATLAS Strip Tracker Upgrade are the staves and petals which host up to 14 modules per side. The incoming data is sent to the EoS and multiplexed by the lpGBT chips on 10 Gbit/s links and sent via optical transmitters (VL+) off-detector. The EoS is a critical component for the upgrade, sitting at a single-point-of failure location. Prototype boards have been designed, manufactured and tested using the first available lpGBT and VL+ prototypes from CERN. We present the first test results and give an outlook towards the production of 2000 boards using these chips.

Summary

We have produced first prototypes using the first available versions of the lpGBT and VL+ ASICS's. Presented will be the design of the electronics, the exercised tests for electrical behavior, mechanical deformation and thermal behavior. By the use of the EoS for substructure tests experience for detector level performance is gained. Since each EoS sits at a single-point-of-failure for an entire stave or petal side, a dedicated quality control and assurance procedure for the planned 2000 EoS PCBs has been developed and will be presented as well.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **50**   Type: **Poster**

The ETROC Project: ASIC development for CMS Endcap Timing Layer (ETL) upgrade

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Endcap Timing Readout Chip (ETROC), being developed for the CMS Endcap Timing Layer (ETL) for HL-LHC, is presented. Each endcap will be instrumented with a two-disk system of MIP-sensitive LGAD silicon devices to be read out by ETROCs for precision timing measurements. The ETROC is designed to handle a 16×16 pixel cell matrix, each pixel cell being 1.3x1.3 mm^2 to match the LGAD sensor pixel size. The design of ETROC, with its unique challenges and how they are addressed, as well as prototype testing results, are presented.

Summary

The ETROC is implemented in TSMC 65nm. At the pixel level, each channel consists of a preamplifier, a discriminator, a TDC used for TOA (time of arrival) and TOT (time over threshold) measurements, and a memory for data storage and readout. The TOT is used for time-walk correction of the TOA measurement. The detailed hit information (TOA and TOT) from within each cell will be read out from a local circular buffer after each Level- 1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of the signal pulses as radiation dose increases, waveform sampling circuits will be included in selected pixel cells. Additional peripheral circuits include a PLL, a phase shifter, an I2C slave, a fast control block, a serializer, and a data driver.

The ETL design goal for the time resolution is 50 ps per hit, in order to achieve a 35 ps arrival time measurement for a MIP track with an ETL hit in each of the two-disk layers. This means that the jitter from the ETROC preamplifier/discriminator has to be kept below 40 ps. The main design challenge is how to extract precision timing information from small LGAD signal size due to high irradiation fluence while at the same time keep the power consumption low. Approximately 15% of the sensors near the highest eta region will have more than 1e15 neq/cm^2 towards end of operation of HL-LHC, resulting in small signal size with LGAD gain reduced to around 10. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the small LGAD signals, with enough flexibilities to meet the ETL specific needs for time resolution, power budget and radiation profile. In addition, the TDC stage design has been optimized for low power operation in such a way that one simple delay line with uncontrolled delay cells is used to measure both TOA and TOT at the same time. This is made possible by using an in-situ delay cell self-calibration technique, that is, to use two consecutive rising clock edges to record two time stamps for each hit. The time difference between the two time stamps is the known clock period, and this fact can be used for delay cell calibration for every hit. Effective clock distribution is a challenge and care must be taken in minimizing clock skew and jitter. For ETROC we have adopted the most common and conservative clock distribution scheme, known as H-tree.

The most critical component, the front-end preamplifier and discriminator, has been implemented in single channel ETROC0 and submitted in Dec. 2018. The testing of the ETROC0 has been on-going since April 2019. The TDC design has been fully implemented and is being integrated in a 16-channel ETROC1 chip, with a 4x4 clock tree distribution. The ETROC1 chip is scheduled to be submitted in summer 2019. The waveform sampling block is being implemented as well and scheduled for submission over summer 2019.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **51**   Type: **Oral**

Production, Quality Control and Performance of VFAT3 Front-end Hybrids for the CMS GE1/1 Upgrade

Friday, September 6, 2019 9:50 AM (25 minutes)

CMS is planning to install GEM chambers as part of the Muon upgrade for High Luminosity Operation at the LHC. The front-end ASIC (VFAT3) has been produced in volume together with its hybrid PCB. This paper describes the design of a custom test bench for the production Quality Control (QC) of the VFAT3 hybrids. The full QC procedure incorporates calibration and performance measurements, database entries and statistical data analysis. The paper details the optimization of firmware and software functions reducing the test time per hybrid from 30 to 1.2 minutes. Pre-Series production of 1000 hybrids shows a yield of 94%.

Summary

VFAT3 is the Front-end ASIC specifically designed for the readout of gaseous detectors within the CMS experiment during the high luminosity upgrade of the LHC at CERN. VFAT3 characterization and hybrid production QC is a compulsory demand for the GE1/1 chambers installation. A custom test bench is designed for VFAT3 characterization and hybrid production testing for the GE1/1 detectors. This platform consists of a Kintex-7 evaluation board, a custom Verification board, a Handheld IR Temperature Gun, a Barcode Scanner, a Power Supply and a Linux PC with test software. The Verification board is connected with the FPGA platform through FMC VITA standard and has onboard power monitoring features. The firmware is based on a System-on-Chip (SoC) architecture with Microblaze processor connected to the Verilog HDL peripherals within the FPGA through Advanced Extensible Interface (AXI) bus architecture. The firmware communicates with VFAT3 through Scalable Low Voltage Signaling (SLVS) at 320 Mbps. The software is designed with Python and the graphical interface is built using TkInter GUI package. The software controls the firmware and other USB peripherals and communicates with the test system through a 1-Gbps TCP/IP interface. Through the test system, the software provides two unique modes. First, one is an interactive mode and is solely utilized for debugging and characterization of the hybrid. The second mode is a production interface, which runs a predefined set of tests and APIs that are needed for the production testing of the hybrid. The production interface requires minimal operator intervention and is user-friendly. The existing test bench was unable to test large volumes of the VFAT3 hybrids, so an extensive upgrade was done to implement complex computing and iterative blocks in the firmware. This helped to reduce the full production test time per VFAT3 hybrid from 30 minutes to 1.2 minutes. The production testing of each hybrid performs several high-level tests including S-Curves and DAC Scans. The results of these routines are compared against predefined selection criteria, which defines a green, yellow or red hybrid. These results are then gathered to decide if the tested hybrid is suitable for GE1/1 production or if it should be discarded. An automatic link to central MySQL is also established for production data storage and retrieval of the hybrid parameters during the CMS experimental run. A pre-series of 1000 hybrids have been tested and the data are statistically analysed to detect the nominal VFAT3 parameters for GE1/1 operation. The common production failure causes are also understood, like broken ADCs, dead/noisy channels and hybrid-short. An overall yield of more than 94% is achieved from VFAT3 production platform.

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Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability

Contribution ID: **52**   Type: **Oral**

A Precision Pure Clock Distribution System

Tuesday, September 3, 2019 2:50 PM (25 minutes)

We will describe a pure clock distribution system, built with discrete RF components, that we
have used to demonstrate the precision that separate clocks generated from a single source can be
distributed within a large detector. Clock signals were distributed directly without any encoding
or
clock cleaners (PLLs) through parallel 90m optical bers to front-end emulators. The phase noise
measured between two 160 MHz clocks was 0.210 ps/1.0 MHz, integrating between 0.01 Hz and 1
MHz. We will discuss the system, the tests made and the steps we are taking to monitor the clock
stability at the point of distribution.

Summary

As precision particle timing becomes a critical component of the design of modern high energy
physics experiments the need for precise clocks distributed across the detector with low jitter be-
tween them becomes very important. The figure of merit in an experiment for a clock distribution
system is not the quality of an individual clock, which can be achieved with one or more PLLs in
the chain, but the stability between two separate clocks. This is because the relevant measurement
is the time difference between two or more signals from different parts of the detector, which may
be separated by tens of meters.
To investigate this question, we have built and tested a stand-alone pure-clock distribution net-
work
to quantify what can be achieved using modern discrete RF integrated circuits. The system con-
sisted
a master clock that was distributed to two parallel chains each with with multiple levels of fan-out,
conversion from electrical to optical signals, transmission on 90m optical multi-mode fibers and
conversion back to an electrical signal to emulate the real needs of an experiment. Using the clock
from one arm as the reference clock and measuring the clock signal in the second arm, we mea-
sured
a phase noise of 0.210 ps/1.0 MHz, integrating between 0.01 Hz and 1 MHz, and the time interval
error measured with a high-performance oscilloscope scope was < 2ps. In this talk we will discuss
the design and testing of the system and steps we are taking to demonstrate that it is feasible to
demonstrate such a high precision used in an experiment.

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Session Classification: Optoelectronics and Links

Track Classification: Optoelectronics and Links

Contribution ID: **53** Type: **Poster**

Analysis of Time of Arrival Measurement with Low-Gain-Avalanche-Diode Sensor

Thursday, September 5, 2019 4:55 PM (20 minutes)

Results of analyzes of Time-of-Arrival measurements with Low-Gain-Avalanche-Diode sensors were carried out for the amplitude or time-over-threshold corrected leading edge measurements and for practical realization of Constant-Fraction-Discrimination based on ideal delay and RC-type low-pass filtering delay. The Expected current waveforms, resulting from modeling of a sensor and application of varied conditioning of a signal in the front-end circuit, including varied transfer functions and their parameters were considered together with practically achievable signal-to-noise ratio. The work has been done to estimate the levels of variations of time-of-arrival measurements that are achievable in the practically built systems.

Summary

Low-Gain-Avalanche-Diode (LGAD) sensors are young devices that possess attractive features for building timing layers in the experiments on the HL-LHC. A program allowing modeling current waveforms, originating from ionization due to the traversing particles through LGADs and consequent multiplication of the generated charge have been developed by Nicolo Cartiglia. To learn what performances can be expected from readout electronics coupled to LGADS, analyzes of Time-of-Arrival (ToA) measurements were carried out for the amplitude or time-over-threshold (ToT) corrected Leading Edge (LE) measurements and for practical realizations of Constant-Fraction-Discrimination (CFD) based on ideal delay and additional RC-type low pass filtering. The time-domain simulation environment, allowing representing the entire signal processing chain from the LGAD current waveforms, through amplification and conditioning of signals in filtering, addition of noise based on equivalence of frequency and time domain representations and discrimination was developed in the Mathematica package.

The purpose of this work was to be able to enter any transfer function of an amplifier-shaper block in s-domain, including cut-off frequency and degree of additional delay in case of realistic realization of CFD, noise assuming signal-to-noise ratio, define time binning of ToA, ToT and binning for amplitude measurements, select family of current waveforms of LGAD signals for designated bias voltage and neutron fluence and obtain results for typical ToA measurement methods. The methods included in the analyzes are: the amplitude or time-over-threshold corrected LE measurements and practical realization of CFD based on subtraction of delayed by either ideal delay or by RC-type low pass filtering waveform from the scaled original one.

As an illustration of the obtained results are given those for the CR-RC3 amplifier-shaper transfer function with the peaking-time varied from 1 to 4 ns and signal-to-noise ratios varying from 30 to 100 for LGAD responses simulated for a 50 μm-thick sensors for neutron fluences 0, 5e14 and 1e15 n1MeV/cm2. Studies of time binning from 20 to 100 ps, from 80 to 1200 ps and amplitude binning from 3 to 8 bits equivalent were done for ToA, ToT and amplitude measurements, respectively, to answer the question about foreseeable level of the time measurement precision.

Assuming a signal-to-noise ratio of 60 and peaking time of impulse response equal to 2 ns (as reasonable values due to power consumption), ToA variation ranging from 30.5 ps and 35.0 ps for ideal CFD and CFD with RC delay to 37.5 and 35 ps for LE with ToT and amplitude correction, were obtained for non-irradiated sensors. These values change correspondingly to 31.5 ps and 35.0 ps

for CFDs and 35.0 and 44.0 ps for LEs for 5e14 n1MeV/cm2 and 36.5 ps and 49.0 ps for CFDs and 50.0 ps and 53 ps for LEs for 1e15 n1MeV/cm2. Decreasing peaking time to 1 ns leads to noticeable improvements in LE results by 5 to 7 ps, while improvements in the CFD results is about 1 ps for the ideal delay and 5 to 7 ps as well for the RC delay. The review of the results is given.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **54**   Type: **Oral**

The upgraded readout electronics of the CMS ECAL: system overview

Thursday, September 5, 2019 10:15 AM (25 minutes)

The readout electronics of the CMS electromagnetic calorimeter (ECAL) barrel will be upgraded to meet the Level-1 trigger requirements at HL-LHC. The new very front-end (VFE) electronics will mitigate the increasing noise from the avalanche photodiodes (APDs), discriminate against anomalous APD signals, and provide the extra bandwidth needed to maintain the integrity of the detector signal shape. The front-end (FE) card will provide the streaming of data from VFE to back-end electronics, which will have increased granularity (tower-level to single crystal-level). The design of the full ECAL barrel readout chain and the status of the components R&D will be presented.

Summary

During High-Luminosity LHC phase (HL-LHC), the CMS ECAL will have to cope with a challenging increase in the number of interactions per bunch crossing and radiation levels. The ECAL barrel (EB) on-detector and off-detector electronics have been completely redesigned to preserve detector performance with the goals of providing precision timing, low noise, and added flexibility in the trigger system.

Two custom ASICs have been developed for the very front-end (VFE) upgrade: CATIA (CAlorimeter Trans-Impedance Amplifier), a fully analog ASIC, and LiTE-DTU, a digital signal processing unit, designed in commercial CMOS 130 nm and 65 nm technology, respectively. CATIA and LiTE-DTU ASICs will manage to cope with the new requirements in terms of input bandwidth, conversion and transmission rates, and radiation tolerance. The two ASICs will be hosted by a VFE board with the same form factor and cooling system as the legacy system. The current readout chip (MGPA) based on Charge Sensitive Amplifier (CSA) will be replaced by a high speed Trans-Impedance Amplifier (TIA), 50 MHz of bandwidth. The output dynamic of CATIA ASIC is split into two ranges: 200 GeV (achieved through a gain10 stage after the TIA) and 2 TeV. The two output gains are fed to a dual 12-bit, 160 MS/s ADC hosted by the LiTE-DTU ASIC. The high speed TIA and the high speed ADC will enable the mitigation of the increasing noise induced by avalanche photodiode (APD) ageing, to improve the suppression capability of APD anomalous signals, and to help to discriminate between energy deposits coming from different overlapping events.

The EB upgrade will face to an increasing of sampling frequency from 40 MS/s to 160 MS/s and a granularity from tower-level (5x5 crystals) to single crystal-level. In addition, the EB system will have to fulfill the maximum trigger rate requirement of 750 kHz and event pipeline of 500 bunch crossings 12.5 us). Each readout channel will produce an amount of data which will require fast data transmission circuitry and high speed serial links. A new digital architecture has been developed in order to decrease the data bandwidth by means of lossless data compression. This function has been integrated in the LiTE-DTU, which performs compression based on a simplified version of Huffman coding taking advantage of the relatively low compression rate needed (around 0.6). This method allows the readout to easily manage two different code lengths while avoiding transmission errors. The new front-end (FE) card will host LpGBT chips that concentrate and stream all data, generated on the VFE cards, and send them to back-end (BE) electronics via Versatile+ links. This will allow the trigger primitive generation (TPG) and the DAQ of the legacy FE to be moved

to a new BE system. The latter will also handle the FE control. In addition, a high precision clock, essential in a high pile-up environment, is foreseen to be distributed to the front-end boards. CATIA, LiTE-DTU, and front-end designs will be presented, along with the verification of the compression scheme and the test results of the prototypes.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **55**   Type: **Oral**

A 4-Channel 10-Gbps/ch CMOS VCSEL Array Driver with on-chip Charge Pumps

Tuesday, September 3, 2019 9:25 AM (25 minutes)

We present the design and test results of a 4-channel 10-Gbps/ch Vertical-Cavity Surface-Emitting Laser (VCSEL) array driver, the cpVLAD, with on-chip charge pumps to extend the biasing headroom for the VCSEL's needs for low temperature operation and mitigation of the radiation effects. The cpVLAD was fabricated in a 65-nm CMOS technology. The test results show that the cpVLAD is capable of driving VCSELs with forward bias voltages as high as 2.8 V. The power consumption of the cpVLAD is 94 mW/ch. Further optical tests and irradiation tests will be carried out and reported at the workshop.

Summary

The cpVLAD, a 4 x 10 Gbps VCSEL array driver, has been designed to address the limited headroom available for driving VCSELs using only the 2.5 V power rail available in 65 nm CMOS technology with radiation-tolerant requirements. The VCSEL forward voltage increases with low temperature and radiation dose, reducing the voltage headroom. The cpVLAD has on-chip charge pumps, which increases the driving stage power supply without the need for additional powering schemes in HL-LHC experiments. The cpVLAD has been prototyped in a 65 nm CMOS technology using a pad-frame that makes it compatible with the current VTRx+ design, thus allowing the possibility of using it in cases that require additional margin for operating in very high radiation environments. The cpVLAD has four independent channels. All channels share a Voltage Controlled Oscillator (VCO) and an Inter-Integrated Circuit (I2C) slave. Each channel consists of a limiting amplifier (LA), an output driver, and a charge pump. The LA has a four-stage structure with two center-tapped shared inductors. The output driver is a differential to single-ended topology. The charge pump utilizes cross-connected NMOS and PMOS transistors driven by an 800 MHz 1.2 V clock from the VCO to boost the 2.5 V power supply to a higher voltage for the output driver. The feedback circuit automatically adjusts the output voltage of the charge pump according to the forward voltage of the VCSEL diode. Each channel of the cpVLAD provides a bias current and a modulation current in the range of 0 to 6.8 mA and 0 to 13.6 mA, respectively. The chip size is 1.85 mm x 1.65 mm.

Electrical tests have been conducted. The measurement results show that the maximum DC output current exceeds 12 mA. The driver is still functional at 10 Gbps even when the forward voltage of the VCSEL diode is as high as 2.8 V. The total jitter is 26.6 ps (P-P for a bit error rate of 1E-12) with a random jitter of 1.1 ps (RMS) and a deterministic jitter of 14.8 ps (P-P). The rise time and the fall time are 31 ps and 32 ps, respectively. The power consumption is 94 mW/ch. A full set of optical and irradiating test results will be presented at the workshop.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **56**   Type: **Oral**

2.5V step-down DCDCs: a radiation-hard solution for power conversion

Thursday, September 5, 2019 11:55 AM (25 minutes)

Radiation- and magnetic field tolerant DCDC converters that step down the voltage from a 2.5V bus are needed for the High-Luminosity detectors. This work presents the developed prototypes, based on ASICs designed in a 130nm CMOS technology. A buck converter (bPOL2V5) is close to production readiness, showing an 89% peak efficiency and tolerance to more than 250Mrad of Total Ionizing Dose and to a fluence of 10ˆ16n/cmˆ2. The ASIC and the PCB have been co-designed to guarantee high reliability. A lower-volume alternative to bPOL2V5 uses a resonant switched-capacitor architecture and shows comparable efficiency, while employing an eight times smaller inductor.

Summary

In the High-Luminosity Large Hadron Collider detectors, some modules require multiple power domains. A compact and efficient power distribution strategy for such systems uses two cascaded Point-of-Load DCDC converters: a first-stage converter having as input a 12V line creates a 2.5V domain, which powers the opto-electronic components. Second-stage converters further step down the voltage from 2.5V to supply the front-end analog and digital circuits. This work presents the status of radiation- and magnetic field tolerant second-stage converters, which provide an output voltage ranging from 0.6V to 1.5V and an output current up to 3A.

Two converters using different architectures and based on ASICs designed in a 130nm CMOS technology have been developed. A buck converter (named bPOL2V5) is close to production readiness, and the characterization results of the final prototype will be presented at the workshop. Furthermore, a functional prototype of a resonant switched-capacitor converter (named rPOL2V5) has been designed, demonstrating that it is possible to reduce the converter volume by adopting a significantly smaller inductor compared to the buck architecture, while keeping a comparable efficiency.

Early prototypes of bPOL2V5 employed devices rated 2.5V. Nevertheless, the current transients experienced by the input parasitic inductor cause voltage spikes that significantly exceed the input voltage. In order to guarantee the converter reliability, a prototype buck converter using devices rated 3.3V devices has been developed. The adoption of a flip-chip assembly to reduce the bonding inductance, the minimization of the PCB parasitic inductance and the proper sizing of the gate driver current of the power MOSFETs guarantee that the voltage spikes never exceed the device rating.

The developed prototype uses a 100nH inductor and shows peak efficiencies of 89% for the 2.5V-to-1.2V conversion, and 87% for the 2.5V-to-1V conversion. Irradiation with x-rays has demonstrated that the circuit is tolerant to more than 250Mrad of Total Ionizing Dose, while neutron irradiation up to a fluence of 10ˆ16n/cmˆ2 has caused no significant degradation in the converter performances. Furthermore, bPOL2V5 will be tested for Single Event Effects using heavy ions, and the results will be reported at the workshop. The ASIC features a trimmable on-chip voltage reference circuit to guarantee an accurate and uniform output voltage. In addition, a test procedure which will be performed at wafer level together with the trimming procedure has been devised.

The resonant switched-capacitor architecture mainly uses a capacitor as the energy storage de-

vice, together with a small inductor. The developed prototype of rPOL2V5 adopts a novel control scheme that uses different modes to optimize the efficiency over the whole load range. It shows a peak efficiency of 92% for 2.5V-to-1.2V conversion and 84% for the 2.5V-to-1V conversion. The efficiency is comparable to that of bPOL2V5, despite the used inductor is approximately eight times smaller (12nH). The radiation performances of rPOL2V5 will be analyzed and reported at the workshop. In order to bring rPOL2V5 to production readiness, additional work is needed to guarantee its stability and the reliable transition between the different operation modes.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **57**   Type: **Poster**

Implementation of a CANbus interface for the Detector Control System in the ALICE ITS Upgrade

Thursday, September 5, 2019 4:55 PM (20 minutes)

For the Long Shutdown 2 upgrade of the ALICE experiment, a new Inner Tracking System (ITS) is under development, based on the ALPIDE Monolitihic Active Pixel Sensor (MAPS) chip.

Data readout from the ALPIDE chips is performed by 192 Readout Units (RU), which are also responsible for trigger distribution, monitoring, configuration, and control of the sensor chips. Monitoring and control of the experiment is performed by the Detector Control System (DCS), normally via optical GBT links offered by the RU. A CANbus interface is also provided as a backup and this paper will discuss the implementation of this interface.

Summary

For the Long Shutdown 2 (LS2) upgrade of the ALICE experiment at the CERN LHC, a new Inner Tracking System (ITS) is under development. The upgraded ITS will consist of 24120 ALPIDE pixel sensor chips in seven cylindrical barrels, which offer significantly improved tracking capabilities over the existing system, and at higher event rates.

Data readout, trigger distribution, configuration, monitoring, and control of the sensor chips is performed by an SRAM-based Xilinx UltraScale FPGA, which is the main FPGA on each of the 192 Readout Unit (RU) boards. In addition, the RU boards have a flash-based Microsemi ProASIC3 FPGA and an external flash memory, which are used for configuration and scrubbing of the main FPGA.

The RU features custom radiation hardened transceivers and ASICs from LHC's GBT project for a radiation hardened bi-directional optical link. It has three optical transceivers; one VTRx with a downlink for triggers (no uplink); another VTRx with a downlink for control, and an uplink for data and control; and one VTTx with two additional data uplinks. These transceivers connect to three transceiver ASICs called GBTx, which are connected to the main FPGA.

The uplinks connect to the Common Readout Unit (CRU) in the First Level Processor (FLP). There are 24 CRUs for the ITS, each handling eight RUs. From the CRU/FLP, data go to the O^2 (Online-Offline) system and control signals go to the Detector Control System (DCS), which is responsible for monitoring and control of every detector in ALICE. In the ITS this is performed by accessing the wishbone bus in the main FPGA on the RUs. This access is implemented over GBT using a custom protocol.

To keep the operational conditions stable the ITS staves should ideally have power at all times, with temperatures and currents monitored by DCS. Normally this is done over the GBT links. But the GBT links are not always available, such as under maintenance periods with no beam, or in the unlikely case of radiation related errors. Therefore, the RU also has a CANbus interface, with a High Level Protocol (HLP) for wishbone access implemented on top of the CANbus frames, based on a protocol developed for the TOF detector in the STAR experiment.

The HLP protocol uses standard CANbus frames with 11-bit ID. Eight of those bits are used for node ID (configurable by DIP switches on the RUs), and the remaining three bits are used to indicate the type of command (e.g. read or write).
CANbus uses a multi-drop network topology, which allows several RUs to be connected to the same bus and limits the amount of cabling. In principle, every node is a master in the base CANbus

protocol, but the HLP protocol implements a request/response scheme where the DCS effectively acts as a master, and the RUs act as slaves that respond to the requests.

This paper presents the implementation of the CANbus HLP in the RU, and also the efforts taken to protect the interface logic in the FPGA against radiation induced upsets.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **58**   Type: **Poster**

ATLASpix3 : A high voltage CMOS sensor chip designed for ATLAS Inner Tracker

Thursday, September 5, 2019 4:55 PM (20 minutes)

ATLASPIX3 is a 2cm x 2cm HVCMOS sensor designed to meet the specifications of layer 4, ATLAS inner tracker. ATLASPIX3 is a depleted monolithic CMOS pixel detector. The chip size allows the construction of quad modules of equal size as that of hybrid sensors. ATLASPIX3 supports triggered readout. The hit information is transmitted via 1.28 Gbit/s. The clock, trigger and configuration bits are derived from a single command input that follows RD53 protocol. This contribution will summarize the detector architecture and concentrate on the design of readout circuitry. If available, the first measurement results will be presented.

Summary

ATLASPIX3 is a HVCMOS sensor designed to meet the specifications of layer 4, ATLAS inner tracker such as radiation tolerance of 100 MRad and 1015 neq/cm2, in-time efficiency of 99% within 25ns, power consumption of less than 300mW/cm2. Several on chip features such as sorted readout, command decoder, aurora 64b/66b encoding are implemented in ATLASpix3 compared to its small-scale predecessors ATLASpix1 and ATLASpix2. It is compatible with the hybrid pixel sensors RD53 ASIC in terms of electronic interface and geometry.

ATLASPIX3 is a depleted monolithic CMOS pixel detector implemented in 180nm high voltage CMOS technology. Instead of standard substrate, we use a high ohmic substrate of resistivity 200-Ohm cm. The chip size is 2cm x 2.1cm, which allows the construction of quad modules of equal size as that of hybrid sensors. 90% of the chip area is active with 10% periphery at the bottom. The pixel pitch is 50μm x 150μm. ATLASPIX3 supports triggered readout with programmable latency up to 25μs. The hit information (pixel address, 10 bit time stamp and 7 bit amplitude information) is transmitted via 1.28Gbit/s digital link. The interface is based on a single command input that is used for providing clock, trigger and configuration commands. The command protocol is the same as that of RD53. The chip has been submitted and we expect the first results in August.

This contribution will summarize the detector architecture and concentrate on the design of digital blocks: hit buffers, trigger buffers, readout control unit, command decoder and clock generator. If available, first measurement results will be presented.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **59**

Type: **Oral**

The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness

Thursday, September 5, 2019 11:30 AM (25 minutes)

We present the electrical and radiation characterisation of the production-ready prototype of the bPOL12V DCDC converter, a stacked assembly of two ASICs inside a QFN32 package. The use of a reference voltage generator chip in 130nm CMOS on top of the ASIC integrating the control system and power train enables improved radiation tolerance and the trimming of the output voltage during the production phase. The comparison of results from proton and neutron irradiations evidence that the NIEL hypothesis is not applicable to the LDMOS transistors used for the bPOL12V, hence making the qualification process for displacement damage more complicated.

Summary

The bPOL12V is an integrated DCDC converter ASIC based on the FEAST2 circuit that has already been deployed in upgraded LHC detector systems, but capable of displacement damage tolerance compatible with the HL-LHC outer trackers' requirements. The electrical specifications generally match those of FEAST2 (maximum power of 10W, with 4A maximum current), with the exception of the input voltage range that might be limited below 12V. Long-term stress tests on fresh and irradiated samples are being conducted at the time of writing this summary, and their result will be presented at the workshop together with conclusions on the maximum recommended voltage. Similarly to its FEAST2 predecessor, the production-ready ASIC will be distributed in a QFN32 plastic package with thermal pad, but inside the package two ASICs are stacked on top of each other. A small ASIC designed in a commercial 130nm CMOS technology contains a reference voltage generator with excellent radiation tolerance and is electrically connected to the larger bPOL12V ASIC via 3 bond wires. Other than a much better stability of the reference voltage with irradiation, this solution also allows to precisely trim the reference voltage on-wafer for every circuit, ensuring a much narrower distribution of the voltage output of the converter across the full production. This assembly will be tried for the first time in early summer, and results will be presented at the workshop, where we will also describe the full production process starting from the production of the wafers and including the trimming of the reference voltage, the stacked assembly in a single package and the testing.

Samples of the supposedly production-ready versions of the bPOL12V ASIC and of the reference voltage generator will be available for testing in May, and will be exposed to different sources of radiation: X-rays, protons, neutrons and heavy ions. Most of these results, if not all, will be available by September and will be presented at the workshop. Particular relevance will be given to the proton and neutron exposures, since very recent results have evidenced the inapplicability of the NIEL hypothesis for the LDMOS (Laterally Diffused MOS) transistors used in the bPOL12V design. LDMOS exposed in identical conditions at three different facilities (Triga reactor at JSI in Ljubljana, IRRAD at CERN and MC40 at the University of Birmingham) show very different damage when the integrated fluxes are converted in 1MeV-equivalent neutrons. This observation considerably complicates the qualification of the bPOL12V ASICs, since typical specifications for displacement damage tolerance in LHC are reported in 1MeV-equivalent neutron fluxes without indication of the particle composition and energy spectra. A different approach for the qualification is needed, based on measured damage at different facilities and on the precise knowledge of

the radiation environment composition at the location where the converters will be installed.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **60**   Type: **Poster**

Multi-threaded TCP hardware stack for pixel detector readout on 10 Gigabit Ethernet

Tuesday, September 3, 2019 5:20 PM (20 minutes)

TCP has been widely used in readout systems. SiTCP is hardware-based TCP stack for Gigabit Ethernet, it realizes direct access and transfer of the data up to 949 Mbps in the memory of FPGA by utilizing TCP communication. The data rate multiplies with the development of pixel detectors for smaller pixels and higher frame-rates. The existing GbE design is no longer satisfied the requirement of transmission bandwidth. This paper describes a multi-threaded TCP hardware stack based on SiTCP for 10 GbE implementing on a single FPGA. The throughput from FPGA to PC is at the upper limits of 10 GbE.

Summary

1、Background：the introduction of pixel detector.
The hybrid pixel detector consists of a silicon sensor and a readout chip which is bump-bonded to the sensor with Indium. The sensor contains an array of 288 x 208 pixels while each pixel measures 150 μm×150 μm. Each pixel of the readout chip comprises a preamplifier, a discriminator and a counter. Aiming at X-ray imaging, pixel detector works in the single photon counting mode, the counting depth of every pixel is 20 bits. Therefore, in the 1.2 kHz frame rate, the throughput of each daisy chain (6 sensors) is around 8.63 Gbps. In order to achieve the purpose of real-time displaying data, we have to use 10 Gbps Ethernet.
2、The multi-threaded TCP hardware stack:
The Transmission control protocol (TCP) and Ethernet have been widely used in readout systems. Because of the functions of retransmission and flow control, it guarantees data reliability and stability. The SiTCP is the standard IP blocks, which provides FIFO (First In, First Out) interface that is convenient to connect with users'logic. The PHY layer can interact directly with the SiTCP via the Gigabit Media Independent Interface (GMII). First, we convert GMII to 10 Gigabit Media Independent Interface (XGMII) via asynchronous FIFOs, and use a simple hub module to connect multi XGMII. If the package comes from the up-port, this hub module will broadcasts to the down-ports. If the packages come from the down-ports, this module will sends packages in roll polling mode to the up-port with the Inter-Packet Gap (IPG). Second, we overclock the SiTCP up to 250MHz beyond its specification of 125MHz in order to run faster. The timing is carefully examined and the signals crossing clock domains are carefully handled to avoid metastability.
In the project of silicon pixel detector, TCP is used to transmit data and UDP is used for interaction between the host computer and the readout. A kind of control bus protocol interface is provided, which helps the host computer to read and write the specific register directly through UDP protocol.
Transfer performance was confirmed with the readout circuit. The multi-threaded TCP hardware stack with five SiTCPs transfers data to PC at a total of 9.2 Gbps, corresponding to the limit of TCP using 10 GbE calculated with overheads, such as protocol headers.
References: T. Uchida, "Hardware-Based TCP Processor for Gigabit Ethernet,"IEEE Trans. Nucl. Sci., vol. 55, no. 3, pp. 1631-1637, June 2008

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **61**   Type: **Oral**

Powering of the CMS Phase-2 Upgraded Tracker

Thursday, September 5, 2019 4:30 PM (25 minutes)

The LHC machine will be upgraded to increase its peak luminosity and possibly reach an integrated luminosity of $3000 - 4500$ fb^{-1}. The CMS experiment is called for an upgrade to keep up with the new challenges such as unprecedented radiation environment, requiring high resilience, and increased number of events per bunch crossing, requiring higher detector granularity. Consequently, both Outer Tracker (OT) and Inner (IT) Tracker have to fulfill very stringent requirements: OT (> 13000 independent modules) uses in situ DC/DC converters to parallel distribute 100 kW of power, IT a serial powering scheme to provide about 60 kW among thousands of modular units.

Summary

Within 2028 the Large Hadron Collider is going to be upgraded, targeting a peak luminosity of $5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1} and aiming to collect an integrated luminosity of $3000 - 4500$ fb^{-1} by the end of 2039. In order to operate at these unprecedented conditions the CMS experiment needs to upgrade its own apparatus, increasing both the radiation resiliance and the granularity of the detectors. A completely new system of central tracking silicon detectors is being designed, composed of innovative pixel detectors in the inner region (Inner Tracker) and silicon strip and macro-pixel detectors in the outer region (Outer Tracker). Two different powering schemes are used to provide bias (down to -1000 V) to the sensors and low Voltage power (in the range 2.5 - 0.8 V) to the front end electronics, for a total power consumption exceeding 100 W for Outer Tracker and 50 W for Inner Tracker. A common requirement is to keep the material budget as low as possible, in order not to compromise the detector performance, which includes minimizing the cross section and/or the number of the cables which bring power to the detectors.

For the Outer Tracker, composed of more than 13 thousand independent detector modules, a parallel power supply scheme is adopted, where one bias voltage and one low voltage line (10-11 V) is provided to each detector module. On detector DC/DC converters are used to transform and distribute the low voltage power to the rest of the front end electronics. The back-end power supply system is modular and has high-granularity; it must operate in the proximity of the detector, inside the experimental cavern, in the presence of ionising radiation and magnetic fields, in order to reduce the voltage drop on the cables.

For the Inner Tracker an innovative serial power distribution scheme is adopted, where series of $8 - 12$ detector modules are connected to one current source, thereby reducing the number of cables required to distribute the power. This powering scheme is supported by the readout chip, which provides the needed shunt and local voltage regulation capabilities. One voltage source distributes the bias voltage to the sensors within each serial chain, following a parallel scheme.

The two powering schemes and the status of their development are reported.

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Presenter: CASSESE, Antonio (INFN, Firenze (IT))

Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **62**   Type: **Oral**

First measurements with the CMS DAQ and Timing Hub prototype-1

Thursday, September 5, 2019 10:40 AM (25 minutes)

The CMS detector will undergo a major upgrade for Phase-2 of the LHC program: the HiLumi LHC, starting around 2026. The Phase-2 CMS back-end electronics will be based on the ATCA standard, with node boards receiving the detector data from the front-ends for processing via custom, radiation-tolerant, optical links. An ATCA hub board, the DAQ and Timing Hub (DTH), will provide the interface between the back-end nodes and the central Trigger, Timing, and DAQ systems. This paper presents the first measurements performed on the initial prototype production, with a focus on clock quality and serial link performance.

Summary

The upgraded CMS detector will be read out at an unprecedented data rate of up to 50 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size of 7.5 MB. The back-end electronics will be based on the ATCA standard, with node boards receiving the detector data via optical links from the front-end electronics and processing them.

The CMS DAQ and Timing Hub will connect to all back-end node boards. The DTH is responsible for the distribution of clock, trigger, and fast-control data from the central trigger control system to all back-end electronics and the handling of throttling signals in the other direction. The DAQ interface for the event data uses point-to-point optical links connected to back-end node boards and runs a custom lossless protocol ("SlinkRocket"). The event data are aggregated in the DTH and transmitted via standard commercial network (with links of 100 Gb/s or higher) and protocol (such as TCP/IP) to event building computer nodes at the surface.

The introduction of timing detectors for Phase-2 CMS, aiming for a 30 ps precision on individual detector hits, strongly tightens the requirements on the clock and timing information distributed throughout the experiment, with different sub-detectors introducing different requirements.

At TWEPP 2018 we presented the design of the first DTH prototype, and discussed some of the design challenges encountered. Other contributions summarised the phase noise studies performed as part of the component selection for the DTH. The DTH P1 board features an FPGA (KU15P) with ancillary components for clock recovery and jitter-cleaning, and serial links to the back-plane implementing the clock, timing, trigger and throttling functions. A second FPGA (KU15P) with mid-board optics (FireFly) connecting to the back-end boards, and QFSP+ cages connecting to the standard commercial network, implements the DAQ event flow functions.

The current paper presents first measurements performed on the initial prototype production, with a focus on clock quality and serial link performance via back plane and mid-board optics. First results will be presented with a proof-of-principle setup of a DTH and a prototype back-end board on the timing performance.

We will conclude with a brief look back at the design and production experience of the first DTH prototype boards, and a look forward to the next evaluation steps and future prototype boards and systems.

Authors: HEGEMAN, Jeroen (CERN); CMS CENTRAL DAQ GROUP

Presenter: HEGEMAN, Jeroen (CERN)

Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **64**   Type: **Poster**

GE1/1 Sustained Operations Investigations

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Ten "slice test" triple-GEM detectors were installed into the CMS endcap in 2017. Data was recorded in 2017-2018, using both cosmic ray muons and LHC collisions. During the slice test, a loss of VFAT2 input channels was observed, with two detectors exhibiting rapidly-increasing channel loss beginning mid-2018.

Concurrent investigations into the cause of the channel loss were launched, one using the in-situ data from P5, the other seeking to recreate the loss in the controlled setting of an external lab. Results from each investigation, and the steps that were taken to prevent such loss in the future, will be reported.

Summary

In this contribution, we will present the results of the investigations into the sustained operation of the triple-GEM (gas electron multiplier) detectors of the GE1/1 system, which is planned for installation into the Compact Muon Solenoid (CMS) in 2019-2020 (LS2).

Ten "slice test" detectors were installed into the CMS endcap in January 2017, as a proof of concept for the full GE1/1 system. These detectors are read out on the front end using 24 VFAT2 chips and a corresponding v2 optohybrid board, and from the back end utilizing a microTCA crate containing CTP7 and AMC13 boards. An additional two detectors were added in 2018, which represent the newer VFAT3-based design, which utilizes a split-GEB (GEM electronics board) and v3 optohybrid on the front end.

Data was recorded throughout the 2017-2018 runs, using both cosmic ray muons and LHC collisions. During the slice test, a loss of VFAT2 input channels was observed, with two detectors exhibiting rapidly-increasing channel loss starting from mid-2018.

Concurrent investigations into the cause of the channel loss were launched. One investigation used the in-situ data from P5, comparing the channel loss times with HV, LV, and current fluctuations, changes in magnetic field, and beam intensity. The other investigation sought to recreate the loss in the controlled setting of an external lab and examine four possible causes of the channel loss, including normal operation of the detector, improper operation of the detector, highly-ionizing background particles, and GEM foil discharges.

Results from each of these investigations, and the steps that were taken to prevent such channel loss in the future, will be reported in this contribution.

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Presenter: STARLING, Elizabeth Rose (Université Libre de Bruxelles (Belgium))

Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **66**
Type: **Poster**

Study of SEU effects in circuits developed in 110 nm UMC technology

Thursday, September 5, 2019 4:55 PM (20 minutes)

At INFN-Torino, ASICs for readout applications of detectors were designed in several technologies, and are now under development. The 110 nm CMOS UMC technology is applied too. This technology has been chosen for its lower cost with respect to IBM or TSMC, even if there was not a systematic characterization for what concerns the radiation tolerance. Obviously, it is important to know the behavior of this technology under radiation. For this reason, configuration registers of a full size prototype for the custom readout circuit of silicon double-sided microstrips of PANDA Micro Vertex Detector were tested with ion and proton beams.

Summary

The 110 nm CMOS UMC technology is one of the technologies used to develop ASICs for the readout of several detectors at INFN-Torino. In spite of its lower cost with respect to IBM or TSMC, its radiation tolerance has not been completely assessed.

First tests of Total Ionizing Dose for this technology have been done by the group of V. Re [E. De Riceputi et al., DOI:10.1109/PRIME.2017.7974152].

For that reason it is important to know the behavior of this technology under radiation and in particular to validate the use of the Triple Modular Redundancy (TMR) technique and Hamming Encoding (HE) to avoid the Single Event Upset (SEU) effects.

The circuit used to perform that evaluation is an ASIC prototype (named PASTA) developed for the readout of silicon double-sided micro-strips of the Micro Vertex Detector of PANDA experiment since it implements the two types of structures (TMR and Hamming Encoding) to be tested.

The full size prototype is a readout solution which uses the Time over Threshold (ToT) technique to determine the charge and time information.

It has 64 channels each containing three distinct building blocks: an analog front-end, an analog TDC and a digital TDC controller.

A fourth block, the global controller, is common to all channels and is used to collect the data from the channels and distribute the configuration.

A dedicated DAQ in LABView has been developed to configure the ASIC registers and acquire data.

The radiation tolerance of the configuration register is evaluated by the following procedure: a writing command is followed by a reading command until a SEU is detected showing an inefficiency of the protection circuit (TMR or Hamming Encoding technique), then the sequence starts again from the begin. The acquisition program counts the number of time when the bit changes its value (0-1, 1-0), allowing the estimation of errors which have been detected and corrected. A balanced sequence of 1 and 0 is used to evaluate also the different behavior of the circuits.

The configuration of each channel requires a sequence 42 bit long. The global configuration requires a sequence 172 bit long.

Two tests were performed, the first one at INFN-LNL using ions beams at the SIRAD facility and the second one at the experimental room of INFN-TIFPA, in the Centro di Protonterapia in Trento, with proton beam.

Several ions were used to obtain the cross section for SEU. Proton beams with different current

intensities were used to investigate the SEU effects as a function of particle flux.
The results will be presented.

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Presenter: CALVO, Daniela (INFN - National Institute for Nuclear Physics)

Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **67**   Type: **Poster**

Proton-Induced Radiation Effects in MAROC3, a full readout 0.35 μm SiGe ASIC

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The MAROC chip was dedicated to MaPMT readout, and its third generation was backup solution in the front-end electronics of the RICH-LHCb Upgrade. Given the expected radiation environment for RICH, the MAROC3 was tested with 35 MeV proton beam at the Nuclear Physics Institute in Juelich, Germany. Investigated samples had the behavior recorded using a dedicated test bench. An increasing in power consumption followed by a rapid annealing - which proceeds at room temperature –was observed. The threshold for TID effects was found between 50 - 100 krad TID (Si), for a TID rate of about 30-170 rad/s.

Summary

For the third and the fourth LHC runs, the LHCb detector will be upgraded to operate at much higher proton-proton collisions rate than the present. Both RICH subdetectors will have the photodetection system redesigned based on MaPMT sensors and the entire detector will benefit from a flexible software-based trigger system, while the RICH readout will be at 40 MHz LHC bunch collisions rate. Embedded in the sensors elementary cells, the front-end electronics of the RICH photodetection system should have a reliable operation in a harsh environment which is estimated to have up to 200 krad (Si) total ionising dose (TID). Among the ASICs considered in the redesign of photodetection system, it was included the MAROC3 backup chip. Therefore, an irradiation campaign was implemented to establish the radiation hardness of this device. Our group investigated the radiation hardness of MAROC3 using a 35 MeV proton beam from Julich Isochronous Cyclotron (JULIC) facility based at the Nuclear Physics Institute of the Research Centre Julich, Germany. A custom test bench was developed to monitor and record the device parameters even during sample irradiation. Two samples were irradiated up to 200 krad TID (Si) while a third one up to 400 krad (Si), with variable TID rate of about 30-170 rad/s. Increasing of power consumption on both digital and analogue blocks was observed due to the leakage current growth within semiconductor structure. Once the irradiation was stopped, a rapid annealing process decreased the power consumption at room temperature close to the baseline values. No permanent failure was seen in the ASICs functionality. Temporary impairments manifesting as changes in triggers efficiency were mitigated through annealing. The TID rate for the third sample was chosen almost six times larger than the rest, and after 200 krad (Si) the MAROC3 configuration was affected in addition to the TID effects, however the device recovered after one hour annealing at room temperature. The main transient problem was found in one of the digital to analog convertor (DAC0). We estimate no operation problems for this chip in an LHCb-like environment with about 0.008 rad/s TID rate.

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Presenter: Dr COJOCARIU, Lucian Nicolae (IFIN-HH (RO))

Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **68** Type: **Poster**

Calibration of Active Pixel Sensor based on TowerJazz 0.18 μm Technology with X-ray

Thursday, September 5, 2019 4:55 PM (20 minutes)

SUPIX-1 is the first version of high spatial resolution monolithic active pixel detector prototype led by Shandong University Pixel Group which serves for CEPC tracker system. The chip has 18μm epi-layer with the resistance of 1kΩ·cm using TowerJazz 0.18 μm technology. Each chip has 9 sub-matrices, 64 rows by 16 columns for each matrix, which gives 16 parallel analog outputs with rolling shutter readout mode, and the chip sensitive area is 2mm*7.88mm. The readout system is based on XILINX KC-705 FPGA board with PCI-e data transmission mode.And the pixel sensor gain was calibrated with Fe-55 K-α peak.

Summary

SUPIX-1 which taped out in 2016, is the first monolithic active pixel sensor prototype in Shandong University with TowerJazz 0.18 μm technology. This prototype serves for the Circular Electron Positron Collider (CEPC) tracker system. In order to calibrate the sensor gain of SUPIX-1, The data acquisition system was set up at Shandong University. The system consists: Device under test (DUT) board, which carries the chip under test. Main board, which convert the analog output from the chip under test to digital signal and the effective bits is 14. FPGA board, which encode the output from the main board and transmit the data to the PC disk through PCI-e protocol, the FPGA board used for the test system is XILINX KC-705. The sensor gain calibration was carried out with Fe-55 K-α and K-β peak. The analysis system for the data acquired is based on ROOT.

Authors: Mr LI, Long (Shandong University); Prof. WANG, Meng (Shandong University)

Presenter: Mr LI, Long (Shandong University)

Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **69**   Type: **Poster**

The eTx line driver and the eRx line receiver: two building blocks for data and clock transmission using the CLPS standard

Tuesday, September 3, 2019 5:20 PM (20 minutes)

This paper presents the design and test results for the line driver (eTx) and the line receiver (eRx) in the lpGBT, fabricated in 65 nm CMOS technology. The two circuits implement the physical layer of the bi-directional eLink interface of the lpGBT. The eTx is a single-ended-to-differential driver with programmable pre-emphasis and driving current. The eRx is a differential-to-single-ended receiver with programmable line equalization. Both circuits comply with the CERN Low Power Signaling (CLPS) standard and have been qualified for data transmission up to 1.28 Gbps.

Summary

The eTx and eRx circuits are part of the lpGBT chip that is used to implement multipurpose high-speed bidirectional optical links for high-energy physics experiments. The eTx and eRx implement the physical layer of the eLink interface in the lpGBT for data and clock transmission between the lpGBT and the front-ends. In this paper, we will discuss the designs, usages and test results of the eTx and the eRx, which have been fabricated in a 65nm CMOS technology and tested as part of the lpGBT.

The eRx block occupies an area of 210 ⬚m ⬚ 80 ⬚m including the eRx core, ESD circuits and on-chip decoupling capacitors. The eRx core is designed to accommodate a rail-to-rail input common voltage range (0 to VDD = 1.2V) and a differential amplitude between 140 mV and 800 mV. On-chip termination resistors and a default input common voltage (Vdd/2) can be enabled or disabled within the eRx to adapt to different system topologies including AC coupling and multiple drop configurations. A passive line equalization at the input of the eRx core provides four preset peaking transfer functions (including "flat-band"). Parallel PMOS and NMOS input differential stages are used to achieve rail-to-rail operation and a self-bias structure is employed in the eRx core to simplify the bias circuits. The whole eRx power consumption is 850 ⬚W (typical) when working at 1.28 Gbps.

The eTx block is designed to operate up to 1.28 Gbps for data transmission (extending beyond the lpGBT downlink eLink data rates) and up to 1.28 GHz for clock transmission. It adopts the Source-Series-Terminated (SST) structure for low power operation and outputs differential signals with 600 mV (VDD/2) common voltage and programmable differential amplitude between 200 mV and 800 mV (typically) when using an external 100 Ohm termination. The eTx also features programmable pre-emphasis. Both the peaking strength and the peaking time duration are programmable.

The lpGBT chip was taped out in July 2018 and testing has been conducted from April 2019. Both the eRx and eTx blocks were verified as part of the lpGBT and perform according to specifications. Besides discussing in detail the architecture of both circuits, the experimental results including those of the irradiation tests, that will take place during the Spring 2019, will also be presented during the conference.

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Presenter: GUO, Di (Southern Methodist University)

Session Classification: Posters

Track Classification: ASIC

Contribution ID: **70**   Type: **Oral**

Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain

Tuesday, September 3, 2019 9:50 AM (25 minutes)

An innovative CGEM (Cylindrical Gas Electron Multiplier) detector will upgrade the current inner tracker of the BESIII experiment.
A custom 64ch ASIC has been specifically designed for the analog readout.
The features of the engineering run version of TIGER will be presented alongside with the ASIC characterization and calibration.
The data are then collected via optical links by two different kind of FPGA-based modules, one in charge to interface the chip and the other deputed to event construction and DAQ communication.
The design of the electronics chain will be presented together with the first results of the integration tests.

Summary

BESIII is a high precision spectrometer in operation at Beijing Electron Positron Collider. Due to aging, it became mandatory to address the replacement of the inner drift chamber.
An innovative CGEM (Cylindrical triple Gas Electron Multiplier) tracker was proposed and built.
The detector is composed by three cylindrical layers, each one rolled, in turn, by three GEM multiplication foils. The signal is induced on a total of ˜10000 channels, read in analog mode.
TIGER (Torino Integrated Gem Electronics for Readout) is the read-out ASIC expressly designed for the CGEM tracker. This chip allows to perform a combination of two different reconstruction methods (charge centroid and micro-TPC), providing the analogue reading of the charge deposited on the CGEM strips.
Thanks to this kind of reconstruction, even with tilted tracks in a 1T magnetic field, the system can reach a spatial resolution of 130 μm, also in the z-direction, and a time resolution of 5 ns, with a strip pitch of 650 μm.
The chip specifications fully respect the design requests, providing a 60 kHz reading frequency for each of the 64 channels, 50 fC maximum input charge, less than 12 mW power dissipation per channel and 2000 e- rms noise for a sensor capacity up to 100 pF.
This ASIC integrates a charge sensitive amplifier (CSA) coupled with a two-branches shaper for each channel, optimized for charge and time measurement, followed by discriminators and ADC stages.
The time stamps are produced by time to digital converters based on an analogue interpolation technique with a quantization error better than 50 ps, while the charge measurement can be obtained with a Sample and Hold (SH) circuit or with a Time Over Threshold (TOT) system, selectable in configuration.
Four Time to Analog Converters (TAC) allow the SH to store more data hence lowering the pile-up probability.
The digital part of the chip also provides a full digital output for the event words and all the DACs and the logic needed for the voltage levels configuration. The configuration registers are protected against Single Event Upsets (SEU) caused by ionizing radiation.
The chip is manufactured in UMC 110nm technology, exportable to China.
The low voltage power supply, the configuration off each chip and the data collection will pass

through the off-detector GEM Read-Out Cards (GEMROC), 20 FPGA-based modules controlled via UDP protocol.

The data will then be streamed to other FPGA-based modules, the GEM Data Concentrator (GEM-DC), which will collect the data and transmit them to the BESIII DAQ system.

The developed electronic system can, in principle, be used for the read-out of other Micro Pattern Gas Detectors.

The features of the engineering run version of TIGER will be presented alongside with the full data acquisition chain and the progresses in its integration.

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Presenter: BORTONE, Alberto (Universita e INFN Torino (IT))

Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **71**   Type: **Oral**

eFEX preproduction module design and test

Wednesday, September 4, 2019 11:55 AM (25 minutes)

The Electron Feature Extractor (eFEX) is one of the core subsystems for the Phase-I upgrade of the ATLAS Level-1 Calorimeter Trigger. In Run 3, the eFEX will identify isolated e/g and tau candidates with much higher discriminatory power than in Run 2. The eFEX subsystem consists of 24 eFEX modules housed in two ATCA shelves. Each eFEX module has up to 200 optical input/output links and more than 400 on-board electrical fan-out links, all running at 11.2Gbps. Four pre-production modules have been made and tested. We present hardware and firmware design experience and test results from the eFEX pre-production modules.

Summary

The ATLAS Level-I Calorimeter Trigger Phase-I upgrade consists of three Feature Extractor (FEX) subsystems: eFEX, jFEX and gFEX. The function of eFEX is to identify the isolated energy deposits in the electromagnetic and hadronic calorimeters indicative of electrons, photons and taus. To cope with the increased pileup in Run 3, the eFEX runs more sophisticated algorithms with higher discriminatory power using finer-granularity calorimeter data to retain the trigger sensitivity to electroweak physics processes at low energy threshold.

In Run 3, the ATLAS front-end detector electronics will remain largely unchanged and the ATLAS Level-1 Trigger latency will still be limited to 2.5 us. The latency budget for the eFEX subsystem is only 13.5 Bunch Crossings (BC). To meet this tight latency requirement, all the eFEX algorithms are implemented in firmware running in modern FPGAs. The whole eFEX subsystem is divided into 24 eFEX modules housed in two ATCA shelves, and each eFEX module holds 4 algorithm processing FPGAs (XCV550T) and one control FPGA. Each module receives data on up to 136 fibre links (11.2 Gb/s) covering a calorimeter area of up to 1.7 x 1.0 (eta x phi). As the eFEX algorithms are based on overlapping windows, the majority of input high-speed links need to be fanned out electrically on-board to multiple FPGAs for the algorithm window environment data sharing, resulting in more than 400 differential high-speed links routed on a single eFEX module. The Trigger OBjects (TOBs) calculated by eFEX algorithms are merged and sorted across the whole module, and only the most energetic TOBs are sent to the L1Topo subsystem over up to 48 fibre links (11.2Gb/s). Upon each L1A, data are collected from various processing stages on the eFEX real-time path, formatted, and sent to L1Calo RODs. This readout function is important for trigger validation and trigger performance analysis. Each eFEX module sends its readout data over 8 electrical links (6.4Gb/s) on the ATCA backplane using multi-lane AURORA protocol, which provides enough bandwidth for both Phase-I and Phase-II readout requirements. The eFEX module control and configuration is done via the IPBus firmware implemented in the control FPGA, which isolates software maintenance issues from the eFEX hardware system. Mission-critical parameters of an eFEX module are monitored by the ATLAS DCS system via an on-board IPMC, which can shut down the module power to prevent hardware damage in case of critical errors such as over-voltage or over-temperature. Non-mission-critical parameters on a eFEX module are collected via IPBus and sent to DCS system.

Following the successful Final Design Review of the eFEX project in Dec 2018, four pre-production eFEX module have been designed and constructed, comprehensive firmware has been developed, and systematic integration tests have been done. This presentation will report the experience of

eFEX hardware and firmware development and the integration test results.

Author: COLLABORATION, ATLAS TDAQ

Presenter: QIAN, Weiming (Science and Technology Facilities Council STFC (GB))

Session Classification: Trigger

Track Classification: Trigger

Contribution ID: **72**   Type: **Oral**

A High Throughput Production Scale Front-End Hybrid Test System for the CMS Phase-2 Tracker Upgrade

Friday, September 6, 2019 9:00 AM (25 minutes)

More than twenty-five thousand hybrids will be produced for the CMS Tracker Phase Two Upgrade. The hybrids are assembled with flip-chips, passives and carbon-fibre stiffeners. They will be glued to their module supports, together with powering and optical transmission hybrids, making repairs almost impossible. Due to the complexity of the hybrid circuits and the circuit assembly, production scale testing is a very important aspect. A crate-based scalable test system was designed to enable a multiplexed test of front-end hybrids. A test card was produced for the 2S
hybrids and two different hybrid test cards are under development.

Summary

Ten different front-end hybrid variants for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High-Luminosity Large Hadron Collider (HL-LHC) are currently under development. The upgraded Tracker is based on two main types of modules, the strip-strip (2S) and
the pixel-strip (PS). The 2S modules contain two parallel strip sensors of 10 × 10 cm2 and two front-end hybrids connected to a service hybrid. The PS modules contain a strip sensor and a macro
pixelated strip sensor of 5 × 10 cm2 and two front-end hybrids connected to a power and a data service hybrid. These modules require state of the art High Density Interconnect (HDI) front-end hybrids assembled with fine pitch flip-chip front-end ASICs, connectors and passives.
The 2S front-end hybrids interface through a fine pitch connector with a service hybrid that contains
the power conversion and a Versatile Link Plus (VTRX+) based optical link connecting to the back-end systems. The PS hybrids have an additional interface with a Macro-Pixel Sensor ASIC assembly block (MAPSA) which is located externally. The proposed system tests the hybrids through these interfaces.
The test infrastructure is based on a 3U 19-inch sub-rack with custom developed multiplexer backplanes enabling the testing of twelve hybrid circuits in one crate. The backplanes are designed to multiplex high speed differential signals, USB, control lines and distribute power. Each sub-rack can fit three backplanes interconnected in series enabling the test with twelve hybrid plug-in cards. In this scheme, smaller systems can be assembled as well, down to four plug-in cards. The backplane connects to the FC7 data acquisition board, which controls the selection of plug-in cards and processes the data. The FC7 is connected through IPBus to a computer running the test

software. Performance of the backplane was characterized and validated for up to a clock frequency
of 640 MHz.
Specific plug-in cards are designed to test each main type of hybrid circuit. In order to avoid designing ten different plug-in card variants, the hybrids are mounted on interchangeable sockets and specific interconnection circuits are designed to connect them to the plug-in cards. The first edge card was designed for all six variants of the 2S hybrids. The card was qualified with the 8CBC3 prototype hybrid linked to a mezzanine hosting the concentrator ASIC (CIC). Two other

test cards are currently under development to test the PS optical readout hybrids (PS-ROH) and the
PS front-end hybrids.
The proceeding will present the design and topology of the test crate and the 2S test card. Results obtained with the 8CBC3 and the CIC Mezzanine will be shown. The design of the PS test card including the hybrid socket design will be presented. The test case for the PS-ROH hybrid will also be presented.

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Presenter: KOVACS, Mark Istvan (CERN)

Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability

Contribution ID: **73**   Type: **Poster**

Processing of the Liquid Xenon Calorimeter's Signals for Timing Measurements

Tuesday, September 3, 2019 5:20 PM (20 minutes)

For identification of neutron-antineutron pair production events in the CMD-3 experiment (BINP, Russia) near threshold is necessary to measure the particles flight time in the LXe-calorimeter with accuracy of about 3ns. The duration of charge collection to the anodes is about 5mks, while the required accuracy of measuring of the signal arrival time is less than 1/1000 of that. Besides, the signal shapes differ substantially between events, so the signal arrival time is measured in two stages. To implement that, a developed special electronics performs waveform digitization and OnLine measurement of signals' arrival times and amplitudes.

Summary

One of the goals of the Cryogenic Magnetic Detector (CMD-3) experiment (BINP, Russia) is a study of the hadrons production in electron-positron annihilation. An important example of such process is a neutron-antineutron pair production near threshold. A signature of this process is a large energy deposition in the barrel. In the barrel calorimeter the antineutron annihilation typically occurs by 5ns or later after beams collision. For identification of such events it is necessary to determine the time of signal appearance with accuracy of few nanoseconds. The arrival time measurement and recognition of antineutron annihilation must be accomplished On-Line in 1.1mks after the beam crossing so that the trigger signal can be generated in time for registration of this event. The liquid xenon based barrel calorimeter (LXe-calorimeter) consists of 14 cylindrical ionization chambers with anode and cathode readout, which are located co-axially at increasing radii. Each anode surface is divided in rectangular cells; the cells at all 14 anode surfaces are located so that the overlapping cells constitute stacks, or "towers", directed approximately to the interaction point. All anode cells of each tower are electrically connected, so the signals from those ionization chambers in which ionization was induced are added up. The sum signal of each tower is fed to a channel of electronics. The collection of electrons from the entire gap to the anode takes about 4.5mks. Thus, the typical signal of a tower is a current pulse with sharp rise and approximately linear fall; the total duration of the pulse is equal to the electrons collection time. However, the amplitude and shape of tower's signal in a particular event depends on the energy deposition and ionization clusters pattern in the volume of the tower. For providing the best signal-to-noise ratio, a charge sensitive amplifier is used at the front end of the electronic channel; therefore the amplified signal available for further processing has the rising edge as long as tower's signal, and the shape of this rising edge varies from event to event in correspondence with the shape of tower's signal. The duration of charge collection to the anodes is about 4.5mks, while the required accuracy of measuring of the signal arrival time is less than 1/1000 of that. Besides, the signal shapes differ substantially from event to event, so the signal arrival time is measured in two stages. At the first stage, the signal arrival time is determined with an accuracy of 1–2 discretization periods, and initial values of parameters for subsequent fitting procedure are calculated. At the second stage, the signal arrival time is determined with the required accuracy by means of fitting of the signal waveform with a template waveform. For the moment, the developed algorithm has been successfully implemented in hardware. The prototypes of new signal processing modules for LXe-calorimeter towers was manufactured and successfully tested at the detector. A obtained timing

resolution was close to the design value.

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Session Classification: Posters

Track Classification: Trigger

Contribution ID: **74**   Type: **Poster**

The trigger system for the electromagnetic calorimeter of the COMET experiment.

Thursday, September 5, 2019 4:55 PM (20 minutes)

The COMET detector will include a electromagnetic calorimeter (ECal). The ECal signals will used for energy deposition measurement and for triggering. For triggering, the calorimeters signals will transformed into special short-shaped analog signals. These signals will then digitally processed with special algorithm, which allows one to obtain a set of logic signals necessary for event selection and a time-tag signal for time alignment of time measurements.

The final design and performance of the front-end and trigger electronics of the electromagnetic calorimeter of the COMET experiment will be presented.

Summary

The COMET Phase-I experiment is seeking to measure the neutrinoless, coherent transition of a muon to an electron (mu->e) conversion in the field of an aluminium nucleus, mu-N -> e-N, with a single event sensitivity of $3.1*10\hat{}-15$. The COMET detector will consist of several subsystem, one of each will be electromagnetic calorimeter (Ecal). The Ecal system will consists of segmented scintillating crystals (LYSO). It is placed down-stream of the straw chamber detector and serves the following three purposes: to measure the energy of electrons (E) with good resolution, to add redundancy to the electron momentum (p) measurement and to provide the ratio E=p for electron identification. The Ecal will also provide an additional hit position to the electron track trajectory at the location of the Ecal, to cross-check the tracker-based electron trajectory. The Ecal also provides the trigger signals, carrying the timing with respect to which the electron events are referenced. Independent and redundant measurements of the energy of electrons are of critical importance to separate true signals of mu-N -> e-N conversion from background tracks that conspire to mimic a signal. For the photon readout will used avalanche photodiodes (APDs) with typical gains of 50–100. Due to lower gain of APDs compared with that of SiPMs, fast and low noise analogue electronics is required to amplify the APD signal. A preamplifier board was developed. The amplifier output is designed to be differential so that the signal can be transmitted over relatively long distances without suffering from noise. The front-end preamplifier board has 16 channel charge sensitive preamplifiers (CSPs) for the readout and 4 channel analog adders for the trigger. The ECAL consists of up to 2400 crystals in an approximately circular array. The trigger is required to give a good time resolution (to keep the readout windows around the trigger time as narrow as possible) and good energy resolution (so as to select energy clusters in the signal region rather than background). Since the energy deposition can be divided among couple crystals, it is necessary to do the summation. On the other hand, at E ˜ 100MeV, if from the entry point of particle to the boundary of the summation area is at least one crystal, then almost all energy will be summed. Thus, if we take the sum of 4x4 crystals, when the particle enters in the middle 2x2 crystal, effectively all the energy will be taken into account. It is therefore proposed to select the basic trigger unit (cell) the group of 2x2 crystals (corresponding to one crystal module of the ECAL), and to determine the total energy by using the sum of an array 2x2 trigger cells (i.e. 4x4 crystals). All possible combinations of the sums 2x2 trigger cells will calculated and the maximum energy found in one of these combinations will be used. Now this algorithm is implimented in pre-trigger board FPGA and whole front-end and trigger system successfully tested.

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Presenter: EPSHTEYN, Leonid (Budker Institute of Nuclear Physics)

Session Classification: Posters

Track Classification: Trigger

Contribution ID: 75

Type: **Oral**

Performance of LAUROC1, ATLAS Liquid Argon Upgrade ReadOut Chip

Tuesday, September 3, 2019 9:00 AM (25 minutes)

The analog front-end readout electronics of the ATLAS Liquid Argon (LAr) Calorimeter will be replaced by a single chip as part of the upgrades for the High-Luminosity Large Hadron Collider (HL-LHC) program. The cornerstone of the circuit is the very demanding preamplifier, which must have low noise (0.4 nV/√Hz), large dynamic range (up to 10 mA, 16 bits) and precise input impedance (25 or 50 Ohms) to terminate the cables from the detector. LAUROC1 is a prototype that integrates an innovative electronically cooled resistor architecture to fulfil these requirements. The design of the ASIC and testbench measurements will be presented.

Summary

The readout electronics of the ATLAS LAr Calorimeter must be upgraded for the HL-LHC phase, due to ageing, and to cope with the demanding radiation tolerance and trigger requirements coming from the very high event rates. The increased integrated luminosity also necessitates a larger dynamic range for the readout chain.

LAUROC1 is an ASIC designed in CMOS 130 nm that integrates four analog front-end channels. Each channel consists of a preamplifier followed by a High-Gain (HG) and a Low-Gain (LG) CRRC2 fully differential shaper. The two-gain shaper accommodates the large dynamic range of the LAr signals to the external 14-bit ADC. Their bipolar waveform optimizes the signal to noise ratio in the presence of the anticipated pileup and acts as anti-aliasing for the following 14 bits 40 MHz ADC.

The cornerstone of the analog Front-End is the preamplifier, which is current sensitive due to the long signal duration (600 ns) of the liquid argon pulse. The input impedance has to be precisely matched to the cable impedance bringing the signals out of the cryostat (25 and 50 Ohm). As always in calorimetry, the dynamic range is very large, with detector current reaching up to 10 mA, and the detector capacitance ranges from 400 pF to 2.2 nF. The dynamic range is split in two 14 bits ranges, with a gain ratio of 20 and a linearity better than 0.3 % on both ranges. The most stringent requirement is actually the very low noise, where the Equivalent Noise Current (ENI) must be smaller than 200 nA for a detector capacitance of 1.5 nF and a central frequency of around 10 MHz. This corresponds to a noise spectral density of 0.4 nV/√Hz, equivalent to a 10 Ohm resistor, hence the denomination of "electronically cooled resistor".

The ASIC incorporates 4 channels with tunable input impedance from 15 to 70 Ohms, with an accuracy of 1 Ohm. The maximum input current is also selectable, from 2 mA to 10 mA, depending on the detector sampling depth. The peaking time is adjustable by slow control, from 30 to 60 ns.

LAUROC1 was received in February 2019. While the linearity measurements over the whole dynamic range for both 25 and 50 Ohm configurations as well as input impedance tunings give good results, the measured noise is larger than simulations by 20% due to extra 1/f noise. As the input transistor has been measured separately with good 1/f performance, the extra noise seems to be due to the dielectric noise of the MIM capacitors, where a tan delta of 1E-3, compatible with data in literature, can explain the discrepancy. This noise source is rarely encountered and highlights the low noise levels reached.

LAUROC1 extensive performance obtained on test bench will be detailed in this presentation.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **76**   Type: **Oral**

SALT, a 128-channel readout ASIC for Upstream Tracker in the LHCb Upgrade

Thursday, September 5, 2019 10:40 AM (25 minutes)

SALT is a 128-channel readout ASIC, designed in CMOS 130˜nm process, for silicon strip detectors in the upgraded Tracker of LHCb experiment. It extracts and digitises analogue signals from the sensor, performs digital signal processing and transmits serially the output data. SALT uses the innovative architecture comprising of a low power analogue front-end and a 40˜MSps 6-bit ADC in each channel. The prototypes of SALT have been already tested confirming full chip functionality and fulfilling expected specifications. The design and results of test measurements will be presented.

Summary

Silicon strip detectors in the Upstream Tracker (UT) of LHCb experiment will be read out by a dedicated 128-channel ASIC called SALT.
SALT, designed in CMOS 130 nm technology, extracts, shapes and digitises analogue signals from the sensor, performs Digital Signal Processing (DSP) and transmits serially the output data.
It uses the innovative architecture comprising an analogue front-end and a 40˜MSps 6-bit ADC per channel. The front-end comprises a charge preamplifier and a fast (T_{peak}=25ns and almost symmetrical) non-standard shaper with complex poles and zeros in transfer function, allowing to distinguish subsequent signals at the LHC bunch crossings 40˜MHz rate. The front-end works with both sensor polarities for capacitances up to $\sim$ 20pF. The phase of the ADC sampling is controlled by a low power DLL.

Digitised data from each ADC channel are processed in the DSP block which subtracts pedestals, calculates the
mean common mode (MCM) and subtracts it in each channel. The last DSP step is zero suppression (ZS). After ZS the data are buffered in SRAM and sent in packets to DAQ via serial DDR e-links equipped with SLVS drivers. A low power PLL generates 160˜MHz clock for data serialization and fast 320˜Mbps DDR transmission circuitry.

SALT is a System-on-Chip type ASIC. Besides already mentioned blocks (front-end, ADC, PLL, DLL, DSP, SRAM, SLVS) it includes: calibration circuitry, reference voltage generators, various 5-8 bit DACs (for biasing, baseline, SLVS, calibration), monitoring ADCs (for PLL, DLL, DACs), variable number of active e-links, I2C block, TFC Timing and Fast Control block, etc…

Many tests have been already performed. First, the digital functionality (e-links, DSP, I2C, TFC, etc.) was positively verified. Next, analogue pulses were observed in analogue form in two test channels and then in all channels after ADC conversion (DLL was used to shift ADC sampling phase to reconstruct pulse shape). The measured performance well agrees with expectations. In next step the measurements were repeated with external capacitances/sensors connected to SALT inputs. In previous prototype large oscillations were seen when capacitance/sensor was connected. This problem was attributed to large internal parasitic inductances in the power network. Designing the present chip the main focus was on proper simulations of parasitic inductances. Measurements done with capacitance/sensor fully confirmed suspected inductance issue. Expected pulse shapes were observed with capacitance/sensor in test channels and in all channels after digitisation and pulse shape reconstruction. For analogue test channels SNR of $\sim$ 20 was measured with $\sim$ 10pF capacitance. For all channels, with largest sensor ($\sim$ 12pF/channel), first measurements

show SNR of about 12. The small pick-up of 40MHz is still present on the baseline but it is expected from simulations and it can be removed by MCM subtraction.

Presently the pre-production tests of larger system with multiple SALT chips on hybrids are on-going in order to verify whether the UT system specifications are fulfilled.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: 77   Type: **Oral**

ALTIROC1, a 25 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)

Wednesday, September 4, 2019 9:25 AM (25 minutes)

ALTIROC1 is a 25-channel ASIC designed to readout the 5 x 5 matrix of 1.3 mm x 1.3 mm x 50 μm Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD detector. The targeted combined time resolution of the sensor and the readout electronics is 50 ps/hit. Each ASIC channel integrates a RF preamplifier followed by a high speed discriminator and two TDCs for Time-of-Arrival and Time-Over-Threshold measurements as well as a local memory. This front-end must exhibit an extremely low jitter noise while keeping a challenging power consumption of less than 4.5 mW. Detailed measurements will be presented.

Summary

The expected increase of the particle flux at the high luminosity phase of the LHC (HL-LHC) will have a severe impact on jet reconstruction performance in the forward region.
A High Granularity Timing Detector is proposed in front of the Liquid Argon end-cap calorimeters for pile-up mitigation and for bunch per bunch luminosity measurements. This detector will cover the pseudo-rapidity range of 2.4 to about 4.0 and will be made of two double sided layers of Low Gain Avalanche Detectors (LGAD) with 1.3 x 1.3 mm2 pads. The aim is to provide a precision timing information for minimum ionizing particle with a resolution better than 50 ps over the entire detector lifetime.

To preserve the intrinsic time resolution of LGAD sensors (25 ps before irradiation for gain larger than 20), the front-end ASIC, ALTIROC, must exhibit an electronics jitter smaller than 25 ps for a MIP signal (10 fC for a LGAD gain of 20 and a capacitance of 3.4 pF). The impact of the 500 ps time-walk after correction using the Time Over Threshold (TOT) measurement, must remain negligible. The ASIC FE electronics is designed to cope with the high radiation levels (up to 4.5 MGy), while keeping a challenging power dissipation smaller than 4.5 mW/readout channel.

ALTIROC1 has been designed in CMOS 130nm to readout a 5x5 LGAD matrix with a complete on-pixel readout. The analog part consists of a 1 GHz RF preamplifier followed by a high speed discriminator, which are both critical elements for the overall electronics time performance. Each discriminator is followed by a TOA (Time-of-Arrival) and a TOT (Time-Over-Threshold) TDC as well as by a SRAM memory to store the digitized data.
The TOA is digitized over 7 bits with a bin of 20 ps and is done within a 2.5 ns window centred on the bunch crossing. A Vernier delay line configuration has been chosen to achieve the 20 ps quantisation step. The conversion is initiated only upon signal detection, enabling power saving.
The TOT measurement is digitized over 9 bits with a bin of 40 ps. The TDC employs an additional coarse delay line for extending the range to 20 ns while the Vernier delay line (identical to the one used in TOA TDC) provides the high resolution of 40 ps.
The total power consumption for both TDCs is 1.1 mW/channel assuming a maximal channel occupancy of 10%.
The memory is also custom designed to minimize the power dissipation to less than 0.5 mW/ch with a 10% occupancy. It has a width of 19 bits and a depth of 400 columns to provide the 10 μs L0 latency.

A first prototype, ALTIROC1_V1, was received in November 2018. It exhibits good performance, with a jitter of 25 ps using the full chain and a detector capacitance of 3.5 pF. A second prototype

with minor modifications, ALTIROC1_V2, is expected in June 2019.
The overall test bench characterization obtained with the ASIC alone as well as measurements performed with a bump-bonded sensor will be presented.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **78**   Type: **Oral**

Development of ultra-low power 10-bit SAR ADC in 65 nm CMOS technology

Thursday, September 5, 2019 10:15 AM (25 minutes)

The design and measurement results of different versions of ultra-low power fast 10-bit SAR ADC prototypes, fabricated in CMOS 65 nm technology, are presented. The prototypes use different capacitive DACs, different DAC switching schemes and different asynchronous logic. All prototypes are fully functional, achieving good linearity (with both INL and DNL below 1 LSB) and ENOB around 9.3 for sampling rates up to 60-90 MSps, depending on the ADC version. The power consumption is linear with sampling frequency and at 40 MSps it is between 450-600 uW.

Summary

In modern and future detectors for particle physics experiments a fast, ultra-low power, area-efficient Analog-to-Digital Converter (ADC) becomes an indispensable component needed to build complex multi-channel readout ASIC. This work presents the development of a 10-bit 60-90 MSps Successive Approximation Register (SAR) ADC meeting the above mentioned requirements and adapted to multi-channel implementation in readout ASICs.

A fully differential ADC architecture was chosen, comprising a pair of bootstrapped switches, a differential capacitive Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture is used to eliminate the static power while asynchronous logic eliminates a fast bit-cycling clock distribution. The implemented switching schemes (Merge Capacitor Switching and a scheme without common mode reference voltage, proposed by Sanyal and Sun) of capacitive DAC result in 93-96% switching energy reduction in comparison to conventional switching scheme. The minimal capacitor size together with a split DAC architecture was used to reduce the total DAC capacitance. Two versions of asynchronous control logic were implemented, focused either on smallest power or on fastest operation. The prototypes were fabricated in CMOS 65 nm technology, which has been proven to be a radiation hard technology. In the design some basic precautions have been taken (like not using minimum size transistors) to improve the ADC immunity to radiation damages. The ADC layout was drawn in 60 um pitch, with the length between 235-330 um, depending on the ADC version. This was done to facilitate the implementation of ADC in a multi-channel readout ASIC.

All prototypes have been tested confirming expected functionality. They achieve a good linearity with DNL and INL errors below 1 LSB and work up to 60-90 MSps sampling rates. Typically, the effective resolution ENOB of around 9.3 bits is measured at 40 MSps for input signal at 0.1 Nyquist frequency. It decreases slightly (~0.3) when going to maximum sampling rate. Power consumption is linear with sampling rate and at 40 MSps it is around 450 uW or 600 uW for the ADC with low or standard power asynchronous control logic, respectively.

In this presentation the architecture of the developed ADCs will be discussed together with differences in implementation in different versions. The complete set of measurements showing the static and dynamic performance will be also presented.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **80**   Type: **Poster**

CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The CMS electromagnetic calorimeter (ECAL) will be upgraded to maintain detector performance in the challenging environment of the High Luminosity LHC. The front-end readout electronics of the ECAL barrel will be replaced, while maintaining the existing crystals and avalanche photodiodes (APDs). Moreover, the upgrade will optimize the timing resolution of the system. The new front-end electronics consists of two cascading ASICs: a fast, dual gain trans-impedance amplifier (CATIA) and a dual ADC, designed in 130 nm and 65 nm CMOS, respectively. The latest test beam and laboratory test results of CATIA coupled with an ADC will be presented.

Summary

CATIA : APD readout ASIC for CMS phase 2 ECAL electronics upgrade.
The High Luminosity Large Hadron Collider (HL-LHC) program will provide about one order of magnitude of additional integrated luminosity than the current LHC program did after ten years. The
impact of the increased luminosity has been carefully taken into account for the current Compact Muon Solenoid (CMS) Electromagnetic Calorimeter (ECAL) barrel detector. Although the legacy crystals and avalanche photo-diodes (APD) will survive the challenging environment of the HL-LHC
with acceptable performance, the ECAL readout electronics must be upgraded to accommodate the
higher data rates. In addition, to deal with the increase in hit density, CMS is adopting a new strategy
for the selection of data by the Level 1 trigger by extending the data retention latency and increasing
the granularity by using single crystal information.
The ECAL barrel readout electronics are being completely redesigned to deal with the bandwidth limitation and increase of Level 1 trigger latency. The new ECAL electronics topology is designed for a continuous readout of the detector, displacing to the back-end electronics the Level 1 trigger generation and buffering. Fitting the continuous readout system, the proposed solution for the front-
end electronics is a cascade of two custom Application Specific Integrated Circuits (ASICs) : a fast, dual gain trans-impedance amplifier (TIA) —named CATIA—designed in a 130 nm CMOS process and a 12-bit, 160 MSPS dual analog to digital converter (ADC) implementing gain selection and data
compression, designed in a 65 nm CMOS process.
Between legacy APD and a new ADC, CATIA has to fulfill the constrains of both old and new electronics system. On one hand, the readout ASIC has to achieve an integral non-linearity (INL) better than ± 0.1 % over 2 TeV of dynamic range. The noise level of the new front-end has to cope with the expected increase of APD leakage current and the loss of transparency of the crystals due to aging. On the other hand, the continuous readout requires the new front end to deliver to the back

Contribution ID: **81**   Type: **Poster**

First results of CIC data aggregation ASIC for the future CMS Tracker

Thursday, September 5, 2019 4:55 PM (20 minutes)

The Concentrator Integrated Circuit ASIC is a front-end chip for both Pixel-Strip and Strip-Strip modules of the future Phase-2 CMS Outer Tracker upgrade. It collects the digital data coming from eight upstream front-end chips, formats the signal in data packets containing the trigger information from eight bunch crossings and the raw data from events passing the first trigger level, and finally transmits them to the LpGBT unit. A first prototype in a 65nm CMOS technology integrating all functionalities for system level operation, CIC1, has been tested in early 2019. The design and its implementation, along with test results, are presented.

Summary

The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). A first prototype in a 65nm CMOS technology integrating all functionalities for system level operation, CIC1, has been tested in early 2019. The design and its implementation, along with test results, are presented, along with the current development of the final CIC version. The future tracker detection module, named pT-module, is a key element of the future detector.The most internal areas will be equipped with so-called PS module (pixels/strips), of greater granularity.

The basic principle, two silicon layers separated by a few mm, is relatively standard in current tracking detectors. Readout electronics, on the other hand, is entirely new. Indeed, as can be seen in the figure on the right, the signal of the 2 layers can be put in coincidence in the module itself, therefore allowing a significant reduction of the detector output data rate. This coincidence is performed by 2 very front-end ASICs types: CBC and MPA for 2S and PS modules respectively. Each pT-module contains 16 such ASICs.
The Concentrator Integrated Chip (CIC) performs a further data compression stage. The CIC is a fully digital ASIC that must be compatible with 2 different modules flavours.

The integrated circuit receives information from 8 identical MPAs or CBCs, it reformats these data, processes them, and groups them in packets before the send to another ASIC that transmits the signal outside the detector. Each pT-module will contain 2 CICs, so there will be about 30000 CICs in the future tracker.

In order to validate the CIC model, a first version was developed and implemented, along with a complete standalone testbench. The CIC1 incorporates all the functionalities of the final chip and has the same footprint for the card wiring. The main difference is that the radiation hardness techniques were not used for its design, whereas it will be the case for the final version.

First CIC1 samples were received in February 2019. Thanks to the test system presented previously, it was possible to rapidly verify the correct functioning of the ASIC: the processing of the data received corresponds to the specifications. Detailed power measurements were performed in order to characterize the architecture.

The results observed so far are very encouraging for the future: the next stage of the project is the completion by the end of 2019 of a pre-production version of the ASIC, the CIC2. This chip will be resistant to radiation and will include modifications to reduce the nominal consumption. The final output of the 30,000 CICs that will be installed in the future tracker is planned for 2020.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **82**　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Design of the Back end card for the JUNO experiment

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Jiangmen Underground Neutrino observatory (JUNO) is a neutrino medium baseline experiment constructing in China, with the main goal to determine the neutrino mass hierarchy. A large liquid scintillator volume instrumented by around 20000 large photomultiplier tubes will detect the antineutrinos issued from nuclear reactors.The JUNO electronics system has mainly two parts: the front-end system inside water,the backend system outside water. For the front-end electronics, global control units (GCU) digitize the analog signals and send out event data as well as trigger requests. The BECs are used to collect the trigger requests from GCUs and process for next trigger decision step.

Summary

The JUNO experiment:
The Jiangmen Underground Neutrino Observatory (JUNO) [1] is a neutrino medium baseline experiment in construction in China, with the goal to determine the neutrino mass hierarchy and perform precise measurements of several neutrino mass and mixing parameters [2,3]. The experiment uses a large liquid scintillator detector aiming at measuring antineutrinos issued from nuclear reactors at a distance of 53 km. The 20 ktons of liquid scintillator contained in a 35 m diameter acrylic sphere is instrumented by more than 17000 20-inch photomultiplier tubes (PMT). Two vetoes are foreseen to reduce the different backgrounds: a 20 ktons ultrapure water Cerenkov pool around the central detector and a muon tracker installed on top of the detector.

The JUNO electronics readout:
One of the innovative aspects of JUNO is its electronics and readout concept [1]. The JUNO electronics system can be separated into mainly two parts: (i) the front-end electronics system performing analog signal processing (the underwater electronics), and (ii) the back-end electronics system, sitting outside water, consisting of the DAQ and the trigger system. 2 100-meters Ethernet cables and 1 coaxial cable are used to link the two parts. One Ethernet cable as DAQ and slow control link, the other one as trigger link, and the coaxial cable is for the power delivery. At the front-end part, a custom designed PCB called GCU (global control unit) [4] will digitize the incoming analog signals from 3 PMTs with custom designed high speed ADC (analog to digital converter). . The GCU will store the data signals in a large local memory under the control of the FPGA (Field-Programmable Gate Array) waiting for trigger decision. The CGU will send and receive the trigger requests and acknowledgments to and from the outside-water system, and in case of positive trigger acknowledgment, it will also send out the corresponding event data to DAQ system.

The Back-End Cards:
The back-end card (BEC) is designed to handle the trigger link. Each BEC will receive the trigger request signals from 48 underwater boxes, and in total of about 150 back-end cards are needed. The BEC is used as a concentrator and the incoming differential trigger request signals will pass an equalizer for compensating the attenuation due to the long cable. An FPGA mezzanine card (FMC), called TTIM, sitting on the BEC will align the received trigger request signals to a certain system clock, make a sum, and send the result to the trigger system over an optical fiber. A 62.5 MHz system clock will be distributed to all the GCUs from the BECs. Besides, IEEE1588 is used to synchronize the two parts to a level of 8 ns.

[1] JUNO Collaboration, "Conceptual Design Report", arXiv:1508.07166, Instrumentation and De-

tectors, 328 pages

[2] JUNO Collaboration, "Neutrino Physics with JUNO", arXiv:1507.05613, J.Phys. G43 (2016) 030401

[3] Yu-Feng Li and al., "Unambiguous determination of the neutrino mass hierarchy using reactor neutrinos",
arXiv:1303:6733, Phys. Rev. D88 (2013) 013008

[4] D. Pedretti , "The Global Control Unit for the JUNO front-end electronics", TIPP2017,
http://indico.ihep.ac.cn/event/6387/session/52/contribution/192/material/slides/0.pdf

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 83

Type: **Oral**

Integration, Commissioning and First Experience of ALICE ITS Control and Readout Electronics

Wednesday, September 4, 2019 9:50 AM (25 minutes)

For the third running period of the CERN LHC, the ALICE experiment will undertake several upgrades of its sub-detectors. One of the detectors to be upgraded is the Inner Tracking System, featuring the new ALPIDE pixel chip. Control and readout of the 24120 chips are handled by 192 custom FPGA-based readout units. Each readout unit can forward 9.6Gbps of data to another custom PCIe card that aggregates the data from several units and transmits it for further offline/online analysis. Integration and commissioning of the system is underway and this paper describes the first experiences and results of this effort.

Summary

During the ongoing Long Shutdown 2 of the CERN LHC, the ALICE experiment will replace the existing Inner Tracking System (ITS), which is based on silicon strip sensors, silicon drift sensors and silicon hybrid pixel sensors, with a completely new detector based on Monolithic Active Pixel Sensor (MAPS) technology. 24120 ALPIDE pixel sensors are mounted onto 192 azimuthally overlapping staves arranged into seven coaxial cylinders of increasing diameters, providing improved tracking and event-rate capability compared to the previous detector. The cylinders are separated into inner and outer barrel, consisting of three and four cylinders, respectively. The aim of the upgrade is to be able to handle 50 kHz Pb–Pb interaction rate and 200 kHz pp interaction rate. However, the current design is aimed at achieving double the rate for Pb–Pb and 1 MHz for pp.

Trigger distribution, readout, control, power management, and monitoring (voltages, currents, and temperatures) of the sensors is handled by 192 custom FPGA-based Readout Units (RUs) based on a Xilinx UltraScale FPGA, one per stave. The RU can operate both in triggered and continuous readout mode, whereas in continuous mode the RU generates the triggers to the sensors internally. Three optical transceivers, each supporting a maximum throughput of 3.2 Gbps, connects each RU to the Common Readout Unit (CRU) hosted in the First Level Processor (FLP). Each FLP can host up to four CRUs and each CRU can receive data from up to eight RUs.

Assembly of the detector, both inner and outer barrel, is well advanced and the commissioning of the complete readout chain, with all final systems, has started. This paper will present the performance of the full system in terms of readout-rate capabilities in both triggered and continuous readout mode under different running conditions: at low detector occupancy and high rates, simulating running with pp interactions at rates up to 1 MHz, and at high occupancy and low rates, simulating Pb–Pb minimum bias collisions at rates up to 100 kHz.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **84**
Type: **Oral**

picoTDC: A 3ps bin bize 64 channel TDC for HEP experiments

Wednesday, September 4, 2019 9:00 AM (25 minutes)

We present the ASIC development and test results of the picoTDC, a 64 channel time tagging TDC with 3ps bin size. The ASIC runs from a single 40MHz reference clock, can be configured very flexible, supports hit rates of up to 320MHz per channel, internal buffering and trigger matching as well as TOT measurements. A prototype has been produced in a 65nm CMOS technology and first test results show a single-shot RMS resolution better than the bin size (3ps).

Summary

A 64 channel time tagging Time-to-Digital Converter (TDC) ASIC with 3ps bin size, the picoTDC, has been implemented, submitted and tested.

In the picoTDC, an external 40MHz reference clock is fed to a PLL generating an internal 1.28GHz reference. This reference is split into 256 phases through a 64 element DLL and a resistive interpolation resulting in the 3.05ps bin size. These clock phases then drive the capture registers of the 64 channels. To reduce the power consumption, the resistive interpolation can be disabled resulting in a bin size of 12.2ps.

The TDC can digitize one edge in each 1.28GHz clock cycle (781ps) which are then (through a small derandomizer) fed to a channel buffer which can hold 512 hits per channel. The digital logic of the ASIC (including the memories) is clocked at 320 MHZ which is thus the maximum hit rate that can be sustained from each channel to the channel buffers. The readout interface consists of four eight bit parallel interfaces with up to 320MHz data rate, resulting in a maximum readout rate of 10GBit/s or 320 million hits per second for the whole ASIC. In order to reduce the required readout bandwith, a trigger functionality is implemented to read out only the interesting hits. For applications where this is not feasible, the data can also be read out triggerless. The ASIC also supports pairing of leading and trailing edges to a TOT measurement in order to reduce the readout bandwidth.

The TDC has been prototyped in a 65nm CMOS technology. First test results show an effective single-shot RMS resolution better than the bin size (including measurement jitter), but a higher mismatch between bins than anticipated. For the submission of the final production version the mismatch will be improved.

This paper discusses the circuit architecture, its principles of operation, test results and their implications from the prototypes as well as improvements for the production version. Detailed measurements and functional tests will be available at the time of the conference.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **85**   Type: **Poster**

Analog front-end characterization of the RD53A chip

Tuesday, September 3, 2019 5:20 PM (20 minutes)

For the Phase-2 upgrade of ATLAS and CMS tracking detectors, a new pixel readout chip, with 50x50 um2 pixel pitch, is being designed in 65 nm CMOS technology by the RD53 collaboration. A large-scale demonstrator chip called RD53A, containing design variations in the pixel matrix, among which three different analog front ends, is now available. A dedicated program of testing and detailed characterization has been devised and carried out to qualify the three front ends in terms of key performance parameters for the operation of a pixel detector at HL-LHC.

Summary

The Phase-2 upgrades of silicon pixel detectors at HL-LHC experiments will have to cope with extreme operating conditions, such as unprecedented radiation levels and high hit and trigger rates. In order to face such challenging requirements, a new generation of pixel readout chip is being designed in 65 nm CMOS technology, thanks to a joint effort between ATLAS and CMS, called RD53 collaboration.

As an intermediate step towards the final implementation, a large-scale demonstrator chip has been designed and called RD53A. The chip size is 20.0 mm by 11.8 mm and the pixel matrix is composed of 400 x 192 pixels, with 50 x 50 um2 pixel pitch. RD53A is not intended to be a production IC for use in an experiment, since it contains design variations in the pixel matrix, among which three different analog front ends.

An analog front end is one of the most crucial parts of a readout chip, as it collects the signal directly from the detector and translates it into the digital world. In the RD53A chip three substantially different analog front-end flavors, designed independently, were implemented. They are called linear, differential and synchronous front end. All three of them have the same calibration injection circuit and use the time-over-threshold technique, to provide a measurement of the signal amplitude.

All three front ends (FE) are based on a charge-sensitive amplifier. The linear and the synchronous FE use a krummenacher circuit for the feedback loop, featuring also the leakage current compensation, while the differential uses a simple MOS in the feedback for continuous reset and a low-pass filter for the leakage current compensation. Moreover, the differential FE uses a differential gain stage in front of the discriminator and implements a threshold by unbalancing the two branches. Both linear and differential FEs have a time-continuous discriminator with per-pixel trimming DAC for threshold tuning. The synchronous FE has a synchronous discriminator and is using an innovative technique, called autozeroing, consisting in a periodic acquisition of the baseline to avoid the need of trimming DACs. Finally, while the linear and differential FEs use the master 40 MHz clock to measure the time over threshold, the synchronous one can optionally use a local oscillator as a fast clock.

In this talk we will present the dedicated testing program established to qualify the three front ends in terms of key performance parameters, such as low threshold operation and threshold dispersion, preamplifier speed, power consumption, noise occupancy and time response. This testing program is expected to allow the CMS collaboration to choose the design of the front-end amplifier for the production readout chip, well before the TWEPP conference, and therefore the most relevant test results leading to this choice (performed on chips bonded to sensors and operated at cold temperature) will be presented.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **86**   Type: **Oral**

A Reconfigurable Monolithic Active Pixel Sensor for Digital Electromagnetic Calorimetry

Wednesday, September 4, 2019 2:00 PM (25 minutes)

Here we describe the DECAL Monolithic Active Pixel Sensor (MAPS) for digital electromagnetic calorimetry. The sensor consists of a matrix of 64x64 55um pixels, and provides a readout at 40MHz of the number of particles which have struck the matrix in the preceding 25ns. It can be configured to report this as a total sum across the sensor (equivalent to the pad of an analogue calorimeter) or the sum per strip (equivalent to a traditional strip detector). Design and operation of the sensor is described, and the results of chip characterisation are reported and compared to simulations.

Summary

Calorimetry is an important technique for the determination of the energy of incident particles in a detector. A small fraction of electromagnetic calorimeters are silicon-based devices, with the largest example under construction [1], and use layers of a dense absorber material (such as iron or tungsten) interleaved with silicon as the detecting material. Particles incident on the absorber initiate showers of lower energy particles, which deposit energy in the detecting layers. The total charge deposited in each detector layer is then summed and read out. By performing this operation for each detector layer, the energy of the initial particle can be determined.

However, it has been suggested that a digital approach can lead to higher energy resolution [2]. In contrast to an analogue calorimeter, which counts the total deposited energy in a given volume, a digital electromagnetic calorimeter is segmented and counts the total number of particles passing through said volume.

Monolithic Active Pixel Sensors (MAPS) are well placed to be the technology of choice for such a detector, since they have the potential to offer good integration of the complex circuitry required for counting, good radiation tolerance, and low cost (thanks to the rapid commercial development of this technology).

In this talk, we will report details and results of the DECAL sensor –a MAPS device for digital electromagnetic calorimetry. DECAL was designed and fabricated in a 180nm commercial CMOS process. It has a matrix of 64x64 pixels with 55um resolution and can be read out at a rate of 40MHz using 16 LVDS channels. Each pixel contains a pre-amplifier, shaper and comparator, as well as trimming logic for individual threshold calibration of the pixels. To perform the digital calorimetry function, each column contains logic to calculate the total number of hits in a column, and the chip sums the hits from each column to provide the total number of hits across the chip. As a further feature, the chip can be reconfigured between "pad mode" in which it behaves as just described, and "strip mode". In "strip mode", the chip reports number of hits on a per column basis, behaving more like a traditional strip detector. This could allow standardisation of components between the calorimeter and tracker in a future detector, by using the same reconfigurable chip. To allow operation at the required 40MHz rate (equivalent to the bunch crossing time of the LHC), the operation of the chip is pipelined. Particle detection, column summation and chip summation each require 25ns and occur simultaneously for consecutive bunch crossings.

We will also report the results of chip characterisation, (functionality of the digital logic, analogue pixel performance and operation of the trimming circuitry). Digital operation is shown to be as expected, and measurements of the analogue performance are compared to SPICE simulations.

[1] M. Valentan, The CMS high granularity calorimeter for the high luminosity LHC, Nuclear Inst.

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[2] Dauncey, Paul. (2011). Performance of CMOS sensors for a digital electromagnetic calorimeter. 502. 10.22323/1.120.0502.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **87**　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Methods for Clock Signal Characterization using FPGA Peripherals

Thursday, September 5, 2019 4:55 PM (20 minutes)

Reliable measurement of clock signal parameters is important in precise-timing applications. Such parameters include frequency, phase, duty cycle and channel-to-channel skew. Especially in applications in which test time for multiple channels is a significant factor, efficient parallelization of measurements is crucial, while often coming with significant extra cost. This work presents an approach to characterizing clock signal parameters using off-the-shelf FPGA evaluation hardware. Approaches for both static measurements (steady-state behaviour) as well as dynamic measurements are presented. Both presented measurement concepts are applied in practice and their achieved performance is presented.

Summary

The dynamic clocking architecture of modern FPGAs combined with their flexible reconfiguration options allows using them to implement high-performance measurement systems replacing commercial test equipment without requiring complex external circuitry. This work presents two methods that can be used to characterize clock signals.

The first method presented allows estimation of static signal parameters for clocks synchronous to a reference clock. It implements an equivalent-time sampling concept by dynamically reconfiguring FPGA PLLs to acquire high-resolution measurements of signal phase (skew), duty cycle and jitter.
The DUT clock signals are sampled using a phase-shifted clock by fabric flip-flops, producing single-bit-quantized outputs. By collecting multiple samples, a measure of probability of the clock signal being high is estimated for each sampling phase offset. The implemented design using the PLLs available in Virtex 7 FPGAs achieves sampling phase increments of 28 ps, dictating the fundamental measurement resolution. By post-processing the acquired data, the temporal resolution can be improved further and additional information about clock jitter can be extracted. Due to the simple architecture and low resource requirements, multiple channels can easily be implemented in a single FPGA.

The second method presented in this work allows transient phase measurements on arbitrary clock signals. It is shown how the Multi-Gigabit transceivers of Virtex-7 FPGAs can be used for this application. Configuring the integrated GTX receivers in a mode where the deserializer operates from a fixed reference frequency (without a CDR being engaged) allows deserializing clock signals with high oversampling ratios, allowing for precise phase measurements without dead time. Multiple measurement channels can be implemented by simply using multiple hardware GTX instances without sacrificing resolution. One of the advantages of such an implementation is that data acquisition can be deterministically synchronized to other FPGA-based components of a test system, which is hard to achieve with external test equipment. FPGA logic can be used to control data acquisition of these signals, for example triggering on phase transients can be done when characterizing PLL circuits. By implementing a modified processing logic in the FPGA fabric, the GTX receivers can also be easily repurposed to operate as a TDC. With the Virtex 7 FPGA series receivers supporting bit rates up to 10.51 Gbit/s, time resolutions of 95 ps can be achieved with very good linearity and without any dead time.

The presented methods were integrated into the test system used for the lpGBT ASIC. The method for static determination of clock signal parameters is used in production testing, where it allows

to measure the characteristics of all 28 ASIC clock outputs at the same time and can test them for expected functionality and performance. The dynamic phase measurement implementation was used during two SEU test campaigns and facilitated detection of small phase transients that would have otherwise been detected only with dedicated high-speed test equipment.
Both methods will be discussed at the workshop and the experimental results presented.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **88**   Type: **Oral**

TCLink: A Timing Compensated High-Speed Optical Link for the HL-LHC experiments

Tuesday, September 3, 2019 2:25 PM (25 minutes)

The High-Luminosity Large Hadron Collider (HL-LHC) will pose unprecedented requirements in terms of timing distribution. The overall stability has to reach picosecond-levels between tens of thousands of end-points. To mitigate long-term environmental variations in the high-speed optical links, phase monitoring and online/offline compensation might be necessary. The Timing Compensated Link (TCLink) is a protocol-agnostic FPGA core that provides monitoring and picosecond-level phase adjustment capabilities. The features can be customized for different user application requirements. A proof-of-concept of TCLink on a setup composed by a Xilinx FPGA evaluation board, the Versatile Link+ and the lpGBT test chip will be demonstrated.

Summary

In order to cope with the high-levels of pile-up expected in the High-Luminosity Large Hadron Collider (HL-LHC), the CMS and ATLAS experiments will use timing information to distinguish between different collisions. This poses challenging requirements in the timing distribution network not to jeopardize the performance of the high-resolution timing detectors which will be installed in the experiments. The stability of the timing distribution network has therefore to reach picosecond-levels.

The baseline timing distribution in the HL-LHC experiments consists of thousands of high-speed optical links responsible for delivering the Timing, Trigger and Control (TTC) information. The back-end part (where no radiation is present) of the timing distribution network is usually represented by FPGAs having multiple transceivers coping with Gbps data-rates. Their front-end counterpart is the radiation-hard low-power Gigabit Transceiver (lpGBT) ASIC, a key player to deliver the TTC signals to the front-end chips.

In 2018, CERN has launched the High-Precision Timing Distribution (HPTD) interest group to study the short- and long-term timing stability performance of different timing components present in the baseline scheme to ensure they can cope with the stringent timing requirements posed by HL-HLC. Studies on the short-term stability of a Versatile Link+ and lpGBT based high-speed optical link have shown that a sub 5-picosecond rms level can be reached. However, long-term stability performance was not yet discussed at that time.

Long-term stability due to environmental variations such as temperature might play a key-role in the overall timing distribution stability. The monitoring and online/offline compensation of the phase of the lpGBT clocks might be necessary in order to reach the picosecond-level requirements.

As part of the HPTD project, the Timing Compensated Link (TCLink) concept was developed. The TCLink is a protocol-agnostic FPGA core envisaged to mitigate long-term variations in high-speed optical links. The concept is to have monitoring and picosecond-level online adjustment capabilities which can be tailored by the user to best fit his/her own convenience and application requirements.

In this paper, a proof-of-concept of the TCLink based on a Xilinx Ultrascale+ FPGA evaluation board, the Versatile Link+ and the lpGBT test chip will be demonstrated. Temperature variations in the different parts of the system (FPGA, fiber and lpGBT) are emulated with a climate chamber

and its effects are discussed.

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Session Classification: Optoelectronics and Links

Track Classification: Optoelectronics and Links

Contribution ID: **89**   Type: **Poster**

X-ray measurements of the effects of radiation damage in the miniMALTA DMAPS prototype

Thursday, September 5, 2019 4:55 PM (20 minutes)

We present tests with a scanning micro-focus photon beam of the miniMALTA DMAPS prototype developed for ATLAS ITk. Tests were carried out at Diamond Light Source which provided a 2um beamspot to be scanned in 1um steps. This allows the in pixel efficiency to be measured directly with high statistics. Three pixel design variations were measured, the standard design, a deeper p well design and an n gap design. This was repeated for an unirradiated chip, a neutron irradiated device and three proton irradiated samples. We compare the effect of different levels of radiation damage on the different pixel designs.

Summary

This contribution presents the results of investigations into the effects of radiation damage on different pixel designs included in the miniMALTA depleted monolithic pixel sensor prototype. MiniMALTA is a prototype test chip developed for the ATLAS ITk project, and contains a number of different pixel designs. We carefully studied the effect of radiation damage for three of these pixel sub matrices in this series of measurements. These were the standard MALTA baseline design, and two variant designs, one with an increased depth of the p-well, and one with a gap in the n-type layer. We used an 8keV micro-focus beam at the Diamond Light Source facility's B16 beamline to scan the pixels with a 2um beam spot in 1um steps to produce a measurement of in-pixel efficiency. An 8 keV beam energy was selected as this best matched the measured energy deposition from a minimum ionising particle in the depleted layer of miniMALTA. We tested chips that had suffered no radiation damage, 1e15 n/cm2 neutron damage, and three chips that had suffered proton damage from 27MeV protons at the Birmingham cyclotron at 7e14 and 5e14 n/cm2. We present and discuss the effect of these different damage levels on the three different pixel designs (MALTA, 'n-gap' & 'p-well'). We analyse the shape of the resultant charge collection efficiency maps, how the damage influences it, and how it is linked to the shape of the underlying collection nodes. We also discuss the effect of radiation damage on the absolute efficiency of the pixel and its effect on the charge sharing region between neighbouring pixels.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **90**
Type: **Poster**

The powering concept of the CBM Silicon Tracking System

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The presentation summarizes the powering concept of the Silicon Tracking System for the future CBM experiment at FAIR/Germany. Efficient powering is an important task with the goal to minimize power dissipation and heat development. Also the limited space for power cable routing has to be taken into account. Chosen solutions determine the necessary cooling and cabling effort and therefore have high impact to system integration. Some aspects are already completely solved while other issues have to be further investigated. The current status concerning powering the STS electronics and the subsequent consequences for system integration will be shown.

Summary

The Silicon Tracking System (STS) detector, which is the main part of the CBM experiment at FAIR/GSI Germany, comprises 9 units that make up 8 detector planes of 900 double sided 300um thick silicon detectors.
The units of the STS will be installed in a thermal enclosure inside a strong magnetic field of 1 T together with the front-end part of the readout electronics and a part of the powering system. Each STS-unit consists of two halves which will be moved independently of each other and supplied with low voltage, sensor biasing high voltage, optical fiber for the readout, cooling medium tubing, controls etc. The base structure of one half-unit is a C-shaped aluminium cooling plate which serves as mechanical support for components like cooling shelves and detector holding ladders. The low-voltage conditioning system as well as the readout electronics will consume many kilowatt of electric energy in a volume of very few cubic meters. This circumstances force the team of developers to optimise energy consumption of electronics on one hand and cooling efficiency on the other. The requirement of the construction foresee separate low voltage powering for readout of each side of every detector, thus the space restrictions inside the thermal enclosure as well as surface available only on the front wall of the box for mounting are critical. According to the simulations the components will absorb a dose of 10 kGy in their life time what poses certain requirements on all system components. Last but not least: assumed mechanical accuracy for the Silicon Tracking System imposes construction solutions which assure mechanical precision and will stand thermal cycling for years of usage.
The overall concept as well as electrical and mechanical details of the system will be discussed.

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Session Classification: Posters

Track Classification: Power, Grounding and Shielding

Contribution ID: **91**   Type: **Oral**

The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC

Tuesday, September 3, 2019 11:55 AM (25 minutes)

The Low-Power Gigabit Transceiver (lpGBT) is a radiation tolerant ASIC for multipurpose high-speed bidirectional optical links in HEP experiments. It supports 2.56 Gbps for the downlink and 5.12 or 10.24 Gbps for the uplink. Its data interface to the detectors'frontends is highly configurable supporting multiple data rates. The lpGBT is a fixed and deterministic latency device that can be used for trigger and timing distribution. It features control interfaces and environmental monitoring functions to implement experiment control.

The device was fabricated in a 65 nm CMOS technology. This paper discusses the lpGBT architecture and experimental results.

Summary

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC tailored to implement multipurpose high-speed bidirectional serial links in High-Energy-Physics experiments. It supports data transmission at 2.56 Gbps for the downlink (counting room-to-detectors) and at 5.12 or 10.24 Gbps for the uplink (detectors-to-counting room). It interfaces with frontend devices through an ad hoc electrical interface called eLink. This interface is highly flexible supporting multiple serial links with configurable data rates ranging from 80 to 320 Mbps for downlinks and 160 to 1280 Mbps for uplinks. Due to its fixed and deterministic latency design, the lpGBT can be used for timing distribution including precise trigger commands and clock signals. All 32 clock outputs are frequency programmable (40 to 1280 MHz) with four of those being additionally programmable in phase with 50 ps resolution.

In order to facilitate the usage of the chip in low mass systems, where lossy and low-bandwidth transmission lines are used, all eLink transmitters and receivers are equipped with programmable pre-emphasis and equalization circuits respectively.

For experimental control, the device features three I2C interface controllers and a General Purpose Input/Output 16-bit port as well as a master reset output. For environment monitoring, the device implements eight analogue inputs that can be read by a 10-bit ADC through a multiplexer. By combining two of the analogue inputs differential operation is also possible. Additionally, the analogue inputs can act as current sources at the same time as they are read by the ADC allowing, for example, to measure the voltage across a PT100 device used for temperature monitoring. Moreover, the lpGBT allows monitoring of its internal supply voltages and temperature. A programmable voltage output with 8-bit resolution and a 1 V reference voltage are also made available.

The lpGBT was fabricated in a 65 nm CMOS technology and uses radiation-hardening techniques for radiation tolerance to both TID effects and Single Event Upsets. The paper discusses in detail the lpGBT architecture and functionality. Extensive experimental results will be presented at the workshop.

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Presenter: MOREIRA, Paulo (CERN)

Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **92**　　　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

LpGBT Tester: an FPGA based test system for the lpGBT ASIC

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The lpGBT transceiver is a radiation tolerant ASIC designed to be used in High Energy Physics detector systems. It aggregates data from up to 28 eLinks to one high-speed link running at 5.12 or 10.24Gbps. In the downlink direction, it can be used for timing and trigger distribution by demultiplexing the incoming downlink bitstream running at 2.56Gbps onto up to 16 eLinks. Moreover, the lpGBT provides additional interfaces to handle the detector slow control. This paper presents the lpGBT tester, based on a Xilinx development kit and a custom FMC card developed to perform the pre-production test.

Summary

Following the lpGBT design, started in 2015, the first batch of LpGBT was produced and delivered at CERN by the end of 2018. The specification defines the transceiver chip interfaces: bi-directional high-speed links to be connected via optical fibre to the back-end electronics, up to 28 electrical links (eLinks) to receive detector data and 16 eLinks to transmit trigger and configuration information to the front-end modules. Elinks are grouped in groups and can be configured with different data rates: 80, 160, 320Mbps for the downlink and 160, 320, 640, 1280Mbps for the uplink. Additionally, the lpGBT delivers 32 clocks with configurable frequency of 40, 80, 160, 320, 640 or 1280MHz. Besides eLinks, the LpGBT offers several slow control features: ADCs, voltage DAC, current DAC, temperature sensor, I2C masters, and GPIOs.

The lpGBT tester is based on the VC707 evaluation platform from Xilinx and a custom dual-port FMC card featuring an lpGBT dedicated socket. A complete and flexible Python framework was developed to streamline the process of testing various functionalities of the chip. The software communicates with the FPGA through an Ethernet interface using the IPBus protocol. The lpGBT-FPGA IP core is instantiated in the firmware to handle the high-speed link. Numerous multimode eLink serializer and deserializer, emulating detector component, were developed to perform complete Bit Error Rate test. The test system offers a set of functionalities to check the slow control features using internal logic or communication with external analog devices.

The development process is based on the Gitlab's continuous integration and issue reporting features to ensure the working state of the main project and split de workload among the developers. Therefore, every time a new feature is implemented and pushed to the remote repository, the software and firmware are compiled and tested on a target platform before being merged to the master development branch.

This paper presents the tester's hardware, firmware and software modules as well as the development workflow used to improve the development reliability.

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **93**　　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Design of Finite State Machines for SRAM-based FPGAs operated in radiation field

Tuesday, September 3, 2019 5:20 PM (20 minutes)

For the CERN LHC Run 3, the ALICE experiment completely redesigned the Inner Tracking System, which now consists of seven cylindrical layers instrumented with 24120 Monolithic Active Pixel Sensors, covering an area of $10 m^2$.

The ITS is controlled and read out by 192 custom Readout Units, which employ commercial SRAM-based FPGAs and will operate in an ionising radiation field, requiring specific FPGA design to ensure system reliability.

This contribution focuses on the techniques developed for designing radiation tolerant finite state machines, discussing the theoretical background, the actual implementation, and their validation with fault injections and proton irradiation tests.

Summary

The new ALICE Inner Tracking System (ITS) employs 24120 ALPIDE sensors throughout all its layers, with more than 12 billion pixels in total. The readout system, composed of 192 identical Readout Units (RUs), has complete control over all sensor operations, including power management and data readout.

Its reliability is, therefore, critical for the correct operation of the entire ITS.

The sensors directly drive the differential high-speed links connecting these to the readout, making it mandatory to place the readout system as close as possible to the detector to achieve the reliable transmission at the required bitrate.

The RUs will be placed at about five meters from the interaction point along the beam axis, and at a radial distance of about one meter.

The expected TID for the entire detector life cycle is about 10 krad (safety factor of 10), which does not raise concerns since all the system components have been validated.

Conversely, the expected flux of particles with sufficient energy (>20 MeV) to induce Single-Event Effects (SEEs) in modern microelectronic devices is of the order of $10^3 \ s^{-1} cm^{-2}$, posing a challenge to the utilisation of commercial, SRAM-based FPGAs.

The options of designing a specific ASIC or employing rad-hard-by-design FPGAs have both been evaluated, but the lack of flexibility of the first and the big cost/performance penalty of the latter ruled these out.

Irradiation tests showed that, with the specific device employed, a Xilinx Kintex UltraScale XCKU060 FPGA, the whole system of 192 RUs will experience, on average, an SEE affecting the FPGA every 8 s (worst-case scenario).

An external scrubbing sub-system, driven by a flash-based FPGA, ensures the long-term stability of the FPGA design.

However, the SRAM-based FPGA design needs to deal with errors until the scrubbing cycle corrects them.

All Finite State Machines (FSMs) must keep their correct state even in case of errors, since the scrubbing can only restore the static configuration and not the logic state.

In digital design, FSMs are implemented with sequential logic, storing the present state, and combinatorial networks, by implementing state transition and output functions.

This contribution investigates the interplay between the combinatorial and sequential blocks, how errors happening in one, or both, propagate through successive state changes, and how they affect

the final FSM behaviour.

The problem is approached, first from a theoretical point of view, providing exact solutions for the expected failure rate of an unprotected FSM and for different protection schemes.

An analytical model describes the system behaviour in such cases.

Subsequently, the best protection topologies were implemented into the real design and extensively tested by means of controlled error injections and a proton irradiation test.

The comparison of the analytical model with the test results on dedicated designs will be discussed.

Finally, this contribution will also illustrate how the selected protection schemes have been implemented in the FPGA design.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **94**　　　　　　　　　　　　　　　　　　　　　　　　　Type: **Oral**

Effects Of Gamma Irradiation On Leakage Current In CMOS Readout Chips For Atlas Upgrades Silicon Strip Tracker

Tuesday, September 3, 2019 2:00 PM (25 minutes)

As part of ATLAS Phase-II upgrade project for the High-Luminosity Large Hadron Collider (HL-LHC), an irradiation experiment using a 60Co source was carried out at Brookhaven National Lab to characterize the leakage current from the 130 nm CMOS technology ABCStar chip as a function of the total ionizing dose (TID). The ABCStar chips were held at -10o and 0o C and received dose rates ranging from 0.6 to 2.5 Krad/h. The outcome of the ABCStar irradiation is presented and compared with previous irradiation campaigns utilizing the ABC130 prototype chips, which were irradiated under similar dose rates and temperatures.

Summary

An irradiation experiment using a 60Co source was carried out at Brookhaven National Lab to characterize the leakage current from the ABC star front end readout chip as a function of the total ionizing dose (TID). The chips were at conditions similar to what is expected in the HL-LHC. Three ABCStar chips were held at -10o C and received a dose rate of 2.5 Krad/h, 1.1 Krad/h and 0.6 Krad/h respectively. A fourth ABCStar was held at 0o C and received a dose rate of 0.6 Krad/h. The outcome of the ABCStar irradiation is presented and compared with previous irradiation campaigns utilizing the prototype readout chips, the ABC130, which were irradiated under similar dose rates and temperatures. The results will help provide an understanding of the physical processes behind the TID effects.

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Session Classification: Radiation Tolerant Components and Systems

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **95**　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Readiness of the ATLAS Tile Calorimeter link daughterboard for the High Luminosity LHC era

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Daughterboard (DB) is the readout link and control board that interfaces the front-end and off-detector electronics for the HL-LHC of the the ATLAS Tile Calorimeter. The DB sends high-speed readout of digitized PMT samples, while receiving and distributing configuration, control and LHC timing. A redundant design, Xilinx SEM, TMR, FEC and CRC strategies minimize single failure points while withstanding single-event upsets and damage from minimum ionizing and hadronic radiation. We present the current results of the performed TID, NIEL and SEU tests, aiming to demonstrate the readiness of the Daughterboard to withstand the radiation requirements imposed by the HL-LHC.

Summary

The Phase-II upgrade plans for the ATLAS central hadronic Calorimeter, the Tile Calorimeter, facing the High Luminosity LHC (HL-LHC) era includes approximately 1024 radiation tolerant readout link and control boards (Daughterboards) that will provide full-granularity digital data to a fully-digital trigger system off-detector through multi-Gbps optic fibers. Four commencial SFP+ modules handle 4x9.6 Gbps uplinks driven by two Kintex Ultrascale+ FPGAs and 2�4.8 Gbps downlinks driven by two GBTxs. The Daughterboard design minimizes radiation-induced errors and enhances data reliability by:
- embracing a fully double redundant design,
- using CERN radiation hard GBTx ASICs and Kintex Ultrascale+ FPGAs,
- implementing Triple Mode Redundancy in the FPGA firmware,
- employing the Xilinx Soft Error Mitigation (SEM) to correct for configuration memory SEEs,
- using CRC error verification in the redundant uplinks while FEC is handled by the each GBTx in each downlink.

We have performed TID, NIEL and SEU radiation tests in order assess the radiation tolerance strategies followed in the design and to qualify the Daughterboard for the HL-LHC requirements according to the ATLAS policy on radiation tolerant electronics. Over the HL-LHC lifetime, the Daughterboard positioned on the area most exposed to radiation will have to withstand 23.57 kRad of Total Ionizing Dose, a total Non-Ionizing Energy Loss corresponding to $1.12655 \times E12$ - 1 MeV equivalent neutron fluence, and seamlessly run and recover from any single event upset and single event latch-up for a fluence of $1.35987 \times E11$ protons per cm^2. We present the current results of the radiation tests performed to demonstrate the readiness of the Daughterboard to withstand the radiation requirements imposed by the HL-LHC, and the new strategies derived to mitigate and minimize the undesired SEU effects seen during the tests.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **96**   Type: **Oral**

Development of the Compact Processing Module for the ATLAS Tile Calorimeter Phase-II Upgrad

Thursday, September 5, 2019 2:25 PM (25 minutes)

The LHC Phase II Upgrade of the ATLAS Tile Calorimeter (TileCal) implies a new readout and trigger architecture. The on-detector readout electronics will transmit detector data to 32 Tile PreProcessor (TilePPr) boards in the counting rooms at the LHC frequency, sending selected data to the ATLAS FELIX and interface with the trigger systems. Each TilePPr is composed of four Compact Processing Modules (CPM) with single-width AMC form factor and one full-size ATCA carrier with 4 slots. This contribution presents the design of the CPMs and first experiences, and reviews the results of the TilePPr prototype for the TileCal Demonstrator programme

Summary

The Tile Calorimeter (TileCal) is one of the subdetectors composing the ATLAS detector at the Large Hadron Collider (LHC). The LHC Phase II Upgrade of TileCal includes the complete redesign of the on- and off-detector electronics, and the implementation of a new readout architecture with new interfaces to the upgraded full digital trigger system.

After the Phase II upgrade, the on-detector readout electronics will transmit the detector data to the Tile PreProcessor (TilePPr) boards in the counting rooms for every bunch crossing (every 25 ns), leading into required data bandwidth of ˜40 Tbps to read out the entire detector. The TilePPr board will store the digitized samples in pileline memories until the reception of a trigger acceptance signal when the data will be transmitted to the Front End LInk eXchange (FELIX) system. The data received from the detector is processed in real-time and calibrated energy and time per cell for every bunch crossing are transferred to the first level of trigger through the Trigger and DAQ interface system (TDAQi).

Each TilePPr module will read out and operate eight TileCal modules, requiring a total of 32 TilePPr modules for the complete readout and operation of the detector. Each TilePPr comprises four Compact Processing Modules (CPM) with single-width Advanced Mezzanine Card (AMC) form factor, one full-size Advanced Telecommunications Computing Architecture (ATCA) carrier with 4 slots, and one GbE switch and one ARM-based computer mezzanine cards. The high-speed communication with the on-detector electronics, data acquisition and core processing functionalities relies on the CPMs, while functionalities for power management, control and configuration of the TilePPr boards are implemented in the mezzanine cards.

Each single AMC CPM hosts eight Samtec FireFly modules with MXC connectors; a Xilinx Kintex UltraScale FPGA for data buffering, digital processing and control; a Xilinx Artix 7 FPGA for slow control and monitoring; and high-speed interconnections to communicate with the TDAQi through the Zone 3 connector. The CPMs provides a high-speed path with the on-detector electronics through 32 GigaBit Transceiver (GBT) links running at 4.8 Gbps for the downlink (to the on-detector electronics) and 9.6 Gbps for the uplink (from the on-detector electronics) with fixed and deterministic latency.

The CPM design is based on the TilePPr prototype developed as part of the Demonstrator programme. This board is a double mid-size AMC form factor equipped one Xilinx Virtex 7 FPGA to read out the Demonstrator module and one Kintex 7 FPGA to perform trigger to perform preprocessing tasks. The TilePPr prototype has served to evaluate the new readout architecture with a

fully functional prototype of the upgraded on-detector electronics during six test beam campaigns at the SPS accelerator facilities between 2015 and 2018.

This contribution presents in detail the design and integration plans of the Compact Processing Modules for the ATLAS Tile Calorimeter Phase II Upgrade, as well as, the results and experiences with the designed prototypes for the TileCal Demonstrator programme.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **97**   Type: **Poster**

Upgrade of the ATLAS TileCal High Voltage system

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The High Voltage (HV) system of TileCal, the ATLAS central hadron calorimeter, needs to be upgraded during the so called Phase II Upgrade of the LHC for the HL-LHC. In thw proposed solution, the HV regulation boards are moved away from the detector and deployed in the counting room, safe from radiation damages and with permanent access for maintenance. This option requires a new layout with HV cables about 100 m long, but removes the requirement of radiation hard boards. HV-remote regulation boards have been developed and tested. Preliminary results of the performance will be presented.

Summary

The High Voltage (HV) system of TileCal for the HL-LHC will consist of HV-remote boards, located far from the detector in the ATLAS counting room and connected to the detector by 100 m long cables. Inside the detector passive HV-bus boards there will be used to bring the HV to each photomultiplier tubes (PMTs) located in mini-drawers inside the girders of the modules.

The HV-remote boards are the boards that regulate the HV for each individual PMT. In total, 256 boards are needed for the TileCal operations. Each input HV (of -830 or -950 V) can serve up to 24 PMTs and the voltage of each PMT can be decreased individually in a range of the order of 350V, as in the current TileCal design [1]. The boards are intended to use two primary HV inputs to provide HV for 48 PMTs in the case of the TileCal central barrel modules and 32 PMTs in the case of the two TileCal Extended Barrel. Relative to the current HV system, the main functional improvement is the addition of individual on/off controls for each individual PMT. The operation in the absence of radiation allows the simplification of the regulation loops with the removal of some electronic components. The control and monitoring, that in the current TileCal design is done with HV-micro boards [1] communicating with the ATLAS Detector Control System via CANbus architecture, will be completely redone.

The first prototype generation of the HV-remote boards has been produced to operate 24 PMTs, while he following generation will operate 48 PMTs. The communication and control is done via SPI bus through an ethernet interface. The first prototype boards use Tibbo EM1206 modules as interface, and it is intended that the final version uses a System on Chip solution.

The primary HV is provided by Hamamatsu C12446-12 modules, installed inside boards located in the ATLAS counting room..

HV-remote boards prototypes have been tested in the laboratory and results on stability, sensitivity to temperature, etc, will be presented. Problems identified in the first prototypes during the tests, will result in changes in the design of the following generations that will be discussed.

[1] R. Chadelas et al., "High voltage distributor system for the Tile hadron calorimeter of the ATLAS detector", ATLAS-TILECAL-2000-003, 2000, https://cds.cern.ch/record/436230

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Session Classification: Posters

Track Classification: Power, Grounding and Shielding

Contribution ID: **98**   Type: **Oral**

Depleted monolithic active pixel prototypes for MIP detection and photon counting

Wednesday, September 4, 2019 2:50 PM (25 minutes)

The LF2 is a depleted MAPS prototype chip produced in the LFoundry 150 nm HV-CMOS process on 500 Ωcm and 1900 Ωcm wafers. The chip includes two monolithic matrices. One matrix of 40 rows x 78 columns contains 50 x 50 µm2 pixels each with a charge sensitive amplifier, a shaper, and a discriminator, which are readout by a digital block with FE-I3 column drain architecture. A 26 x 52 photon counter matrix of 75 x 75 µm2 pixels each with a 16-bit counter completes the LF2. Testbench measurements, including charge collection, have been carried out and will be presented.

Summary

The ATLAS and RD50 collaborations have been investigating the use of depleted Monolithic Active Pixel Sensors (DMAPS) for HEP experiments. This technology could offer a cost effective solution for the pixel and strip vertex detectors, where the radiation requirements are not exceedingly high, replacing the traditional hybrid solution. Furthermore, photon counting DMAPS could also be an interesting technology for various imaging applications.

The LF2 is a depleted MAPS prototype chip produced in 2018 in the LFoundry 150 nm HV-CMOS process on 500 Ωcm and 1900 Ωcm wafers by the collaboration of IFAE, University of Liverpool, University of Geneva and KIT with the support of RD50. The ASIC includes two monolithic matrices which are completely independent and only share the substrate: a tracking pixel detector and a photon counting device. Both matrices integrate analog and digital readout electronics. The sensor is implemented by means of a p-substrate/deep n-well junction. The p-substrate is biased at a negative voltage to create a depleted volume. The main components of the analog readout electronics, very similar in both matrices, are a sensor bias circuit based on a high ohmic resistor, a charge sensitive amplifier, a source follower, filter and a CMOS comparator with a local 4-bit DAC to compensate for offset variations. Each pixel also includes an injection circuit to test the readout electronics. With respect to the digital readout electronics, the photon counting array contains a 16-bit counter while in the tracking matrix the circuits follow an FE-I3 readout approach. The analog and digital readout electronics are embedded inside the pixel sensitive area in both matrices.

The readout of the tracking matrix is asynchronous, zero suppressed and triggerless. The matrix is handled by a control unit that reads sequentially the content of each EOC cell at 40MHz. The data are passed to 2 serializers and transmitted off-chip at a speed of up to 320 MHz through LVDS pads. The readout of the photon counting matrix is simple and not conceived for high speed, only to test the monolithic concept. Pixels are read individually. The content of the 16-bits counter of the accessed pixel is loaded in parallel to a 16-bits shift register at the periphery. Then, the data is serialized at a maximum speed of 40MHz.

The LF2 ASICs were received in 2018 and a readout system, based on the Xilinx ZC706 FPGA board, was developed. The initial results of the table-top characterization of the devices will be presented, including charge collection studies with radiation sources and Transient Current Technique measurements.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **100**   Type: **Poster**

Design of a radiation hardened TDC with a resolution of 4 ps and an improved interpolation technique

Thursday, September 5, 2019 4:55 PM (20 minutes)

This paper presents a radiation tolerant single-shot time-to-digital converter (TDC) with a resolution of 4 ps, fabricated in a 65 nm Complementary Metal Oxide Semiconductor (CMOS) technology. To achieve the low resolution, the delay elements are implemented using a new interlocked interpolation technique to reduce the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) error. The delay line is placed inside a Delay Locked Look (DLL) to compensate for Process, Voltage and Temperature (PVT) variations- and variations due to ionizing radiation.

Summary

Time-to-Digital Converters (TDCs) can be compared to Analog-to-Digital Converters (ADCs) as they digitize analog-like time differences instead of analog voltage differences. Several applications require precise time measurements such as particle tracking in high energy physics, where a high resolution TDC is required to distinguish tracks from different vertices. Also inside Time-Of-Flight distance measurements and many other circuits like frequency synthesizers, clock generators, clock data recovery circuits (CDRs), time-domain ADCs and jitter measurement circuits, the on-board TDC is critical to the overall performance of the circuit. High-performance TDCs thus require a small quantization delay, low noise, large sampling speed and high linearity. One of the main challenges for increasing the resolution of the TDC, is overcoming the minimum gate-delay of the technology. The methods which are commonly used to overcome this problem are, the Vernier architecture, (passive or active) interpolation and the parallel TDC. All of these architectures come with their own challenges, but the most suitable architecture for the mentioned applications is the passive interpolation.

In this design the Delay Line (DL) consists of 64 pseudo-differential delay cells which are interpolated four times, this results in a resolution of 4 ps. Increasing the number of interpolation stages will also increase the raw resolution, but the nonlinear behavior of the passive interpolation will cause the DNL and INL error to dominate the effective resolution. Therefore, an interpolation of only four times has been chosen. To further improve the performance of the TDC, a new technique of interlocked interpolation is proposed. Hereby two delay lines are connected through each other by the interpolation resistors. Therefore, interlocking the phase of every second interpolation node. By using this technique, the DNL and INL error decreases significantly. The TDC is designed to be tolerant to ionizing radiation up to 2 MGy. In order to achieve MGy TID tolerance enclosed layout transistors are used. Additionally, the DL is placed in a Delay Locked Loop (DLL) to ensure that the TDC is robust against Process, Voltage and Temperature (PVT) variations, and to ionizing radiation.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **101**   Type: **Poster**

Measurement results for AARDVARC: Waveform Sampling System On Chip with Picosecond Timing Resolution

Thursday, September 5, 2019 4:55 PM (20 minutes)

In this article we describe the measurement results on an "AARDVARC" prototype in 130 nm. AARDVARC is a multi-channel waveform digitizing and processing Application Specific Integrated Circuit (ASIC) front-end. We report on various performance metrics: fast sampling (10-14 Gsa/s), deep storage (32K samples), timing resolution (better than 5ps), low power consumption (<100mW/channel).

Summary

State of the art large collider experiments pose conflicting requirements to the data acquisition electronics: extreme integration and density, extremely good timing accuracy, low power, high data transfer rates, large radiation awareness. The sheer number of channels also calls for reduced per-channel cost. In order to achieve accuracy goals, fast waveform sampling and digitization are often preferred to allow for tracking of radiation degradation of the light detectors, pile up events and ultra precision timing resolution.

Through higher integration with analog signal conditioning, waveform sampling, digital readout and signal processing with extended digital functions on chip, the AARDVARC allows for flexible digital signal processing within the front-end which reduces the amount of data needed to be transferred to the backend. The device performs continuous sampling and deep analog storage and on-demand or self-triggered digitization of analog storage, packetization and digital transmission (with parallel or serial interfaces). The AARDVARC ASIC has been fabricated in 130nm process (in Feb 2019). In this paper we cover various measurement results from the testing campaign.

Voltage Noise/RMS: due to the distributed nature of the ADC conversion, the individual samples are subject to large recording offsets ("pedestals"), that need to be measured, recorded and corrected. The remaining errors in voltage conversion after this correction are due to noise during conversions, and have been measured for each storage sample position. The typical errors are normally distributed with a standard deviation of approximately 0.7 mV.

Sampling Speed: AARDVARC uses an internal Delay Locked Loop (DLL) to adjust and control a variable delay line - by controlling the frequency of an input clock it is therefore possible to automatically adjust the sampling frequency. The sampling speed of the AARDVARC was measured by feeding a fast periodic input (approximately 1GHz). The results for a sampling frequency of 13 GSa/s will be presented.. Effect of sampling rate on various ASIC parameters has been studied.

Accuracy/Sample jitter: To better study the achievable accuracy, the individual sample stability was investigated by feeding a signal whose phase relationship with the sampling clock was known and with jitter better than 100 fs. By varying the phase and repeating the measurement, jitter as a function of sampling array position was investigated, as it was expected that it would increase with integrated delay across the delay chain. The delay distribution for an individual sample position will be presented. Both measurements are performed at a sampling rate of 13 GSa/s. At this sampling rate, the figure shows that individual samples have a stable timing with a standard deviation of less than 2.5ps across the entire sampling space. Other experiments show that the accuracy is higher for higher sampling frequency - this is understood, and due to the specifics of

the delay line. Methods to better control jitter at lower sampling rates are now being studied and will be implemented in the next revision of the AARDVARC.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **102**   Type: **Poster**

FAST: a front-end readout ASIC for a 30 ps time resolution with 6 pF UFSD sensors

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The UFSD group of Turin is working at the development of custom front-end electronics for the read-out of thin silicon sensors with moderate internal gain, aiming at high-precision time tagging applications. The development of specific ASIC for timing at INFN-Torino started in 2016. The first two ASIC prototypes, TOFFEE and ABACUS, have been successfully tested in our laboratories and at particle accelerator facilities. Leveraging on the know-how obtained in those two projects, a new low power front-end chip, named FAST, has been designed to reach the intrinsic 30 ps UFSD time resolution with a 6 pF sensor capacitance coupling.

Summary

The activities of the Turin Ultra Fast Silicon Detector (UFSD) group, are centered on the design and characterization of silicon sensors and the development of front-end electronics dedicated to UFSD sensor readout. The activity of the group is mainly focused on meeting the requirements of the next generation of HEP colliders: much higher luminosity will require systems able to include very strict requirements in terms of timing capabilities. The main role in this field is played by the High-Luminosity upgrade of the LHC (HL-LHC), where the new requirements include a pile-up factor of 150-200 events per bunch crossing. In this context, time tagging is one of the fundamental tools which can be exploited to distinguish events overlapping in space but separated in time by a few tens of pico-seconds: both ATLAS, with the High Granularity Timing Detector (HGTD) and CMS, with the MIP Timing Detectors (MTD), are pursuing time tagging projects with a 30 ps time resolution.

The measurement of the Time of Arrival of a particle is affected by uncertainties coming both from the sensor used to detect particles and from the readout electronics used to measure the weak signals generated by the sensor. In order to increase the time resolution, signals with high amplitudes and small rising time are key points. This requirement leads to the optimization of both silicon sensor and readout electronics. In this context, UFSD sensors are proposed as a good candidate for time measurements, due to their capability to generate signals with the properties listed above. For what concerns the contribution of the readout electronics, the slew rate and the front-end noise are mainly influencing the timing performances. In this paper, we present FAST, a 20 channels novel low power front-end electronics devoted to timing resolution with a front-end jitter lower than the intrinsic 30 ps limit of a typical 55 micron thick UFSD sensor. The design has been optimized for a 2 mW/ch power consumption and a sensor capacitance of 6 pF. Extensive simulation took into account the charge probability distribution, the sensor time resolution and the radiation damage effect at the expected fluencies for the CMS MTD upgrade. In order to map different solutions, we designed three flavors of FAST that differ in the amplification stages: all based on a resistive feedback TIA architecture, they presents different bandwidth and signal shaping approach, due to both topology and device choices.

The FAST performances are promising even for other research branches of applied physics, like particle therapy. In this field, having fast sensors with high spatial and time resolution is crucial to fulfill the requirement of future particle beam counters. An additional requirement for these clinical applications is the capability of being able to work with an input signal rate in the order

of hundreds of MHz. According to accurate simulation, the novel ASIC FAST is able to meet the HEP timing requests as well the high rate single ion detection, useful for clinical applications with accelerated ions.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **104**   Type: **Poster**

Study of a triggered, full event zero-suppressed front-end readout chain operating up to 1 MHz trigger rate and 300 pile-up for CMS Outer Tracker upgrade at HL-LHC

Thursday, September 5, 2019 4:55 PM (20 minutes)

The CMS Outer Tracker at HL-LHC will have to cope with 300 pile-up events per bunch crossing and to improved tracking performance while operating at a trigger rate up to 1 MHz. The front-end electronics readout chain consists of sensor readout ASICs connected to a data concentrator ASIC featuring zero-suppression. This contribution presents the methodology and the analysis work for the sizing of a multichip FIFO-based architecture and implementation of a full exception handling mechanism featuring a robust data readout synchronization and event loss probability lower than 0.1% at the highest pile-up condition with a power density lower than $100 \ \mathrm{mW/cm^2}$.

Summary

The front-end electronics of the CMS Outer Tracker detector presents very challenging requirements to operate in the future HL-LHC. An efficient event selection at a particle rate up to 300 pile-up requires an increase in the trigger rate and latency with respect to the existing system. Level-1 trigger requires with a fixed latency of 12.8 us the full event to be read out at an average rate of 1 MHz.

The readout of the raw full event produces a data rate of 32 Gbps that does not fit the limited output bandwidth per module of 640 Mbps. Therefore, upon the reception of a trigger, 32 sensor readout ASICs provide the zero-suppressed full event to 2 data concentrator ASICs. Zero suppression and data compression functions generate variable size event data packets while the finite datalink bandwidth and the random nature of trigger arrival times make necessary a temporary on-chip data storage. For this reason, a FIFO-based architecture has been studied and implemented.

FIFO storage elements are based on latches to reduce the overall power consumption. To accurately size FIFOs, a multichip simulation based on physics Monte Carlo samples has been performed. Although a low event loss probability is acceptable, overflow condition in a FIFO must not affect the synchronization between ASICs and with the experiment back end. Therefore, the architecture implements exception handling with error generation at different levels of the readout chain guaranteeing a robust synchronization.

This contribution will present the methodology, the analysis work and the results for sizing the data FIFOs and the implementation of FIFO overflow handling techniques using physics Monte Carlo generated events for different detector occupancy values. Simulation results provide an event loss probability lower than 0.1 % at an average rate of 1 MHz and in 300 pile-up condition with a total power density lower than 100 mW/cm2 for the readout ASICs and data concentrator ASICs.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **105**   Type: **Oral**

A Muon Telescope as Demonstrator of the JUNO Top Tracker Detector

Tuesday, September 3, 2019 9:50 AM (25 minutes)

A four-layer muon telescope has been built employing the equipment and electronics developed for the Top Tracker (TT) detector of the Jiangmen Underground Neutrino Observatory (JUNO). It will serve as a demonstrator of the hardware capabilities in terms of detection efficiency, processing power and system reliability. The entire read out, trigger and acquisition systems have been conceived and build around versatile modular electronics embedding the latest generation of system on chips. A detailed description of the telescope will be given along with the status of the TT electronics and their validation tests.

Summary

Studying neutrino interactions with the JUNO experiment requires dealing with important background signals caused by atmospheric muons traversing the main detector. To reduce the atmospheric muon rate, the experiment will be located underground, but the surrounding rock thickness is not sufficient to shield the detector. To account for the remaining atmospheric muon background, JUNO will be equipped with an external veto system called Top Tracker (TT), made of crossing planes of plastic scintillator strips, which have a high muon detection efficiency to identify and reconstruct these muon tracks. As a small demonstrator of the TT, a muon telescope has been built at the Institut Pluridisciplinaire Hubert CURIEN (IPHC). The detection system of this muon telescope is composed of the same elementary blocks as the TT but arranged in a different configuration. Four tiles of two-layer scintillator strips crossed in a XY lattice are used for precise muon tracking. A 64-anode Photomultiplier Tube (PMT H8804) collects the light of each strip layer and feeds directly the Front-End Board electronics (FEB). The heart of the FEB is a multipurpose ASIC called MAROC3 developed by Omega Microelectronics. It is a 64-channel preamplifier followed by a fast shaper and a discriminator, allowing for fast triggering in parallel with a slow shaper plus two "track and hold" for providing a multiplexed analog charge. A digital version of the latter is also available thanks to an internal Wilkinson ADC (8/10/12 bit). All the infrastructure needed by the PMT and MAROC3 is provided by a Read Out Board (ROB) that configures, controls and reads out the ASIC. The full telescope system is equipped with 8 FEB and ROB cards. A third board called Concentrator (CB) aggregates all the data coming from each ROB and sends them to the DAQ through a GbE optical link. CB provides a timestamp for ROB data with the nanosecond resolution before applying a first level (L1) trigger functionality. A simple coincidence algorithm has been implemented in order to reject the events that do not appear in the same time window in both the X and Y planes of the same detector layer. Finally, CB sends valid events to the DAQ. CB has been implemented as a motherboard that accommodates a daughter card hosting the processing unit. All the connectivity with the ROBs, DAQ, the slow control system, as well as the L2 trigger electronics (present only in JUNO) is provided by the motherboard while the daughter is an embedded high-performance system on module. It hosts a Xilinx system-on-chip of the latest generation (Zynq Ultrascale+) along with a 16Gb DDR4 RAM. Equipping this muon telescope with the readout and trigger electronics that will be deployed in the TT detector allows us to validate the whole readout chain of the future JUNO external veto system.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **106**   Type: **Oral**

Versatile Link+ Transceiver Production Readiness

Tuesday, September 3, 2019 4:30 PM (20 minutes)

The Versatile Link+ project is about to enter its production phase, ready for the Phase 2 HL-LHC detector upgrades. We present the status of the front-end part of the Versatile Link+ project: the Versatile Link+ Transceiver (VTRx+), which provides a low-mass, radiation tolerant, optical transmit- and receive module for tight integration in the upgrading HL-LHC detectors. We describe the development and thorough testing carried out with the transceiver prototypes and their sub-components and the design decisions that have led to the final production-ready prototype. The planned production timeline, aligned with the assembly timescales of the HL-LHC experiments, is also presented.

Summary

During the phase 2 upgrades of the ATLAS and CMS experiments at the Large Hadron Collider (LHC) several detectors will be replaced to improve their physics performance. In particular, these upgrades aim to replace the innermost detectors that are exposed to the harshest radiation environments. To cope with the increasing data volume and the higher trigger rate, high-speed optical links will be deployed in large quantities as part of the upgrade programme. The tight space constraints and the high channel count of the on-detector electronics will require to develop a low-profile (20mm x 10mm x 2.5mm), multi-channel front-end component. During their expected lifetime these components will have to withstand high radiation levels (1MGy total dose, 1×10^{15} n/cm2 and 1×10^{15} hadrons/cm2 total fluence) and they have to operate over a wide temperature range (-35 ℃ to +60 ℃).

The Versatile Link+ (VL+) project has developed a custom front-end module that fulfils these requirements. The front-end module (VTRx+) will be based on radiation-tolerant Laser Diode Driver (LDD) and TransImpedance Amplifier (TIA) ASICs, and commercial VCSEL and PIN photodiode (PD) components. Components have been evaluated and shown to meet the required performance targets during both functional and environmental testing. We will show an overview of the performance of VCSELs and PDs operating over the full required temperature range. Radiation testing has also been carried out for candidate VCSELs and PDs and the results will be shown, along with the impact of the observed degradation on system performance and margins. The design decisions that aim to guarantee the best performance in the special environment of the final applications are explained.

Several VTRx+ prototype generations have been developed and tested in order to optimize the design. The final VTRx+ utilizes a thin optical coupling lens that covers the qualified optical components and the latest versions of the radiation-hard ASICs. Electrical connectivity is accomplished using a low-profile 40-pin connector and optical connection is provided by a fibre pigtail with a MT connector interface. The test results of the final prototypes will be presented.

Finally, we will present the planned production timeline, which starts with a pre-series production at the end of 2019 followed by a thorough pre-series qualification programme. The launch of the series production is planned for mid-2020. The series production is foreseen to last for around two years providing VTRx+ transceiver modules in time for the planned experiment upgrades.

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Session Classification: Optoelectronics and Links

Track Classification: Optoelectronics and Links

Contribution ID: **107**   Type: **Poster**

A Monolithic Active Pixel Sensor for CEPC vertex detector

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The proposed CEPC presents new challenges for the pixel detector in terms of cell size and functionality. A high data rate digital design and readout architecture of a MAPS prototype for the CEPC vertex detector is presented. The column drain based readout architecture, benefiting from the ALPIDE and FE-I3 approach, has been implemented to achieve high spatial resolution, fast readout, and low power consumption. The simulation results indicate the readout logic works properly with the high input data rate of 120MHz; both analogue front end and in-pixel readout logic meet the 25ns bunch spacing.

Summary

The Circular Electron-Positron Collider (CEPC) is proposed for high-precision measurements of the Higgs boson. It will include a vertex detector designed to provide an excellent impact parameter resolution. Monolithic Active Pixel Sensors (MAPS) are being investigated for the CEPC vertex detector due to its high granularity, high speed, low material budget, low power consumption and radiation tolerance. According to the preliminary estimation, radiation hardness requirements will be of ˜1MRad/year and 2×10^{12} 1MeVneq/cm2/year for Total Ionizing Dose (TID) and Non-Ionizing Energy Loss (NIEL) respectively. The previous MOST1 project resulted in the first prototype of 25×25μm2 pixels was produced with a 0.18um CIS process from TowerJazz. However, the analogue peaking time (1μs) and integration readout time (100μs) of the MOST1 did not meet the requirement. In order to overcome those limitations, the MOST2 was launched in 2018. The first prototype with a pixel matrix of 192×64 has been submitted to fabrication in June 2019 and it is presented in this paper.

This new prototype includes several enhancements. The analogue front end has been optimized for fast rising time (<25ns) and two new fast in-pixel readout logics have been designed: an FE-I3 like scheme and ALPIDE scheme. In the first readout logic, the electronics are very similar to those of the FEI3 but due to area limitations, the address ROM has been replaced by a simplified address generator array and the timestamp is not stored in-pixel but at the End Of Column (EOC). In the ALPIDE pixel, the electronics are the same but the hit storage registers have been replaced by an edge-triggered flip-flop in order to reduce the global control signal for less area occupancy and the priority Address Encoder and Reset Decoder (AERD) block has been modified to boost its speed to 40MHz. The pixel matrix is subdivided into two matrices of 96×64 pixels, each one with a type of pixel flavor so that their performances and challenges can be addressed in direct comparison. Both schemes employ the same double column drain architecture. The pixel readout is arbitrated by a token propagation, with the topmost pixel having the highest readout priority. At the EOC, the circuitry has a counter running at 40MHz to generate the timestamp with 25ns steps; the data will match the timestamp and be stored temporally for each double column in the first level FIFO, then the data will be suppressed to eliminate mismatched timestamps with the trigger mode and transmitter to a serializer buffered by the second level FIFO. Triggerless mode is also supported to preserve all the readout data before buffering to the output. In order to implement a high-speed serialization transmission, the clocks are managed by a Phase Lock Loop (PLL) which offers up to 4Gbps data rate capability.

In this work, the prototype mentioned above will be described and the preliminary simulation results will be presented.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **108**   Type: **Poster**

SRS VMM and SRS Timepix3 as platforms for particle detectors

Within the last years, the VMM and Timepix3 ASICs were implemented into the general purpose Scalable Readout System (SRS). Both flavours of the SRS will be presented. They are continuously improved and extended to increase their field of application.

Already with prototypes of these systems, detectors for different applications were read out during test beams of R&D towards the employment in experiments as NMX at the ESS, MAGIX in Mainz, GBAR at CERN or Beam Gas Vertex (BGV) monitors for the HL-LHC. The adaptation of the SRS to some projects will be outlined together with a glance at the experiments.

Summary

The Scalable Readout System (SRS) of the RD51 collaboration, introduced 2009 with the APV25 front-end ASIC, is a general purpose data acquisition system. It includes the full readout chain from the front-end chip and FPGA-based data concentration to data acquisition software. Due to its architecture, SRS is scalable from small laboratory systems to the size of a large experiment.

Within the BrightnESS project and supported by AIDA2020 and the Detector Group of the European Spallation Source (ESS), the recently completed VMM ASIC was implemented into SRS by the Gaseous Detector Development (GDD) group at CERN.

At the same time, the Timepix3 chip was implemented in the SRS at Bonn University supported by AIDA2020.

Both flavours of SRS are targeted towards different applications due to the complementary of the front-end ASICs.

While the Timepix3 project in Bonn is focused to R&D for BabyIAXO and a Pixel-TPC for the ILC, the VMM implementation was primarily targeted to the NMX instrument at ESS. However, due to the general design of SRS, both system can be adapted to different applications and have raised interest by many groups mainly from the gaseous detector community.

Examples are the MAGIX experiments planned at a new accelerator at Mainz University, the GBAR experiment at CERN or Beam Gas Vertex (BGV) monitors for the HL-LHC. Common test beams with groups coordinating the R&D for those projects have been carried at at CERN's SPS or the MAMI accelerator. The results are entering the technical design reports or grant applications with SRS as the baseline solution.

The presentation will introduce the concept of the SRS, with a focus on the latest implementation of the Timepix3 and VMM ASICs and ongoing improvements of the systems. Some of the upcoming experiments and R&D projects will be outlined together with required adaptations of the SRS in the future.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 109   **Type: Oral**

Results of the Powerboard for ATLAS ITk Strip Barrel Modules

Thursday, September 5, 2019 2:00 PM (25 minutes)

The Inner Tracker silicon strip detector (ITk Strips) a part of the ATLAS upgrade for the HL-LHC. It employs a parallel powering scheme for the bias high voltage and the low voltage power. To reduce the amount of services, on-module DCDC conversion and high voltage switching is required. These features are implemented on the Powerboard using a step-down buck converter (bPOL12V) to drop the low voltage, a GaN FET for the HV switch and a custom ASIC (AMAC) for control and monitoring. This contribution will present the design, initial test results and plans for the production of O(10,000) Powerboards.

Summary

The ATLAS upgrade for the HL-LHC contains a new silicon tracker called the Inner Tracker (ITk). The ITk Strip detector is a subset of the ITk with striped silicon sensors. It will employ a powering scheme where a single power supply provides power to several modules in parallel. This includes both the high voltage to bias the sensor and the low voltage to power the on-module electronics. The low voltage is supplied to the supporting stave structure using an external 10-11V. The power of a single module will be managed using a custom electronics board called the Powerboard. The Powerboard has four main functionalities; employ a rad-hard switching DCDC regulator (bPOL12V) to step the low voltage from 11V down to 1.5V for local power, monitor the low and high voltage currents directly on a module, disable power in case of module failure and monitor the local temperature. The last three tasks are accomplished using a custom ASIC called the Autonomous Monitor And Control (AMAC) chip. The AMAC is powered using a rad-hard linear regulator (linPOL12V).

The pre-production version of the Powerboard aimed at barrel modules has been designed. Prototypes were used to demonstrate that the design meets the desired specifications.

All functionality was tested with the Powerboard being irradiated using x-rays past 66 Mrad, corresponding to the expected lifetime dose (plus safety margin). The bPOL12V ASIC provided a stable 1.5V output voltage at 2 Amps current load above the desired 70% efficiency. This meets the requirements from the expected maximum life-time load from the front-end chips. The high voltage switch remained closed throughout the irradiation with 500V applied. The monitoring functionality provided correct measurements, with the help of in-situ calibration procedures. The only unexplained result was the steady rise of the linPOL12V output voltage.

The Powerboard has also been operated as a part of complete ITk Strip modules. The only issue observed was an increase in noise hits on strips localized underneath bPOL12V circuit. Even in spite of a 100 μm thick metal shield box surrounding the air-core solenoid coil used as the main inductor. Its impact has been reduced through layout optimizations guided by multiple measurements.

To meet the construction schedule, the scaling up of the production to ˜10,000 Powerboards required for the barre of the ITk Strip upgrade has begun. To maintain high reliability, a stringent quality assurance (QA) and control (QC) plan has been developed. The QA involves a comprehensive stress testing of a random sampling from each batch. The QC will be done on every board at an industrial partner responsible for both the assembly and final testing. After standard manufacturing controls, a full electrical test and burn-in is performed. A custom system consisting of a passive carrier board containing multiple Powerboards that can be connected to an active board

for testing. The active board contains the necessary circuits to test AMAC communication, monitor low and high voltage power outputs, measure the bPOL12V efficiency at varying loads and detect any EMI outside of the shield box.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **110**   Type: **Poster**

First 10Gb/s Transmission with radiation-hardened Silicon Photonic Mach-Zehnder Modulators in a Full Transmission System

Thursday, September 5, 2019 4:55 PM (20 minutes)

In this work, we present a customized pn depletion type Mach-Zehnder modulator (MZM) as well as a fully integrated wavelength division multiplexing (WDM) transmitter design with the merits of high bandwidth and radiation hardness, aiming to upgrade the optical data transmission of future detector systems. A detailed characterization of the modulators on modulation efficiency and RF response was carried out. Based on this work, the first optical link with a data rate of 11.3 Gb/s was set up transmitting $6x10^{12}$ bits error free.

Summary

The number of detector read-out channels as well as the data rate of each individual channel are rapidly increasing in detector instrumentation. Optical links exploited in current large-scale detector systems use directly modulated laser diode based transmitter units. In this scheme, each transmitter is connected by an individual optical fiber with an off-detector receiver. The most viable way to cope with ever increasing data throughput is adding more and more fibers at the price of increased mass and space requirements. In contrast we propose an integrated WDM transmission system with which the data transmission bandwidth of each fiber can be greatly enhanced. The system also addresses the problem of limited radiation hardness of the laser diodes as they will be placed outside of the radiation area.

According to the radiation hardness study of CERN [1], we fabricated radiation-hardened MZMs with customized etch depth and doping concentration. From steady state measurements, we found the driving voltage on one 3 mm long arm to get a phase shift of π is about 15.3 V, resulting in the figure of merit $V_\pi * L$ = 4.6 Vcm. This is a significant improvement compared to our previous device. Also, we fabricated another set of modulators with different lengths and etch depth for comparison on the same chip. Extensive characterizations are in progress and a detailed comparison will be presented.

Considering the DC measurement results, RF measurements were carried out by applying a reverse bias voltage of 2.5 V and an RF amplitude of 2 V_{pp} to the two phase shifters. The modulated optical signal was measured with an electrical spectrum analyzer via a fast photodiode. From the measurements we derived a nearly linear decrease of the signal with frequency at a rate of 1.1 dB per GHz.

Furthermore a complete transmission experiment was set up based on an FPGA as high-speed data source, a two-stage amplifier to drive the modulator with an amplitude of up to 7 V_{pp}, the modulator, an optical amplifier and a commercial SFP+ receiver. The receiver output was connected to the FPGA for bit error rate measurements. We conducted successfully error free transmissions of $6x10^{12}$ bits at a rate of 11.3 Gb/s with a driving amplitude down to 3.1 V_{pp}. A thorough characterization to sound the limits of error free transmission and transmission with acceptable error rates for different scenarios is ongoing and will be presented.

[1] M. Zeiler, S. Seif El Nasr-Storey, S. Detraz, A. Kraxner, L. Olantera, C. Scarcella, Ch. Sigaud, C. Soos, J. Troska, F. Vasey, "Radiation Damage in Silicon PhotonicMach–Zehnder Modulators and Photodiodes", IEEE Trans. on Nuclear Science, vol. 64, no. 11, Nov. 2017, pp. 2794

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Session Classification: Posters

Track Classification: Optoelectronics and Links

Contribution ID: **111**   Type: **Oral**

The Digitizer ReAdout Controller (DIRAC) of the Mu2e electromagnetic calorimeter at Fermilab

Tuesday, September 3, 2019 9:00 AM (25 minutes)

We report on the design and performance of the Digitizer ReAdout Controller (DIRAC) of the Mu2e electromagnetic calorimeter, which consists of a 670 CsI crystals matrix readout by SiPM. The 20-channels DIRAC performs 200 MHz sampling of the SiPM signals transmitted by the front-end electronics. Operation in the Mu2e hostile environment expected Total Ionizing Dose (TID) of 12 Krad and neutron fluenceof 5x1010 n/cm2 @ 1 MeVeq (Si)/y, 1T magnetic field, level of vacuum of 10-4 Torr has made the DIRAC design challenging. We describe design, specifications, architecture and results of the performance tests performed on the DIRAC prototypes.

Summary

The goal of Mu2e experiment is to measure the ratio of the rate of the neutrino-less muon-to-electron coherent conversion in the field of a nucleus, relative to the rate of ordinary muon capture. The observation of this process would be the first evidence of Charged Lepton Flavor Violation and would provide unambiguous evidence for the existence of physics beyond the Standard Model.
The Mu2e detector system consists of a low-mass straw tube tracker to measure particle momentum and an electromagnetic calorimeter made of pure CsI crystals to measure particle energy. The calorimeter is made of two disks each composed of 674 un-doped CsI crystals. Each crystal is read out by two large area MPCC. The calorimeter has three main tasks: provide an additional rejection factor of 200 on cosmic muons, a tracker-independent trigger and improve pattern recognition quality and efficiency for the electron tracks.
Monte Carlo simulation has shown that the calorimeter fulfills all these requirements if it reconstructs the conversion electron energy with a resolution of O(5%) and determines its time of arrival with a resolution better than 500 ps @ 100 MeV. This implies that the front-end signals should be sampled with 12-bit resolution and a sampling frequency of 200 MHz.
The Mu2e calorimeter is a high-granularity crystal calorimeter consisting of 1348 un-doped CsI crystals, arranged in two disks and located inside the detector cryostat. In order to limit the number of pass-through connectors and the length of the cables, the calorimeter readout and digitization electronics will be located inside the cryostat. This choice has made the DIRAC design challenging due to the hostile environment: neutron fluence 5x1010 n/cm2 @ 1 MeVeq (Si)/y, TID 12 Krad, 1T magnetic field, which have required an extended campaign of tests to qualify the employed electronic components, and a level of vacuum of 10-4 Torr, which has required the design of a dedicated cooling system for power dissipation. Given the expected challenging DIRAC performance in terms of sampling frequency and amount of processed data with no equivalent in literature, we have to setup numerous tests campaigns, described elsewhere, in several laboratories to fully qualify the complete set of employed components.
The DIRAC core is a Microsemi® FPGA, that handles the entire ADCs protocol and timing, sparsifies and compresses the digitized data and forms a data packet that is sent to the card or to the DAQ servers through optical fibers. We have chosen the TI ADS4229 ADC and the optical transceiver VTRX developed at CERN. The readout of the entire Mu2e calorimeter requires a complex system of 140 DIRAC cards, for a total of 2800 digitization channels. The DIRACs will be located in custom designed crates, which implement a dedicated cooling system and positioned on the external

lateral surface of the calorimeter disks.

The DIRAC prototypes have been designed, built and tested. We have performed a full vertical-slice test with cosmic rays over a matrix of 20 CsI crystals readout with the full SiPM and front-end electronics. System performance will be reported.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **112**   Type: **Oral**

63U ATCA rack thermal performance and its integration in the undergound areas

Thursday, September 5, 2019 2:25 PM (25 minutes)

As for the High Luminosity LHC the instantaneous luminosity will be increased by a factor 3, an efficient trigger selection will be crucial. To reduce signal latency, the proximity of the readout electronics to the detector becomes very important. A custom designed 63U rack has been chosen as a house for the ATCA based systems allowing installing 50% more shelves in the detector proximity. The higher power dissipation requires an assessment of the impact on the existing underground infrastructures and cooling capabilities verification in a test setup, which also became the cooling facility to qualify the detector boards prototypes.

Summary

In November 2014, the ATLAS technical coordination launched a project dedicated to the study of the ATCA (Advanced Telecommunications Computing Architecture) integration in the existing LHC rack infrastructure. At the beginning, the project focused on the standard 52U 19"rack equipped with two ATCA shelves cooling capabilities assessment. But over the years, the goals of the test campaign were changing to adjust to the current needs of the detectors groups and to face encountered problems and restrictions such as high noise generated by the shelves and limited cooling water flow in the counting rooms. At a certain stage of the project, it was clear that there will be a need for additional space for shelves in the detector proximity –due to the nature of the counting rooms the only possibility was to go to taller racks.

Therefore, a 63U - 19"rack was designed, ordered and installed in a test facility together with three newly designed adjusted for ATCA dimensions –2U air/water heat exchangers and three ATCA shelves. Over the months, there were many requests for different tests layouts of which most were addressed. Among them are tests with different computing architectures mixed –ATCA and VME (Virtual Machine Environment), to evaluate if these two very different (in terms of power dissipation and cooling needs) architectures can be combined and work in one rack. Or tests to evaluate the RTM power influence on the overall cooling of the board.

The 63U ATCA rack due to its large power dissipation has a strong impact on the counting rooms existing infrastructures such as HVAC (air conditioning) and water cooling systems, not to mention the noise contamination of the environment –this is why significant part of the test campaign was dedicated to address the unwanted heat release to the counting rooms, and consequently increasing the overall rack cooling efficiency. For this reason different ATCA shelf types were tested to evaluate their cooling capabilities, also tests with air leak tightened rack were carried out to diminish the escaping heat. In order to mitigate the generated noise the soundproofing on the rack level is necessary, the project to further reduce the environment noise contamination is ongoing and its introduction is schedule for the beginning of LS3.

One of the most important goals of this test campaign was to set the limit for the maximum power in front of the boards and on RTM that can be applied per slot to be able to stay within the 50℃ temperature target –the results of a measurement campaign with different types of load boards will be presented.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **113**   Type: **Poster**

KARATE - a setup for high rate tests on the CMS Outer Tracker 2S module readout chain

Thursday, September 5, 2019 4:55 PM (20 minutes)

KARATE (KArlsruher high RAte TEst) is a new system to stress the readout chain of strip modules for the future CMS Outer Tracker at HL LHC. The readout chain of a module starts with CMS Binary Chips (CBC) connected simultaneously to two sensors. The sparsified output is send out via an optical link. KARATE injects patterns with varying pulse heights, occupancies and trigger rates into the CBC giving full control on 48 channels at 40 MHz. Afterwards injection pattern are compared with readout patterns. The talk introduces the system and summarizes measurements on a CBC that is read out electrically.

Summary

KARATE (KArlsruher high RAte TEst) is a new test system to stress the readout chain of detector modules for the upgrade of the CMS Outer Tracker for the high-luminosity LHC. The readout chain of a 2S module consists of 16 CMS Binary Chips (CBC) connected simultaneously to two stacked silicon strip sensors. Each CBC contributes data to the level 1 trigger by detecting particles with large transverse momenta. The output is sparsified on two concentrator chips which are then connected to a Gigabit transceiver preparing the data for output through an optical module. Standard test systems such as test beams or radioactive source measurements need a track reconstruction or do have gaussian distributed hit profiles and do not reach the occupancy or trigger rates expected in the future outer tracker of CMS. KARATE uses a combination of LEDs and photodiodes to inject hit patterns with varying pulse heights, occupancies and trigger rates into the front-end of the CBC giving full control on 48 channels at 40 MHz. This gives the opportunity to directly compare injection patterns with readout patterns. The talk introduces the test system and summarizes measurements on a CBC that is read out electrically.

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **114**   Type: **Poster**

Design and operation of radiation hard 65 nm drivers for Silicon Photonics based optical links

Thursday, September 5, 2019 4:55 PM (20 minutes)

We will present the design and the performance of two drivers in 65 nm TSMC technology, for Silicon Photonics Mach-Zehnder Modulator (MZM) devices, able to withstand radiation levels of up few 1016 n/cm2 and ˜0.5 - 1 Grad. The drivers use a CML architecture and are optimized for >500 Mrad and a target a bit rate between 5 to 10 Gbps. They have been tested up to 800 Mrad showing about 25% degradation in voltage. Results of irradiation with ions will been shown. Finally, the results of operations with MZM and Ring-Resonators will be given and discuss the photonic-electronic integration.

Summary

Silicon Photonics is currently being investigated as an alternative to directly modulated laser-based radiation-hard optical links [1]: custom-designed Mach-Zehnder Modulators (MZM) withstand non-ionizing energy losses (NIEL) of up few 1016 n/cm2 using shallow etch optical waveguides and high doping concentrations in their p-n junctions. In order to exploit the high bandwidths offered by MZM based systems (few tens of Gbps) careful design of drivers is required.

The drivers presented are designed to operate the MZM in [1] and to sustain similar TID, thus about 0.5 −1 Grad. To be able to study the integration of the driver with the MZM, one driver has an internal pull-up resistor of 50 Ohm to possibly match the impedence of an external load, while the second doesn't, thus requiring an external regulator.

A CML (Current Mode Logic) architecture, designed in TSMC 65 nm technology, has been used to mitigate effects due TID and operate at a target bit rate between 5 to 10 Gbps. The core-MOSFETs having thin gate oxide are less affected by TID effects but, on the other hand, can sustain only 1.2 V, which doesn't match the 2 Vpp required to drive the MZM. To face this issue a cascode architecture is adopted in the last stage, which shares the output signals wide swing on the two-cascode MOSFETs. The driver has a 220×175 µm2 layout area and 149 mW power consumption. The post-layout simulations show a sustainable data-rate up to 10 Gbps.

The drivers have been fabricated by IMEC and received in September 2018. A printed circuit board (PCB) was designed to test the chip, whose naked die was glued on the board and its I/O pads wire bonded. The first driver was measured to deliver a single ended signal amplitude of about 1.2 V for a bandwidth up to about 3.5 GHz. The second driver (with internal pull-up) generates a single ended signal amplitude 1.2 V and a bandwidth of about 3 GHz. The eye diagrams show an open eye up to 5 Gbps. We are studying the reasons for the discrepancy between the expected performance of the chip after post-layout simulations and the actual measurement, addressing a non-optimal design of the board and of the wire-bonded connections. Measurements using a probe station are currently ongoing to bypass wire bonding and PCB effects.

The chip has been exposed to X-ray up to 800 Mrad, showing a degradation of the output voltage of about 25-30% for a signal frequency of 1 GHz. Tests with heavy ions have been performed, and results of the cross-section versus LET will be shown.

Finally, the chip was used to drive the MZM and Ring-Resonator described in [1]. The results of the measurements show a 3 dB bandwidth of about 2 GHz. The eye diagrams for the MZM show an open eye up to 5 Gbps.

References

[1] M. Zeiler, F. Vasey, et. al. "Radiation Damage in Silicon Photonic Mach-Zehnder Modulators and Photodiodes", IEEE Transaction on Nuclear Science, vol. 64, num. 11, Nov 2017

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Session Classification: Posters

Track Classification: Optoelectronics and Links

Contribution ID: **115**

Type: **Oral**

The analog readout channel for the Si(Li) tracker of the GAPS experiment

Tuesday, September 3, 2019 2:50 PM (25 minutes)

This paper describes the first experimental results from the characterization of the analog front-end designed for the readout of a Si(Li) detector based tracker. The instrument is conceived for the identification of low-energy cosmic-ray antiprotons and antideuterons in the GAPS (General Antiparticle Spectrometer) experiment to search for dark matter, whose launch is currently scheduled for late 2021. The analog front-end, featuring a dynamic signal compression to comply with the wide input range, has been designed in a 180 nm CMOS technology and was produced in two prototype ASICs. The development will be completed by early summer 2020.

Summary

GAPS (General Antiparticle Spectrometer) is an experiment that is being built by an international collaboration that aims to detect indirect signatures of dark matter through the identification of cosmic particles of antimatter. The experiment involves the use of a stratospheric balloon with a detection system composed of Si(Li), Silicon-Lithium, sensors divided into strips.

Each segment requires a readout channel suitable to resolve both X-rays (with a resolution of 4 keV FWHM at a strip capacitance of about 40 pF and a leakage current less than 10 nA) in the range of 20 to 100 keV and charged particles with energy up to 100 MeV. To comply with these requirements, the analog conditioning scheme is based on a low-noise charge-sensitive amplifier (CSA) performing a dynamic signal compression. This solution takes advantage of the non-linear features of a MOS capacitor in the feedback loop of the charge-sensitive preamplifier.

In the CSA, a continuous reset is provided by a Krummenacher feedback network.

This architecture was specifically chosen for its capability to compensate for the detector leakage current.

The amplifier is followed by a unipolar second order semi-Gaussian shaper. The shaping actually takes place in two steps. First the signal from the preamplifier undergoes an integration, then the shaping is completed by an active filter which provides one more integration and a differentiation. The signal peaking time at the shaper output is selectable among eight values, from 250 ns up to 2 us. After the filtering stage, the analog conditioning scheme is split into three different paths. On one side, a comparator is used to discriminate the amplified pulse: a threshold circuit converts the single-ended signal at the shaper output to a differential one and a differential DC threshold voltage is superimposed to the signal to drive the comparator. Another branch includes a single-ended to differential Sample\&Hold which provides a signal proportional to the peak of the shaped signal to the subsequent differential SAR ADC for the event data acquisition. On the third branch, the signal at the shaper output undergoes a further differentiation. The identification of the zero-crossing of the resulting bipolar signal provides a trigger, synchronous with the shaper peaking time, for the single-ended to differential Sample\&Hold.

The first two prototypes of this analog processing channel were designed in a 180 nm CMOS technology. The ASICs, named SLIDER4 and SLIDER8 (Si-Li DEtector Readout) were submitted and fabricated in 2018. The former includes only 4 standalone analog readout channels, whereas the latter is comprised of 8 readout channels, an 8:1 analog multiplexer, an 11-bits SAR ADC and a digital backend section which is responsible for ASIC slow control and serial interface communi-

cation. Experimental results will be used for the design of the final 32-channel ASIC. The device has to be ready in time for the launch of the balloon, that is currently scheduled for the second half of 2021 from the McMurdo station in Antarctica.

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Presenter: RICEPUTI, Elisa (University of Bergamo)

Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **116**   Type: **Oral**

Overview of the HL-LHC Upgrade for the CMS Level-1 Trigger

Wednesday, September 4, 2019 2:00 PM (25 minutes)

In view of the High-Luminosity LHC, the Compact Muon Solenoid (CMS) experiment is planning to replace entirely its trigger and data acquisition system. Novel design choices are being explored such as ATCA prototyping platforms and newly available interconnect technologies proving links up to 28 Gb/s. Higher-level trigger object reconstruction is performed through large scale FPGAs (such as Xilinx UltraScale) handling over 50Tb/s of fine granularity detector data with an event rate of 750 kHz. The system design and ongoing hardware R&D will be described.

Summary

The High-Luminosity LHC will open an unprecedented window on the weak-scale nature of the universe, providing high-precision measurements of the Standard Model as well as searches for new physics beyond the Standard Model. Such precision measurements and searches require information-rich datasets with a statistical power that matches the high-luminosity provided by the Phase-2 upgrade of the LHC. Efficiently collecting those datasets will be a challenging task, given the harsh environment of 200 proton-proton interactions per LHC bunch crossing. For this purpose, CMS is designing an efficient data-processing hardware trigger (Level-1) that will include tracking information and high-granularity calorimeter information. The current conceptual system design is expected to take full advantage of advances in FPGA and link technologies over the coming years, providing a high-performance, low-latency computing platform for large throughput and sophisticated data correlation across diverse sources

Modern technologies offer an effective solution to achieve these goals. The upgraded system makes use of newly released UltraScale Xilinx FPGAs technology implemented on the ATCA platforms. Data received from the tracker, the calorimeters and the muon systems represents a total bandwidth of 50 Tb/s, which are processed through innovative architecture designs such as Time-Multiplexed-Trigger (TMT). Higher granularity inputs, algorithms operating on a wider field of view allow for improved position and energy resolution of regional and global quantities. Optical interconnects are via 28 Gbps optical links are being studied and currently tested on various subsystems.

A dedicated Correlator Trigger will be used as central processor to compute high-level trigger objects and correlation among objects. A Time-Multiplexed approach is considered to provide enough latency for the implementation of sophisticated algorithms such as particle flow reconstruction. This approach is designed to allow for a high processing clock speed and thus efficient use of logic resources. The fully pipelined firmware approach of the TMT provides an efficient way to localize the processing, reduce the size and number of fan-outs, minimize ⬚routing delays and eliminates register duplication. The successful firmware implementation and testing of such algorithms will be discussed.

The talk will cover the technological aspects of the Phase II upgrade trigger system emphasizing on the many challenges of its implementation and in particular the innovative algorithms proposed. Results of its expected performance based on simulated data will be presented. The recent results from demonstration and hardware validation vs software emulator will also be detailed. The ATCA boards designed for this project are aiming towards a standardization of the data processing required for the future LHC electronics systems.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: **117**   Type: **Oral**

The APOLLO ATCA Platform

Tuesday, September 3, 2019 4:55 PM (25 minutes)

We have developed a novel open-source Advanced Telecommunications
Computing Architecture (ATCA) platform - APOLLO - which simplifies the
design of custom ATCA blades by factoring the design into generic
infrastructure and application-specific parts. The APOLLO "Service
Module" provides the required ATCA Intelligent Platform Management
Controller (IPMC), power entry and conditioning, a powerful
system-on-module (SoM) computer, and flexible clock and communications
infrastructure. The APOLLO "Command Module" is customized for the
application but typically includes one or more large
field-programmable gate arrays, several hundred optical fiber
interfaces operating at speeds up to 28 Gbps, memories, and other
supporting infrastructure.

Summary

The APOLLO platform provides a relatively simple hardware
environment and firmware and software toolkit which can be used for
the development of ATCA blades. The development of
high-performance ATCA blades for high-energy physics applications has
proven to be quite challenging. Many problems must be solved,
including: The delivery of adequate power (up to 400W in some cases);
cooling to remove the resulting heat; high-performance
communications interfaces for control, monitoring and data acquisition;
optical fiber management; and industry-standard debug and programming
interfaces for routine monitoring and recovery of "bricked" modules.

`The APOLLO Service Module is a standard-size ATCA blade with a`

7U x 180 mm cutout to accommodate one or two Command Module boards.
The Service Module design is quite conventional and uses standard
commercial power entry and conditioning modules, delivering 12VDC at
up to 30A to the Command Module(s). A CERN, Wisconsin or other
compatible IPMC in an SODIMM package can be accommodated. The IPMC
sensor bus is routed to several sensors on the Service Module as well
as to the sensor tree on the Command Module. Joint Test Action Group
(JTAG) master capability may be provided by the IPMC for diagnostic
purposes or reprogramming of the SoM as well as Command Module
programmable logic.

`The demonstrator APOLLO Service Module accommodates a commercial`

Zynq SoM which runs an embedded version of the Linux OS. The module
contains 1 GB of system memory, 512 MB of flash and a micro secure
digital (uSD) card interface. Flexible on-blade interfaces are
provided, including: Front-panel gigabit Ethernet, an additional
Ethernet to the switch; four 10 Gbps bidirectional serial links to the
Command Module, asynchronous serial and Inter-Integrated Circuit (I2C)

interfaces to the IPMC and Command Module as well as JTAG
master/target capability.

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A firmware and software reference design is provided for the
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APOLLO platform to allow new users to become quickly productive. A
set of Advanced eXtensible Interface (AXI) peripherals are included to
provide convenient access to the on-blade interfaces. A complete
Makefile and script-based build environment supports easy
customization of the Zynq system using a pure text system description
which integrates well with repositories and version control systems.
A reference software system provides access to all hardware features
using the IPbus software suite.

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Anticipated applications for the APOLLO platform include: The
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Level 0 trigger for the monitored drift tubes (L0MDT) in the ATLAS
experiment; the data acquisition and timing card (DTC) for the inner
tracker and the track finder for the CMS experiment. All hardware and
firmware of the APOLLO is open-source to the extent permitted.

The APOLLO demonstrator hardware will be presented, along with test
results and a brief description of each of the currently planned
implementations.

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Presenters: HAZEN, Eric Shearer (Boston University (US)); GLEIN, Robert (University of Colorado Boulder (US))

Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **118**　　　　　　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Triple-Modular Redundancy Deployment Optimization in the Sensor Readout System of the CBM Micro Vertex Detector

Tuesday, September 3, 2019 5:20 PM (20 minutes)

This paper describes the deployment and optimization process of triple-module redundancy (TMR) under high design constraints against single-event upset (SEU) and single-event transient (SET). It includes modeling of single-event effects (SEE) pulses with TCAD mesh model, TMR deployment strategies, and verification methods. The simulation result shows that the prototype with optimized TMR deployment has high reliability with respect to design requirements. The system can run for more than 5 years without crucial errors. And the equivalent error rate in the working environment is lower than 10^{-9}.

Summary

MIMOSIS-1 is a CMOS pixel sensor now being designed for the Micro Vertex Detector (MVD) of the Compressed Baryonic Matter (CBM) experiment. CBM will record data from gold-gold and proton-gold collision system. Highly ionization particles generated by collisions, such as gold, carbon and proton, may induce single-event effects (SEE), which are temporary or permanent circuit functional errors such as single-event upset, single-event transient, single-event latch-up, etc.

In logic circuits, triple-modular redundancy (TMR) allows achieving high reliability against SEE. However, circuits hardened by TMR feature at least three times the power and area of original circuits. Therefore, balancing design parameters is crucial.

To match the large hit rate, the MIMOSIS-1 readout architecture implements a 3-layer-buffer structure. Two types of digital circuits appear in this architecture: control logic and data buffer path. With calculation, the control logic of readout system is vulnerable to SEE pulse, while the data path is not.

A control logic is described as a finite state machine (FSM) where the internal status counter is driven an assignment loop. If SEE occurs in the assignment loop, the state will not be automatically restored until reinitialized and may induce a crucial error in the system. If SEE pulse occurs in the sequential processing, the status will be flushed during processing.

The time to recover from a SEE pulse provides guidance for deploying TMR or not. An FSM controlled by a pair of Enable and Disable signals can recover periodically back to idle state. If protected by TMR, the recovery time is only one clock period, much before the Disable signal. This shorter recovery time helps to decrease error rate.

The reliability of the TMR deployment design is evaluated by digital post-simulation. SEEs are modeled in the TCAD tool as transient pulses. The pulse amplitude is randomly generated according to the LET distribution of the incident particles. The pulse width depends on the driver load ratio of the impacted node. Design and verification are done iteratively on a module-by-module basis. At the end of the design, the system reliability verification is performed on the netlist with parasitic parameters that are output after layout and routing. Both fanout and clock trees are considered.

We found that without TMR, the system is susceptible to SEE at an unacceptable level. After our TMR optimization, the system can run for 5 years without crucial errors induced by SEEs. The equivalent error rate in the operational environment is lower than 10-9. Meanwhile the area and

power cost are only 20% and 50% higher compared to the original design.

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Presenter: ZHAO, Yue (IPHC)

Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: 119　　　　　　　　　　　　　　　　　　　　Type: **Poster**

Throttling Studies for the CBM Self-triggered Readout

Thursday, September 5, 2019 4:55 PM (20 minutes)

The Compressed Baryonic Matter experiment (CBM) will study rare probes in a heavy-ion environment at high interaction rates of up to 10 MHz. The observation of detached vertices requires a topological trigger, which is realized in software. CBM opted for a free-running readout, for reasons similar to LHC-b. The primary beam is delivered by a slow extraction synchrotron. To be able to operate the experiment at highest interaction rates, despite beam intensity fluctuations, a time-based throttling mechanism is under study. We will compare different throttling strategies.

Summary

This study is based on Silicon Tracking System (STS) subsystem which is closest to the target. The readout tree of STS comprises 16000 STS-XYTER ASICs, connecting to about 100 Common Readout Interface cards (CRI) which are interfaced to a global Timing and Fast Control system(TFC). Each ASIC comprises 128 readout channels. Each channel has a FIFO of 8 words. A FIFO-almost-full flag is asserted once 7 elements are filled. The ASIC counts the number of almost-full channels, and reports the busy alert to the CRI with a programmable alert threshold. Based on the busy information from all CRIs, the TFC decides if CBM as a whole should be throttled. The CRIs will propagate system dependent throttling instructions to the ASICs. This time-based throttling without trigger or event information, is designed to satisfy the limited latency requirement of TFC system.

The closed-loop simulation model comprises the event generator, the data flow model and result analysis. The data flow model describes relevant functionality of ASICs, CRIs and TFC, using the System Verilog language. It calls Linux shells to invoke the other stages realized in C++/ROOT. Each event means one collision and generates particles detected as hits. The hit rate equals to the event rate multiplying by hit size per event.

Throttling parameters are alert thresholds per ASIC, and fraction of ASICs reporting alerts. The total hit losses can be distinguished into controlled and uncontrolled losses. Uncontrolled losses come from FIFO overflow. Controlled losses represent full events discarded when either data input is stopped or complete events are cleared from FIFO.

The model is firstly verified through an event generator with a fixed hit rate. The output is equal to input when the hit rate is up to the maximum bandwidth of ASICs. Using a Poisson event generator, the model begins to lose data when the average hit rate is more than about 98% of maximum bandwidth. These conclusions approve our expectation.

Two throttling strategies are compared. The first is to stop accepting new hits, drain the ASIC FIFOs, then restart accepting hits. We select maximum 5 readout links for each ASIC. The fastest drain time in the STS-XYTER is about 20 us. The second strategy is to clear the FIFOs, then re-enable data taking immediately. They are abbreviated as "Stop"and "Clear"strategy.

For both strategies, lower alert thresholds lead to less uncontrolled losses and more controlled losses with increasing throttling-on operations. The total losses stay the same.

Furthermore, for event reconstruction random uncontrolled losses are much worse than block controlled losses. We define the time windows of block losses as discard windows. For Clear strategy, random losses are automatically removed when the FIFOs are cleared. The discard windows are

equal to FIFO cleared windows. For Stop strategy, the discard windows have to be extended out of the hit mask windows since uncontrolled losses exist before the hit masking.

Next, more complete evaluation criteria will be introduced. Realistic beam intensity fluctuations and distributions of bandwidth utilization of ASICs will be added.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **120**   Type: **Poster**

20 Mrad-TID Effects on Time over Threshold performance of GEMINI chip

Tuesday, September 3, 2019 5:20 PM (20 minutes)

GEMINI is an integrated readout system designed for Triple-GEM detectors. To fully exploit the potential of this technology, GEMINI produces outputs for both arrival time and energy thanks to Time-over-Threshold (ToT) technique. This work presents an analysis of the effect of up-to-20 Mrad-TID absorbed by GEMINI chip in lab environment with X-rays. ToT data analysis before and after irradiation allows estimating overall performance variation while reproducing typical use cases with emulated input signals. Experimental GEMINI rad-hard performance will open new applications for this device.

Summary

GEMINI is a 16 channels integrated readout interface for Triple-GEM detectors. Each channel detects events comparing input signal with a 9-bit threshold and provides digital output with an LVDS driver for 6.7 mW-per-channel power consumption. The digital output allows to acquire information on both arrival time and input charge thanks to ToT technique. A complete GEMINI characterization, developed for imaging applications, has been presented in [1].

This work presents the experimental radiation hardness study for GEMINI. The methodology observes the same channel on two GEMINI chips irradiated with X-rays up to 20 Mrad-TID. Overall performance variations are evaluated comparing ToT data acquired from the channel with the same input signals before and after irradiation. In this way also TID-induces mismatch is studied, so important in imaging applications. Input signal provided to the GEMINI chips was generated emulating Triple-GEM detector output with charge between 250 fC and 1800 fC, to make generated ToT data to reproduce possible events read from the detector.
ToT data histograms before irradiating the samples shows distinguishable peaks with positions consistent with input signals. ToT data acquired after irradiation shows that chip response variation due to radiation damage still allows correct operation of GEMINI. Comparison of average ToT obtained from each input signal before and after irradiation gives an average relative variation lower than 10 % and average variation of standard deviation lower than 6 %. These results suggest that corrections in data analysis could effectively address the problem of device ageing due to ionizing radiation.
Results obtained give positive indications about the adoption of GEMINI for ToT measurements with Triple-GEM detectors in new applications where rad-hard performance are mandatory like fusion experiments and monitoring of neutron sources.

[1] Mangiagalli, L. et al. "Characterization of GEMINI, a 16-channels programmable readout interface for Triple-GEM detectors in 180 nm CMOS.", TWEPP 2018

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **122**   Type: **Poster**

Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs

Tuesday, September 3, 2019 5:20 PM (20 minutes)

Single Event Effects represent one of the main challenges for digital designs exposed to ionizing particles in high energy physics detectors. Radiation hardening techniques are based on redundancy, leading to a significant increase in power consumption and area overhead. This contribution will present the SEE hardening techniques adopted in the pixel and strip readout ASICs of the PS-modules for the CMS tracker upgrade in relation to power requirements and error rates. Cross-section measurements on the silicon prototypes and expected error-rates evaluated for the CMS tracker particle flux and spectrum will be presented.

Summary

Single Event Effects (SEE) represent one of the main concerns for ASICs exposed to ionizing particles in high energy physics applications. Single event hardening techniques are based on redundancy and may introduce significant overhead in power consumption. In applications as the pixel and strip readout-ASICs for the CMS tracker upgrade, the readout front-end and the complex digital logic capable of performing on-chip real-time discrimination of particles based on transverse momentum, are required to operate with a very tight power budget of 100 mW/cm2. This contribution will present the SEE hardening techniques evaluated for the design in relation to power requirements and affordable error rates. It is essential to study how different parts of the design may benefit from different SEE protecting techniques and eventually which percentage of power consumption could be traded to reach higher radiation tolerance.

The full-size prototypes of the SSA and MPA ASICs incorporating all functionality to operate in the CMS experiment have been prototyped in a 65nm technology. For control state machines, a full triple module redundancy (TMR) architecture with 15um distance among triplicated registers was selected to prevent the ASICs to operate in unknown states. Single event tolerance in clock-gated logic, as the static configuration, was achieved with self-correcting feedback enabled by an SEU detection circuit. For the data memories, encoding techniques have been evaluated. A SystemVerilog/UVM verification environment allowed to simulate the single event effects on the ASIC functionality.

An heavy-ion irradiation campaign allowed to study the capability of the prototype to auto-correct single event induced errors in control and configuration logic and to evaluate the cross-section as a function of the Linear Energy Transfer (LET). The equivalent error-rate extrapolated for the CMS tracker particle flux and spectrum results in less than 5E-12 errors per bunch crossing per module for the continuous transmission of high transverse momentum particles information and less than 4E-11 errors per bunch crossing per module for the triggered readout of the full pixel and strip sensor data.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **123**   Type: **Oral**

The Engineering, Production and Quality Assurance of the Inner Barrel Staves for the Upgrade of the ALICE Inner Tracking System

Friday, September 6, 2019 9:25 AM (25 minutes)

A major upgrade of the ALICE Detector is underway during LHC LS2 (2019-2020). This includes a new Inner Tracking System (ITS) consisting of seven cylindrical layers of CMOS Monolithic Active Pixel Sensors. The building blocks of each layer are azimuthal elements called Staves.

The Inner Layer Staves are made of a carbon fiber support structure (spaceframe), a carbon fiber cold plate and a Hybrid Integrated Circuit (HIC) consisting of Pixel Chips and passive components bonded onto an aluminum polyimide Flexible Printed Circuit (FPC).

This contribution will describe the Inner Layers Staves, the manufacturing processes and the quality assurance methodologies.

Summary

A major upgrade of the ALICE Detector is underway during LHC LS2 (2019-2020) to enhance its measurement and data recording capabilities. This includes a new Inner Tracking System (ITS) which consists of seven concentric cylindrical layers of CMOS Monolithic Active Pixel Sensors. The basic building blocks of the detector are azimuthal segments called Staves, extending over the whole length of each layer.
The staves of the three inner layers are 30 cm long. Those of the middle and outer layers are 92 cm and 154 cm long.
The radial distances from the beam line of the three innermost layers are 23, 31 and 39 mm. The radial distance of the outermost layer is 39 cm.

The staves constituting the three innermost layers (Inner Barrel) are identical. They feature an unprecedented low material budget of 0.357% X0.

They are made of a carbon fiber support structure (spaceframe), a cold plate, and a Hybrid Integrated Circuit (HIC). The cold plate is a sheet of high thermal-conductivity carbon fiber with embedded polyimide cooling pipes.

The HIC of the Inner Layers consists of the assembly of a Flexible Printed Circuit (FPC), nine Pixel Sensors and passive components. The FPC has two Aluminum layers (25 μm thick) on a 75 μm thick polyimide substrate. Its design has to satisfy stringent constraints. The FPC distributes the analog and digital supplies and the reverse-bias voltage for the sensors. The traces for the readout of data at 1.2 Gb/s and for the slow control of the chips are routed without through-vias. The FPC and the chip floorplan were co-designed to make a stack-up of the FPC with only two layers possible and to spread the connections of the supplies over the entire surface of the chips.
The manufacturing of the FPC is very demanding. The thickness of the conductive layers, the cleanliness and roughness of bonding surfaces, and the resistance of metals are verified after production to ensure the required quality.

The assembly of the Inner Barrel HICs employs innovative techniques and demands constant monitoring, particularly against contaminations by small foreign bodies, that can damage the 50 μm thick chips.
Custom developed machines are used to test and align the pixel sensors on assembly jigs. Next, glue is carefully spread onto the FPC before it is flipped and placed on top of the pre-aligned chips. After curing and inspections, this assembly is then wire bonded with an innovative technique of

bonding through holes in the FPC itself. Finally, the assembled HIC is glued onto the cold plate and support structures to form an Inner Barrel Stave. Electrical tests are carried out at several steps during the assembly process.

This contribution will describe the engineering and manufacturing of the Inner Barrel Staves, and the quality assurance methods. It will discuss challenges, findings and lessons learnt.

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Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability

Contribution ID: **124**   Type: **Oral**

The lpGBTIA, a 2.5 Gbps Radiation-Tolerant Optical Receiver for InGaAs photodiodes

Friday, September 6, 2019 9:25 AM (25 minutes)

The Low Power GigaBit Transimpedance Amplifier (lpGBTIA) is the optical receiver amplifier in the lpGBT chipset. It is a highly sensitive transimpedance amplifier designed to operate at 2.56 Gbps. It is implemented in a commercial 65 nm CMOS process.

The device has been designed for radiation tolerance and, in particular, to accommodate the radiation effects in photodiodes that manifest themselves as an increase of both their dark current and junction capacitance. The operation of the lpGBTIA was successfully tested and this paper describes its architecture, the experimental and irradiation results.

Summary

High-energy physics experiments in the LHC require high-speed optical links for transmission of large amounts of data between the experiments and the counting room. In certain detectors or sub-detectors, the radiation levels reach 2 MGy and 1E15 particles/cm2. High-speed optical links and their constituent electronic and optoelectronic devices need thus to sustain such high radiation levels. In this paper, we report on the design of the radiation-tolerant lpGBTIA that is a highly sensitive optical receiver amplifier operating at 2.56 Gbps.

The first element of an optical receiver is the photodetector to convert the input optical signal into an electrical current. Given the relatively low radiation-induced degradation of the responsivity of InGaAs photodiodes, they are good candidates to implement optical transmission systems in HEP experiments. However, for these devices, radiation also results in a strong increase of the leakage current (up to 1 mA) and in a large increase of the junction capacitance especially at low reverse bias voltages that are typically encountered in detector systems due to power supply voltage limitations.

The lpGBTIA is designed to accommodate radiation-induced changes in InGaAs photodiodes. It is based on a differential structure to suppress power supply and substrate noise. It consists of a transimpedance amplifier, a limiting amplifier and a 100 Ohm output stage. The design is implemented in a commercial 65 nm CMOS process and radiation tolerant design principles have been followed in the design to ensure a high tolerance to the total ionizing dose.

Due to the relatively large impedance of the photodiode bias circuit, large dark currents can reduce the voltage across the photodiode and thus prevent the optical receiver from operating properly. To avoid this, a novel bias circuit for the photodetector has been designed and implemented in the chip to maintain sufficient voltage across the photodiode in the presence of the high DC leakage currents induced by irradiation. Moreover, this helps to maintain the capacitance of the photodiode within the low values needed for operation at 2.56 Gbps.

The bandwidth and the input-referred noise current of the lpGBTIA depend significantly on the photodetector capacitance. The pre-irradiation capacitance photodiode used in this optical receiver is typically less than 500 fF. The transimpedance input stage of the lpGBTIA is however optimized for 2 pF to accommodate the expected increase due to radiation.

The lpGBTIA chip size is 1750 μm × 461 μm. It has been fabricated and it is currently under characterisation. First measurements at 2.56 Gbps display a sensitivity better than -19 dBm for a BER of 1E-12. The differential output across an external 100 Ohm load remains constant at 400 mVpp even for signals near the sensitivity limit. The total power consumption is less than 67 mW. Radiation tolerance tests are being prepared and the results will be presented at the conference.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **127**   Type: **Oral**

Commissioning High-speed readout for the LHCb VELO Upgrade

Friday, September 6, 2019 11:30 AM (25 minutes)

The new LHCb Vertex Locator for LHCb, comprising a new pixel detector and readout electronics will be installed in 2020 for data-taking in Run 3 at the LHC. The electronics centre around the "VeloPix" ASIC at the front-end operating in a triggerless readout at 40 MHz. Custom serialisers send zero-suppressed data from the VeloPix at a line rate of 5.13 Gb/s. Signal integrity tests of the data path components showing characteristic impedance and jitter measurements will be presented. System tests of the complete electronic and optical chain, along with early results from the VELO module production sites will be shown.

Summary

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s/ASIC and produce an output data rate of over 15 Gb/s, and totalling 2.85 Tb/s of data for the 40M pixels of the whole VELO.

This paper will present an overview of VELO front-end and back-end electronics, with an emphasis on tests of the high speed transmission. The detector consists of 208 tiles of 3 VeloPix flip chipped to a silicon sensor surrounding the beam as close as 5 mm in a secondary vacuum tank and extremely high and inhomogeneous radiation environment.

The VeloPix transmits zero suppressed, time-stamped, unsorted packets with binary hit information over 5.13 Gb/s links. The VELO detector opens during LHC beam injection, to prevent damage from the unstable beams. To facilitate movement, the high speed links are implemented with low mass, flexible data tapes. Signals are driven out of the vacuum chamber through a Vacuum Feed-through Board (VFB) and subsequently converted from electrical to optical in the Opto-Power Board (OPB). 300 metre optical links originating at the OPB drive the data from the LHCb cavern to the PCIe40 back-end data acquisition boards in the surface, where they are recovered, synchronized, sorted, packed and sent in real time to the CPU farm to be further processed.

As the project enters its early production phase, several full system integration tests have been performed to qualify the modules for production. Signal integrity (eye diagram, S-parameters, characteristic impedance, BER) of the different parts of the readout chain (hybrids, flexible data tapes, VFB, OPB) has been controlled. The DAQ system was tested using three full-scale prototype modules in a beam test in November 2018. Results of the readout performance and synchronisation between the modules will be shown.

Some of the latest test results include:
- Jitter measurements of the VeloPix output links have been performed and show a relation to VeloPix serialiser PLL phase. We scan the phases to find the optimal minimum bit-error rate (<1e-14). These scans are supplemented with eye diagrams at the end of the electronic readout chain.
- An equalisation procedure is used to tune the analogue parameters of the VeloPix. Extra noise on odd columns of the VeloPix matrix have been identified during this procedure. An alternative calibration method, using the high speed output links, and not suffering this extra noise will be shown.

A full readout chain slice of the detector has been qualified prior to the electronics module production. New results are expected of these high rate scans at the nominal operating temperature of the detector at -30C.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **128**   Type: **Poster**

Back-end firmware for the LHCb VELO upgrade phase I

Thursday, September 5, 2019 4:55 PM (20 minutes)

LHCb detector is a general purpose experiment instrumented in the forward region at the LHC, specialized in b- and c- physics, new physics and CP violation. The Vertex Locator (VELO) detector is being upgraded along with the rest of the tracking system and readout architecture during 2019-2020. The aim of this poster is to present the architecture of the control and readout firmware on the VELO specific back-end boards. Latest progress towards the installation and commissioning will be shown.

Summary

The upgrade of the LHCb experiment is being installed during the long shut down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the front-end ASIC (VeloPix). The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s/ASIC and produce an output data rate of over 15

Gbits/s, adding up to 2.85 Tbit/s of data for the 40 Mpixels of the whole VELO.

The VeloPix transmits zero suppressed, time-stamped, non sorted packets with binary hit information over 5.13 Gbits/s links with a custom data protocol (GWT) to the back-end boards in the LHCb surface. Back-end readout boards (FPGA based) recover, synchronize, sort, clusterize the data and send it to the LHCb CPU farm for further processing. Due to the lack of a hardware trigger at LHCb, a significant processing load is placed on the CPU farm. A campaign to reduce this processing overhead for LHCb has been initiated, and implementing more of the processing in the FPGA back-end is critical to this endeavour.

This poster will present an overview of VELO back-end firmware. This VELO firmware is comes in two variants, (control and data acquisition) derived from a LHCb common

framework. The control firmware is dedicated to the distribution of slow control and fast timing signals to the front-end electronics. Customization to the control framework for

the SLVS protocol used by VeloPix will be outlined.

The data acquisition firmware accepts the data from the twenty links of one VeloPix module with an input rate up to 100 Gbits/s. The GWT transmission protocol and its

motivating factors over the standard GBT will be described. The time-ordering of the unsorted input data will detailed and the impact of this modification to the standard LHCb firmware framework. We will present new algorithms for clustering the VeloPix hits, and the positive impact to the downstream CPU processing downstream. Methods for simulating the firmware algorithms and the monitoring tools developed for verification will also be presented.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **129**   Type: **Poster**

A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature

Thursday, September 5, 2019 4:55 PM (20 minutes)

A mixed-signal ASIC developed to readout silicon photomultipliers (SiPM) at low temperature is presented. The chip is designed in a 110 nm CMOS technology. Both single photon counting and Time-over-Threshold (ToT) operating modes are supported. In single photon counting mode an event rate of up to 5 MHz per channel can be accommodated. The time resolution is 50 ps and the target power consumption is less than 5 mW per channel. The architecture of a first 32-channel prototype is described. Dedicated test structures to qualify critical building blocks at cryogenic temperature have also been deployed.

Summary

There is a growing interest in the use of Silicon photomultipliers (SiPMs) operating at cryogenic temperatures. The largely suppressed dark count rate observed at liquid Xenon and liquid Argon temperatures makes such sensors ideally suited to equip large area detectors like those needed in dark matter and neutrino experiments. Research programs to explore the possibility of building total body PET scanners based on noble liquids readout by SiPM are also ongoing.

ALCOR (A Low-power Circuit for Optical Readout) is a first prototype of a mixed-signal ASIC optimised for the readout of SiPMs at low temperature. The mixed-signal channel is implemented in an area of 440x440 um2 and can be configured to operate either in single photon counting or in Time-over-Threshold (ToT) mode. In the first mode, the arrival time of the single photons is recorded. The ToT mode is useful when many photons pile-up in the individual SiPM pixel and are treated by the electronics as a single continuous signal. Such a situation is common, for instance, in PET applications. In each channel, a regulated common-gate input stage acts as the interface between the sensor and the rest of the chain. Then the signal is conditioned by two amplifiers with programmable gain and shaping time. Two leading edge discriminators with configurable threshold generate the trigger CMOS signals that are fed to the channel digital control block. A coarse time stamp, derived from a binary 15-bit counter on-channel, is generated while four low-power time-to-digital converters (TDCs), generate the fine counter information of 9-bit. The clock frequency can be up to 320 MHz. In this condition, the TDCs have a binning of 50 ps and a dead-time of 150 ns. Data generated is a 32-bit payload that includes the time-stamp, the channel ID, and the specific TDC address. Generated data are collected to the periphery and transmitted off-chip using 4 LVDS drivers.

The design of chips working at cryogenic conditions entails several issues. The increased carriers mobility at low temperature may induce an accelerated device ageing. This can be partially mitigated by avoiding minimum length transistors and/or reducing the power supply voltage. Furthermore, transistor and digital standard cells are usually not modelled below -40 ℃. To gain useful insights in view of the design of the ALCOR chip, dedicated test structures were fabricated. These include a copy of the front-end amplifier, a bandgap reference voltage, LVDS transmitters, basic digital gates, a clock buffer and a synchronisation circuit. The characterisation work is ongoing. The ALCOR design will be then finalised and optimised using inputs provided by the results obtained on the test structures. At the conference, the experimental results of the test structures will be presented and the architecture of the ALCOR chip will be discussed in detail in the poster.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **130**   Type: **Poster**

40 MHz Level-1 Trigger Scouting for CMS

We will discuss the feasibility of a system capturing Level-1 intermediate data at the LHC beam-crossing rate of 40 MHz and carrying out online analyses based on these data. This 40 MHz scouting system has the potential to enable the study of otherwise inaccessible signatures. In such a system, data from the Level-1 trigger is preprocessed in an FPGA before being transferred to a computer for further analysis. A demonstrator was operated at the end of Run-2 using trigger data from CMS. We will present this system as well as the possible architecture of a Phase-2 40 MHz scouting system.

Summary

The CMS experiment will be upgraded for operation at the High-Luminosity LHC to maintain and extend its optimal physics performance under extreme pileup conditions. Upgrades will include an entirely new tracking system, supplemented by a track trigger processor capable of providing tracks to the Level-1 trigger, as well as a high-granularity calorimeter in the endcap region. New front-end and back-end electronics will also provide the Level-1 trigger with high-resolution information from the barrel calorimeter and the muon systems. The upgraded Level-1 processors, based on powerful FPGAs, will be able to carry out sophisticated feature searches with resolutions often similar to the offline ones, while keeping pileup effects under control.

In this paper, we discuss the feasibility of a system capturing Level-1 intermediate data at the beam-crossing rate of 40 MHz and carrying out online analyses based on these limited-resolution data.

This 40 MHz scouting system would provide fast and virtually unlimited statistics for detector diagnostics, alternative luminosity measurements and, in some cases, calibrations, and it has the potential to enable the study of otherwise inaccessible signatures, either too common to fit in the L1 accept budget, or with requirements which are orthogonal to "mainstream"physics, such as long-lived particles.

To realise such a system, data from the Level-1 trigger is branched off into a dedicated system with optical multi-gigabit inputs and powerful FPGAs for preprocessing before being moved into the memory of compute nodes. Algorithms familiar from the big data industry can be used to quickly operate on the recorded data before a distilled data set is stored on disk.

We discuss the design of a demonstrator system operated at the end of Run-2 using the Global Muon Trigger data from CMS. This demonstrator was implemented on a Xilinx KCU1500 Acceleration Development Board that is equipped with a Xilinx Kintex Ultrascale FPGA and provides eight GTH transceivers for optical multi-gigabit communication as well as two x8 PCIe Gen3 interfaces bifurcated to a x16 edge connector. The demonstrator board received muon data via all eight input links at 10 Gbit/s and applied a basic zero suppression scheme before transmitting the remaining valid data to the host computer via DMA. To optimise the performance during data taking measurements of the performance of the board to host DMA transfer for different drivers and packet sizes were done. The system was then used to record data during the last week of the LHC's proton-proton run in 2018 as well as during the entire 2018 lead-lead run. At the LHC's peak instantaneous luminosity up to 800 MB/s were transferred to the host, this value dropping with decreasing luminosity.

Plans for further demonstrators envisaged for Run 3 as well as the requirements and possible architecture of a Phase-2 40 MHz scouting system are also discussed.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 131   Type: **Oral**

Power hybrids for silicon modules with macro-pixel and strip sensors for the CMS Phase-2 tracker upgrade

Wednesday, September 4, 2019 11:55 AM (25 minutes)

The upgraded CMS tracker at the HL-LHC will feature new silicon modules with a macro-pixel sensor and a strip sensor on top of each other. The modules require three supply voltages (1.0V, 1.2V, 2.5V), which are provided in a two-stage DC-DC conversion powering scheme. Two DC-DC buck converters are supplied in parallel from the first powering stage. A four-layer flexible power hybrid based on the FEAST2 and bPOL2V5 DC-DC converters by CERN has been developed, using custom air-core inductors and a custom shield. The power hybrid development will be presented and the results from the characterization will be discussed.

Summary

The CMS Collaboration will exchange its silicon strip detector during Long Shutdown 3 of the LHC with a completely new silicon tracker, which will be more radiation tolerant and be able to cope with the increase in instantaneous luminosity. The new tracker will feature modules with two closely spaced silicon sensor that are read out by common readout ASICs. This allows to correlate hits in the two sensor planes in order to estimate on-chip the transverse momentum of charged particles. Only information of tracks with a transverse momentum above a configurable threshold will be forwarded at the bunch crossing frequency to the Level 1 trigger, reducing the data volume to a manageable level. In this way tracking information can be used in the Level 1 trigger of the experiment. One type of these new modules, referred to as PS modules, features a strip sensor and a macro-pixel sensor, with 1.5mm long macro-pixels.

The PS modules require three operating voltages: 2.5V for the VTRx+ opto-electrical converter, 1.2V for the LpGBT ASIC, the VTRx+, the readout chip of the strip sensor, and the analog domain of the readout chip of the macro-pixel sensor, and 1.0V for the digital domain of the macro-pixel readout chip. This is realized in a two-step DC-DC conversion powering scheme, using DC-DC buck converters. DC-DC conversion allows us to reduce the current on the long supply cables and thus to reduce voltage drops and Ohmic losses on these cables. The first DC-DC conversion stage will be implemented with the CERN bPOL12V ASIC, receiving about 10V at the input and providing 2.5V for the VTRx+ and the second stage. The CERN bPOL2V5 ASIC will be used in the second stage, with two bPOL2V5 connected in parallel to the first stage. The three DC-DC converters are located on a flex PCB, the Power Hybrid, which sits on the edge of the PS module, very close to the sensors. The Power Hybrid connects via flexible pigtails to the two readout hybrids of the module.

Prototype Power Hybrids have been developed and produced. The FEAST2 ASIC is used in place of the bPOL12V in the first stage, since the bPOL12V was not yet available at the time of the development. For the second stage, though, close-to-final prototypes of the bPOL2V5 are used. The PCBs are flex boards with four copper layers. The bPOL2V5 is assembled in flip-chip technology, featuring a bump-bond pitch of 300μm. The boards have been tested and characterized. We will report on the development and the test results, including dynamic behavior as a function of load, efficiency, line and load regulation, voltage drops, the inductor and shield development, as well as conducted and radiated noise emissions.

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Session Classification: Packaging and Interconnects

Track Classification: Packaging and Interconnects

Contribution ID: **132**   Type: **Oral**

Multi-channel time-tagging module for fast-timing Resistive Plate Chamber detectors

Thursday, September 5, 2019 2:00 PM (25 minutes)

To update associated electronics with fast-timing resistive plate chamber (RPC) detectors, we present here a multi-channel time-tagging module implemented on a low-end and low-power cyclone V FPGA. A key part in each channel has a time-to-digital converter (TDC) in tapped-delay-line (TDL) architecture (built with delay line and associated registers, fine-time encoder, coarse-time counter and look-up-table memory). The firmware implementation employs several techniques, including input-signal reshaping and bubble-noise filtering to deal with GBVS (ground bounce and Vcc sag) effects. It has successfully been tested in all-channel simultaneous operation conditions, with 9.2 to 12.85 ps time resolution and full event-detecting efficiency.

Summary

New generation of resistive plate chamber (RPC) has been proposed to equip two of the high η muon stations in view of the high-luminosity large hadron collider (HL-LHC) phase. The RPC should be instrumented with precise timing readout electronics. The system requires multi-channel readout and time-tagging electronics with low power consumption. This has led us to develop a new readout board including a time-tagging module. The readout board incorporates two multi-channel front-end readout ASICs followed by a low-cost and low-power Cyclone V GT FPGA. The time tagging is performed by the FPGA based on multi-channel time-to-digital converters (TDC) to fulfill the following requirements: full event-detecting efficiency, up to 16-channal simultaneous measurements, 30ns dead time and less than 60ps RMS (root mean square) time resolution.

The time-tagging module via FPGA firmware implementation has 48 channels: 46 for input signal tagging, one for external trigger signal tagging and another for reset signal tagging.

One key part of the module is the TDC in each channel. To implement it, we have adopted the tapped-delay-line (TDL) architecture (built with delay line and associated registers, fine-time encoder, coarse-time counter and look-up-table memory). For operation with a 400-MHz clock, the delay-line consists of over 500 delay elements, each connected to pipeline D-type flip-flop (DFF) registers. It operates in two phases. In the first (within a clock cycle), one single input signal's transition edge can successively toggle hundreds of delay-elements as it propagates in the delay line. In the second phase (the two following cycles), the DFF register could toggle simultaneously at the clock's rising edge. This simultaneous large-scale toggling in a small area could induce ground bounce and Vcc sag (GBVS). The GBVS effect is more marked in the low-power and narrow-wiring FPGA. Furthermore, for simultaneous operation of TDC channels, the resulting GBVS is a source of interferences, which corrupts the delay elements' states (called bubble noise) and temporally slows down the signal transition time (due to power supply voltage fluctuations). Consequently, this degrades the accuracy of time-tagging measurements.

To deal with this issue, firstly we use a signal-reshaping technique in the delay line implementation: to reshape input signal pulse with an edge-detecting logic followed by a DFF. Secondly we propose a bubble-noise-filter-based encoder to detect the first transition bit and to distinguish between signal and noise according to signal's transition pattern.

Each channel includes a coarse time counter for extending measurement range, and a look-up-table memory for fine-time-to-digital conversion. For an input tagging channel or the trigger one, it gives the measured signal's timestamp. The reset tagging channel employs a TDC to detect

extern reset signal from the system, for a timing precision of system synchronization below 20 ps. The final signal's timestamp is obtained by subtracting the measured timestamp by the reset one.

The time-tagging module has successfully been tested in all-channel simultaneous operation. It gives a tagging time resolution of 9.2 to 12.9ps RMS, with full event-detecting efficiency. The next system test at CERN has been scheduled.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **133**   Type: **Poster**

The Firmware for the European Spallation Source Cavity Simulator

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Cavity Simulator reproduces the behavior of superconducting cavities and high power amplifiers used in the medium and high beta sections of European Spallation Source (ESS) linac. The device is foreseen to be used for tests and development of the ESS's LLRF control system. High-performance Xilinx Kintex Ultrascale FPGA runs dedicated firmware, which performs all calculations including the simulation models. The firmware is also responsible for device control and communication. This contribution presents the general overview of the Cavity Simulator's firmware together with simulation and measurement results.

Summary

The Cavity Simulator reproduces the behavior of superconducting cavities and high power amplifiers used in the medium and high beta sections of the European Spallation Source (ESS) linac. The simulated phenomena include, but are not limited to: klystron bandwidth and non-linearity, the influence of the power supply ripple, cavity dynamics, beam loading, Lorentz force detuning, microphonics, as well as mechanical modes. The device is foreseen to be used for tests and development of the ESS's LLRF control system.

A digital FPGA circuit executes the simulation algorithm. However, the Cavity Simulator operates on RF and analog signals. Therefore a dedicated frontend and set of data converters are used. The input RF signals are first down-converted to an intermediate frequency and then sampled by high-speed ADCs. Vector modulator circuits generate the RF output signals. Additionally, the device is equipped with RF reference, Local Oscillator (LO) and clock signals generation modules.

High-performance Xilinx Kintex Ultrascale FPGA runs dedicated firmware, which performs all calculations including the simulation models. The firmware is divided into three blocks: hardware interface, model and communication. The first part is responsible for the connection to the data converters and other circuits used. It also converts the signals from the ADCs into an IQ complex vector format, which is used for the signal processing. The cavity model consists of six tunable IIR filters that simulate the transfer function of all pi-modes. Other elements of the model detune the filters. The device mimics the piezo actuator used for fine-tuning of the cavity resonance. The piezo simulation includes modeling of the hysteresis, based on a Dahl model. The firmware architecture is optimized for the shortest possible processing time. So are the selected algorithms and their implementation.

The firmware is also responsible for device control and communication through an Ethernet network or USB interface. These functions are realized by a Micro-Blaze softcore processor, which communicates with other blocks through the AXI bus.

This contribution presents the general overview of the Cavity Simulator's firmware together with simulation and measurement results.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: **134**   Type: **Poster**

Simulation of new charge summing and hit allocation algorithm

Thursday, September 5, 2019 4:55 PM (20 minutes)

Modern VLSI technology allows the development of new class X-ray imaging detectors capable of capturing an image in various energy ranges in one shot. Such spectroscopic imaging detectors have a high demand for the spatial and energy resolution of individual photons. With decreasing size of pixels, the charge cloud generated by the primary photon interaction, and in high-Z materials also by the fluorescent photon interaction, is shared across several pixels. That limits both spatial and spectroscopy resolution. This paper presents a novel charge summing algorithm called Winner-Master-Slave and describes the functionality, implementation, and simulation of the proposed algorithm in Verilog-AMS.

Summary

Several charge summing algorithms have been developed and implemented in ASIC. Unfortunately, most of the algorithms sum charge just from the four neighboring pixels. That prevents the possibility of collecting charge from more considerable distance which is generated by long-travel fluorescent photons. That limits spatial resolution as well as spectroscopic capabilities of detectors.

In this work, a new fully asynchronous algorithm called Winner-Master-Slave (WMS), which deals with charge sharing effects as well as with long-travel fluorescent photons, is presented. WMS is designed to work fully asynchronous, and it is capable of charge summing over 25 pixels (cluster size 5 x 5). Every interaction of a photon with the detector which generates a charge cloud is called an event. WMS is event-driven; thus whenever an event occurs WMS automatically creates a cluster and sums total charge in the cluster.

Described functionality of the novel algorithm has been implemented in Verilog-AMS and simulated with AMS simulator in Cadence® Virtuoso® environment. The algorithm has been systematically tested using randomly generated clusters. The simulation outcome proved that WMS algorithm solves several problems of existing solutions and is suitable for implementation in a front-end ASIC for a spectroscopic imaging detector.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: 135   Type: **Oral**

Increased radiation tolerance of CMOS sensors with small collection electrodes through accelerated charge collection

Tuesday, September 3, 2019 11:30 AM (25 minutes)

Mini-MALTA is a Monolithic Active Pixel Sensor prototype developed in the TowerJazz 180 nm CMOS imaging process, with a small collection electrode design (3um), and a small pixel size (36.4 um), on high resistivity substrates and large voltage bias. It targets the outermost layer of the ATLAS ITK Pixel detector for the HL-LHC. This design addresses the pixel in-efficiencies observed in MALTA and TJ-Monopix to meet the radiation hardness requirements. This contribution will present the results from characterisation in particle beam tests that show full efficiency up to 1E15 neq/cm2 and 70 Mrad.

Summary

Several monolithic CMOS sensor technologies have been considered for the outer pixel layer of the ATLAS detector upgrade for the High-Luminosity LHC [1], requiring radiation tolerance to about 2E15 1 MeV neq/cm2 and 70 Mrad. The TowerJazz 180 nm CMOS imaging process with small, low capacitance collection electrodes offers a better combination of analog performance and power consumption. It allows full CMOS circuitry in the pixel, which in combination with a modification in the process allows full depletion of the epitaxial layer. First measurements performed on this technology showed improved radiation tolerance by an order of magnitude with respect to the un-modified process [2]. Following these results, two large scale prototypes were designed and fabricated. The TJ Monopix that used the well-known synchronous column drain readout architecture, and the MALTA that implemented a new asynchronous readout offering lower power consumption and higher matrix bandwidth. However, both prototypes showed severe charge collection inefficiencies near the pixel edges after irradiation despite the process modification [3-4]. Detailed investigation including TCAD simulations [5] showed the low lateral electric field near the pixel borders significantly increases the collection time for signal charge generated in that area, especially for larger pixel pitches. The study confirmed that the pitch increase from 25 and 30 micron of the relevant early test structures to 36.4 micron or more in the large scale prototypes caused a significant penalty. Two further sensor modifications were introduced to improve the lateral electric field at the pixel border and implemented on a new small prototype chip, the Mini-MALTA. The first sensor modification is the introduction of a gap in the low dose additional deep n-type implant, and the second is the introduction of a deep p-type implant, both near the pixel border. In addition to the sensor modifications the size of two NMOS transistors was increased in an effort to reduce the random telegraph noise observed on both TJ Monopix and MALTA. This paper presents first experimental results using source and test beam obtained with Mini-MALTA before and after irradiation. Efficiency measurements show significant improvement in the pixel edges. Thus confirm that both sensor and front-end modifications significantly improve the performance and bring sensors with 36.4 micron pixel pitch to practically full detection efficiency after irradiation up to 1E15 neq/cm2, an comparable with low energy proton irradiated devices up to 7.1e14 neq/cm2 and 94 Mrad.

[1] The ATLAS Collaboration, ATLAS Phase-II Upgrade Scoping Document, CERN-LHCC-2015-020

[2] H. Pernegger et al., 2017 JINST 12 P06008, https://doi.org/10.1088/1748-0221/12/06/P06008

[3] I. Caicedo et al, PIXEL 2018

[4] R. Cardella et al, PIXEL 2018

[5] M. Munker et al, PIXEL 2018

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Session Classification: Radiation Tolerant Components and Systems

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **136**   Type: **Oral**

External scrubber implementation for the ALICE ITS Readout Unit

Tuesday, September 3, 2019 11:55 AM (25 minutes)

Abstract

Commercial components are used in the readout
electronics of the upgraded ALICE Inner Tracking System detector,
hence a system-level single event upset (SEU) mitigation strategy
for the FPGAs is needed to ensure correct operation. Inclusion of
a flash-based auxiliary FPGA on the Readout Unit enables
fault-tolerant operation, by implementing periodic blind
scrubbing to correct SEUs in the configuration memory of the main
FPGA, an SRAM-based Xilinx FPGA responsible for data transfer and
detector configuration. This contribution discusses the external
scrubber solution on the Readout Unit, focusing on the FPGA
design and software design. Test results are also presented.

Summary

The ALICE Inner Tracking System (ITS) is currently being upgraded
to prepare for LHC Run 3, which is scheduled to start in 2021.
The upgraded ITS will consist of 7 layers of ALPIDE ASICs (a high
granularity monolithic active pixel sensor). The ALPIDEs are
organized in 192 staves, consisting of 9 to 196 ALPIDEs depending
on the layer. Each stave is read out by a Readout Unit (RU)
located in racks inside the ALICE magnet at around 6 m from the
interaction point. In the location of the RUs, the high-energy
hadron flux is expected to be about 1 kHz/cmˆ2
in Run 3. Thus the design of the Readout Unit and of its FPGAs
is required to be radiation tolerant. The main FPGA on the RU is
an SRAM-based Xilinx Kintex Ultrascale FPGA, and single event
upsets (SEUs) will happen in the configuration memory of the
device. Scrubbing of this memory is implemented to correct the
SEUs. Based on earlier irradiation campaigns with a Kintex-7
device, it was decided to use an auxiliary device (auxFPGA) to
scrub the configuration memory. The auxFPGA is a flash-based
Microsemi ProASIC3 A3PE600L FPGA, which is the commercial
counterpart of the radiation tolerant RT ProASIC3 series. The
large flash cells are radiation tolerant by technology, so
mitigation is only needed on specific design elements such as
registers and memory.

In order for the scrubbing to be effective, SEU mitigation
techniques such as Triple Modular Redundancy (TMR) and error
correction coding (ECC) is also applied to the design of the RU
main FPGA. Additionally, the design scrubbing rate is at least
three orders of magnitude higher than the mean expected SEU rate.
Hence, the SEUs will not accumulate, improving the effectiveness
of the TMR.

Configuration and scrubbing of the main FPGA are the main tasks of the auxFPGA, utilizing the Xilinx selectMap interface. The scrubbing and configuration files are stored on a Samsung flash-memory with 1048/1024 bit hamming coding for single bit error correction and double bit error detection. The combination of ECC encoded configuration files and local TMR of the auxFPGA design achieves a high degree of radiation tolerance.

To test the functionality of the auxFPGA, a Python-based suite of unit-tests is set up and runs on the CRU host computer, which significantly shortens the testing time during development. The tests are also a reference for extended integration-tests and system level operations, as well as final detector control system functions.

The auxFPGA is currently under commissioning and integration tests are ongoing. All basic functionality works as intended, and it has been verified that continuous blind scrubbing does not interfere with the normal operation of the RU and main FPGA in normal environmental conditions. It will be shown that control, monitoring and data readout run as normal while scrubbing is continuously executed.

This contribution will give details of the design, implementation and testing in the system of the external scrubber, of the storage and management of the configuration files and of the fault injection features.

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Session Classification: Radiation Tolerant Components and Systems

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **137**
Type: **Poster**

MARTA's DAQ system

Thursday, September 5, 2019 4:55 PM (20 minutes)

We successfully developed, built and tested a low power and stand alone DAQ system to be used with RPCs to measure the muonic component of air showers in the framework of MARTA. The MARTA system includes a front-end readout, high voltage, detector monitoring and a central unit to manage the different components of the system. The front-end is based on the MAROC ASIC coupled to an FPGA respecting the strict demands of field operations in Cosmic Ray experiments. Prototypes were produced and deployed, performing as expected. An engineering array will be installed at the Pierre Auger Observatory.

Summary

Muon Array with RPCs for Tagging Air showers (MARTA) was designed to measure the muonic component of the extensive air showers (EAS) that are created when a high energy cosmic ray interacts at the top of the atmosphere.
Extensive air showers can be detected using Cherenkov water tanks.
Light particles are absorbed in the tank while muons, which are deeply penetrating, cross the tank.
In a MARTA station, detector units are placed in a concrete structure below the water tank to detect the muonic content.
Each unit consists of a Resistive Plate Chamber (RPC) detector, HV, RPC monitoring and a front-end that are placed inside a aluminum box.
A central unit will be responsible for communications, trigger, data transfer and power distribution for the units of each station.
These detectors are expected to be deployed in the field where the environment is not favorable, with space and power limitations and harsh weather conditions.
Moreover, an engineering array as a proof of concept will be installed at Auger.

In this work, we will present the DAQ that was created and developed to read the fast RPC signals and sustain the adverse conditions presented in the field.
RPCs are mostly used in laboratory and only now are starting to be being tested in the field.
Other than be able to read the fast RPC pulses, this system also needs to be low power, compact, stable and reliable for low maintenance operation.
The center piece of the DAQ is the front-end.
Due to the space and power limitations it is based on a low power ASIC: MAROC3n developed by OMEGA.
The ASIC is able to perform a simple threshold measurement (hit) as well as measure the charge that is deposited by the avalanche in the detector.
An FPGA is responsible for the control of the ASIC.
It will also receive and store the ASICs digital outputs before they are sent out to the central unit.

After optimizing the ASIC's parameters to measure the RPC signals, validation tests were performed to both the hit and charge measurement.
The hit measurement results show a similar performance for different temperatures.
Efficiency measurements were obtained simultaneously using MARTA's front-end and an establish one with compatible results.
The charge measurement was studied for different ASIC's and RPC's configurations and several spectra acquired that are consistent with the spectra measured in the past for this kind of detectors.

The trigger used will be given by the water tank DAQ.
It is typically of the order of 100 MHz which is compatible with the dead times of the measurements.

The central unit is based on a FPGA with a dual-core ARM processor.
It is connected via LVDS to the front-ends for fast communication and I2C to the monitoring and HV.
It is also connected to a server via ethernet where data will be stored.

The first prototype station is expected to be installed in the next couple of months as production of the detectors, electronics and structures are already complete.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experi-ence

Contribution ID: **138**

Type: **Oral**

A Clock and Data Recovery Circuit for the ALTAS/CMS HL-LHC Pixel Front End Chip in 65 nm CMOS Technology

Tuesday, September 3, 2019 11:30 AM (25 minutes)

A Clock-Data Recovery (CDR) circuit has been developed to be integrated in the RD53B front end chip for the HL-LHC upgrade of the ATLAS/CMS pixel detector. The 160 Mb/s input data stream is recovered and used to synthesize the 1.28 GHz clock that drives the high speed output link. Robust locking is guaranteed by starting up in PLL mode and afterwards automatically switching to CDR operation. Full characterization was performed with the aid of a dedicated test chip. Less than 60 ps p-p jitter was measured while the circuit remains fully functional after a TID of 600 Mrad.

Summary

In order to cope with the unprecedented requirements of the HL-LHC in terms of output bandwidth and radiation tolerance, a clock-data recovery (CDR) circuit has been designed in 65 nm CMOS technology and was integrated in the RD53A demonstrator chip for the phase II upgrade of the ATLAS/CMS pixel detector. This chip has been produced and successfully tested. To increase locking reliability and reduce jitter, an improved CDR has been designed for the RD53B chip. The 160 Mb/s input command stream is recovered and used to synthesize all the necessary clock signals for the RD53B chip including the 1.28 Ghz clock that drives the high speed output link.

Since the CDR is a timing-critical block, it must incorporate a robust locking mechanism and output jitter < 200 ps p-p. Furthermore it has to withstand up to 500 Mrad total ionizing dose (TID) and be tolerant to single event effects (SEE). Locking is guaranteed by starting up in PLL mode, providing a training pattern to a phase frequency detector (PFD) and afterwards automatically switching to CDR operation by a counter with appropriate preset value. The CDR loop utilizes an Alexander phase detector (PD) which is aided by a rotational frequency detector (FD). A low noise charge pump drives the low pass filter which consists of a 300pF metal-metal capacitor and programmable resistance up to $1\ k\Omega$. A unity gain buffer is used to reduce the charge sharing effect during the switching phase. The voltage controlled oscillator (VCO) consists of a three stage differential ring oscillator with gain equal to 1.5 GHz/V. It has been designed for low period jitter of $J_c = 450\,fs$ which is essential to increase input jitter tolerance. The feedback loop is completed by a fully triplicated divider with synchronous architecture. The PFD, PD and FD were designed using a customized low threshold library with increased transistor size for TID robustness. To accelerate the closed loop jitter optimization, each block was simulated separately and the extracted parameters were used to construct behavioral models. The closed loop parameters were than tuned for maximum phase margin and optimum loop bandwidth of $\approx 5\ MHz$.

A dedicated test chip was designed to characterize the CDR circuit. The necessary support blocks (bias generators, serializer, cable driver, etc.) were imported from RD53A chip library. The chip was irradiated with X-rays up to 600 Mrad while being cooled down to -14^oC. Locking was always successful down to a power supply voltage of 0.9V, with 1.2V nominal value. Less than 60 ps p-p jitter was measured while providing input data with 5 ps RMS jitter. After irradiation to a TID of 600 Mrad, the jitter increased by only 13\% caused mostly by duty cycle distortion at the output. SEE robustness was tested with a heavy ion beam and the results are currently analyzed and will also be presented.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: 139   Type: **Poster**

Overview of Electronics Developed by ISE for the European Spallation Source Project

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Institute of Electronic Systems (ISE) of shall design and deliver hundreds of pieces of various control, signal distribution, and safety modules to be used at the European Spallation Source research facility by the Low-Level RF control, Phase Reference, and Beam Diagnostic systems. This contribution presents the design, as well as strategies and results of acceptance testing of selected modules produced by ISE for the project.

Summary

European Spallation Source (ESS), currently constructed in Lund (Sweden), is a research facility based on a 2000 MeV proton linac, that will deliver neutrons for material sciences. A significant part of the project is designed and delivered by partner laboratories as in-kind contributions from various countries. The Institute of Electronic Systems (ISE) of the Warsaw University of Technology (WUT) shall design and deliver hundreds of pieces of various control, signal distribution, and safety modules to be used at the ESS facility by the Low-Level RF (LLRF) control, Phase Reference and Beam Diagnostic systems.

An RF SplitBox module was designed by the ISE team to distribute RF signals shared between the LLRF control and interlock systems. The device must be configurable at the production phase to support different RF power levels and frequencies. It must also introduce as little temperature induced phase drifts as possible. Multiple long-term measurements of various high-frequency power dividers were performed. Transformer and integrated components were rejected in favor of a custom designed Wilkinson divider. Scattering parameters of each unit are measured to verify proper operation by an automatic test-stand.

The Phase Reference Line system for the ESS is designed as a passive, almost 600 m long 1 5/8" coaxial rigid line distributing 352 MHz and 704 MHz signals to almost 300 outputs located along the proton linac tunnel. The entire line is temperature stabilized down to +/- 0.1 degree C to assure phase stability reaching 0.1 degree. The PRL project consists (among others) of more than 150 sections of the coaxial rigid line including precise temperature control hardware, 56 diplexer and power splitter modules as well as almost 20 temperature control boxes. All PRL components passed rigorous RF parameters, signal phase drift and production tests within test setups designed for this project.

The Personal Safety System Relay Switch shuts off the RF signal at the input of a high power amplifier feeding the accelerating cavities. It must be robust and assure high reliability. The testing procedure includes measurement of current consumption and logic outputs as well as scattering parameters.

ISE also co-designed and manufactured front-end modules for signal conditioning of the Beam Current Monitors (BCM). To assure reliable operation of devices each piece must be tested in a repeatable manner. A dedicated automated test-stand was prepared for the BCM subproject. The BCM front-end filters the input signals and matches their voltage range to the level compatible with the uTCA digitizer cards. The stable-over-time pulses can be generated to calibrate the system. To achieve high availability, two redundant power supplies were used and are automatically switched on-line in case of failure. A random unit was selected for long-term observation. Every

second a calibration pulse was triggered and recorded with an oscilloscope. One hundred thousand waveforms were acquired and compared with each other. Later each device was tested with waveform count reduced to 200 cycles.

This contribution presents strategies and results of acceptance testing of selected modules produced by ISE for the ESS project.

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **140**   Type: **Poster**

Radiation Tolerance Specification & Testing Campaign For the Mu2e Experiment at Fermilab

We present an overview of the approach of the Mu2e experiment at Fermilab to address radiation tolerance issues in the front-end electronics. The campaign includes simulations, specifications, testing, and mitigation strategies. The tests include tolerance measurements of Total Ionizing Dose (TID), Non-Ionizing Energy Loss (NIEL), and Single Event Effects (SEE). We describe how the simulations were performed, the resulting performance requirements, the test setups developed, the campaigns executed, and some of the mitigations that were required.

Summary

Work is in progress to build the Mu2e experiment at Fermilab. The goal of the experiment is to measure the ratio of the rate of the neutrino-less conversion of muons into electrons in the field of a nucleus, relative to the rate of ordinary muon capture. This would be an example of charged lepton flavor violation (CLFV), which has never been observed experimentally. Observation would provide unambiguous evidence for physics beyond the Standard Model.

The experiment will use a high intensity, low energy muon beam, with a detector capable of efficiently identifying 105 MeV electrons while minimizing background from conventional processes. The detector has several subsystems: a 20,000 channel Tracker used for measuring the trajectory of charged particles; a 3,500 channel Calorimeter used to measure energy, position and time; and a 29,000 channel Cosmic Ray Veto, which surrounds the detector to identify cosmic rays that can cause backgrounds. The detectors all have front-end electronics that amplify and digitize the detector signals, and programmable logic for processing ant transmitting data off-detector. Data is read out over optical links, which also provide the system timing (clock-encoded data.) DC-DC converters are used on the front-ends, which receive input voltages from off the detector and convert to levels needed by the front-end circuitry. A technical decision was made early on to not use any custom integrated circuits in the front-end electronics, and instead use only commercial off-the-shelf (COTS) parts.

Beginning in 2015, we began to study the radiation levels in the front-end electronics of the experiment, primarily using MARS15, with some simulations done with GEANT4. MARS15 simulations start with events from proton-on-target,and follow the traversing of particles through the detector components. Fluxes of electrons, photons, and hadrons at critical locations are simulated, and Total Ionizing Dose (TID) is derived. and flux of electrons and hadrons. Further processing of the data produces 1 MeV neutron equivalent fluence (Non-Ionizing Energy Loss, or NIEL,) and the fluence of hadrons in specified energy bins, from which the fluence of Single Event Effects (SEE) can be derived. Applying the strategy and experience gathered from the ATLAS and CMS experiments at the LHC, we observed that the radiation tolerance required for the tracker electronics for a 5-year running period was of order 600 krad TID, 6E12 n/cm2 NIEL fluence, and 1E11 p/cm2 SEE fluence. These levels were much higher than originally estimated, and pose a challenge for COTS parts. The Mu2e Electronics Integration Team began coordinating radiation tolerance measurements of front-end components. Issues with all designs were encountered the tracker and calorimeter subsystems. One outcome was a decision to use the VTRx optical transceiver developed at CERN for the data and timing interface on the front ends, and to use rad-hard Draka fiber for the fiber optics.

We will present the process that we developed to assess the radiation tolerance requirements for this large, multi-subsystem detector. We will describe some of the radiation measurement campaigns, and some of the surprises that we encountered that necessitated design changes.

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Session Classification: Posters

Track Classification: Radiation Tolerant Components and Systems

Contribution ID: **141**　　　　　　　　　　　　　　　　　　　　　　Type: **Poster**

The first ASIC prototype of a 28 nm time-space front-end electronics for real-time tracking

Tuesday, September 3, 2019 5:20 PM (20 minutes)

A front-end ASIC for 4D tracking is presented. The circuit includes a charge-sensitive amplifier, a discriminator with programmable threshold, and a time-to-digital converter. A prototype has been designed and integrated in 28 nm CMOS technology. The presented design is part of a project aiming at reaching a high resolution both in space and in time, to provide front-end circuitry suitable for next generation colliders.

Summary

The next generation of colliders will produce a large number of events, and therefore will require a more tight selection of data to be stored for off-line analysis. Future track triggers should be able to perform a tight selection of events, even in case of high pile-up (150 to 200) and high background noise. The problem of track recognition can be simplified by adding time information to spatial information, thus providing '4D' data at the pixel output. The track trigger will use both time and space information, to reconstruct tracks with better accuracy.

The TimeSPOT project, funded by INFN, aims at the development of a complete processing chain for particle detection with high resolution, both in space (< 100 μm) and in time (< 100 ps). The project will exploit the potential of 3D detectors, made either of silicon and of diamond, and will take advantage of the high speed and of the radiation hardness performance provided by the 28 nm CMOS technology.

This communication describes the read-out electronics and the design of the first silicon prototype for the TimeSPOT project. The ASIC has been designed in 28 nm CMOS technology, and includes all the relevant blocks of the front-end: charge amplifier and shaper, discriminator, time-to-digital converter, and output interface.

The first stage of the chain is a Charge Sensitive Amplifier (CSA) capacitively matched with the sensor. The CSA includes a sensor leakage current compensation, and its output signal is compared with a programmable voltage threshold, provided by a 6-bit DAC. The time difference between this pulse and a reference clock is digitized by a time-to-digital converter, and the resulting data is sent off-chip by a serial output with Low-Voltage Differential Signalling (LVDS) interface.

In the first prototype, circuit blocks can be characterized individually, or they can be connected together to form a processing chain. The architecture of the chip and the results of prototype characterization will be addressed in the presentation.

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Session Classification:　Posters

Track Classification:　ASIC

Contribution ID: **142**   Type: **Poster**

VICE++: a building block of the debug and quality control systems for CMS ECAL upgrade on-detector electronics

Thursday, September 5, 2019 4:55 PM (20 minutes)

VICE++ is a FPGA-based unit with interfaces compatible with the upgrade Very
Front End (VFE) and Front End (FE) boards. Once equipped with the appropriate firmware, it act
as a test unit for debugging and tuning of different versions
of VFE and FE prototypes, and as a building block of the QC/QA systems for VFE and FE production.
FPGA power allow run lpGBT-FPGA firmware, hence the unit can emulate some functionality of
the on-detector electronics for the off-detector electronics tests. The board can be used to evaluate
the quality of the data transactions from the FE to the Back-End electronics.

Summary

VICE (VFE Interface Converting Electronics) is a small FPGA-based interface board, designed at
early stage of the CME ECAL upgrade on-detector electronics development to match the legacy
Very Front End (VFE) output –single ended parallel LVDS, to GBTx –based Front End (FE) prototype
input –serial bipolar SLVS-400. The board happened to be very useful, much beyond the simple
interface domain as it allowed to decouple VFE and FE prototypes testing, providing all necessary
test functions.

VICE++ is the more powerful extended version of this board, designed for the next stage of ECAL
on-detector electronics prototypes: CATIA & Lite-DTU –based VFE with 160MHz ADC sampling,
and lpGBT –based FE with 1280Mb/s s-links and 10.24 Gb/s serial links.
The board is designed to provide all data, clock, and control signals for VFE prototypes on one side
and FE prototypes on the other. It contains two fast optical links to host computer, running up to
10.3Gb/s for the data readout and control.
Being equipped with the appropriate firmware, it can emulate most of the functionalities of the FE
card for the VFE prototypes tests, as well as VFE card for the FE prototypes. It has also capacity to
run the full speed readout of one Lite-DTU without compression to debug and optimize the data
compression procedure.
FPGA is powerful enough to run lpGBT-FPGA firmware, hence the board can also emulate large
fraction of the on-detector electronics functionality for the upgrade off-detector electronics (BCP)
tests.
Presentation will describe design of the VICE++ board and different application for the debug-
ging and testing of all upgrade ECAL electronics components. It will also address the VICE++ -
based design of the Quality Control and Quality Assurance systems for the VFE and FE cards mass
production.

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Presenter: Mr SINGOVSKI, Alexander

Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **143**

Type: **Poster**

A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePIx4

Tuesday, September 3, 2019 5:20 PM (20 minutes)

SAR converters are usually the natural choice to implement monitoring ADCs. Additional circuits for calibration are needed to compensate process variations which become more important for large resolutions and deep-submicron technologies. This paper presents a 12-bits second-order incremental sigma delta converter for TimePix4 fabricated in TSCM 65nm. It does not need calibration and is robust to process variations because most of the signal processing is performed in the digital domain. It provides a maximum conversion rate of 1kHz/s, enough for monitoring the internal signals of the chip, consuming only 8µW. Simulations show a SNR of 84.9dB operating in free-running mode.

Summary

Delta-sigma converters offer high resolution at moderate speeds and present low sensitivity to process variations because a significant amount of the signal processing is performed in the digital domain. This robustness to process variations is an important feature nowadays, where the use of deep submicron processes is generalized and parameter spread is more significant in each new technological node. It was decided to exploit this robustness to implement a 12-bit delta-sigma ADC for monitoring bias signals instead of the common SAR solution, which requires a calibration circuit for such level of resolution. However, delta-sigma converters are not suitable to measure DC signals. Instead it was used an incremental delta-sigma converter, which can be considered a delta-sigma data converter in transient mode, because it can be reset and easily multiplexed among several channels. The presented ADC is implemented inside TimePix4 and its purpose is to monitor 32 internal bias voltages. These are DC signals, so a sampling rate of 1ksample/s as much is needed. The chip has been designed in a 65nm CMOS process, and it will be submitted for fabrication during 2019.

The design of the ADC started by working at architectural level with Matlab. This allowed to determine the oversampling ratio, the open gain and band-width of the operational amplifiers, as well as to dimension the sizes of the capacitors. Instead of creating Simulink models for each integrating stage, it was used the SimSides library for Matlab developed by INM-CNM to design delta-sigma converters. It was found that a second order Cascaded Integrators Feed Forward (CIFF) architecture operating with an oversampling rate of 210 allowed to meet the requirements in terms of conversion speed, area and power consumption.

The phases of the first integrator stage were modified in order to work with single-ended input signals and provide a fully differential output for the fully differential second stage. The operational amplifiers are fully differential folded cascode with a switched-capacitor circuit to generate the common-mode voltage. With the 65nm process, it was not possible to reach an open-loop gain of at least of 75dB as needed, so gain-boosting techniques were used to enhance the gain to 90dB. The power consumption of the converter at an operating oversampling frequency of 250kHz is of 8µW working at 1.2V. A lot of care was taken in the layout to avoid crosstalk between signals that could degrade the performances of the ADC. The size of the layout of the modulator is of 110x150µm2. The correct operation of the ADC was tested by simulating the converter in free-running mode,

that is, as a conventional delta-sigma converter. In incremental mode, the test of the whole range would have required a week at schematic level, so we only tested some small regions of the whole range for all corners at schematic and layout level. Results shown that ADC achieved the desired resolution for an input range of 25mV-1175mV. For the free-running test mode, it was obtained a SNR 84.9dB for the given input range in the typical case.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **144**   Type: **Poster**

Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The compact structure of the HGTD proposed for the High Luminosity ATLAS detector upgrade at the CERN LHC requires a design to match the tight mechanical and electrical constraints. Our solution with a flexible printed circuit manages the signals to read out and control the modules, to bias the sensors with high voltage and to power the ASIC. It is crucial to match the characteristic impedance of the lines. The high voltage bias requires clearance and shielding to limit the interference with the digital logic. We present the results of several geometrical and electrical tests performed on the first prototype.

Summary

The High Granularity Timing Detector (HGTD) proposed for the High Luminosity upgrade of the ATLAS detector at the LHC at CERN has the purpose to provide a very precise time information for each track (30 ps resolution) to assign them correctly to the hard scatter vertex or to the additional collisions taking place at the same bunch crossing (pile-up).

The HGTD consists of 8000 modules that are the basic unit of the detector. A bare module comprises a Low Gain Avalanche Detector (LGAD), which requires biasing, up to 1000 V, bump-bonded to two ASICs. A module has a surface of 2x4 cm2 . The signal transmission from each elementary unit to the electronics boards that surround (peripheral electronics) the detection region requires customized electronics. High Voltage (HV), slow control, high-speed differential signals (1.28 Gb/s) and clock at different protocols should be transferred. All these signals must be contained in an independent cable to be fitted in the very limited available space. Considering all the relevant specifications, a flexible printed circuit (FLEX cable) is the most appropriate choice to fulfill the requirements. A module consists of a bare module wire-bonded and glued to the FLEX cable.

The cable thickness should not exceed 350 μm (up to 10 FLEX cables max. will be stacked) and the width should be less than 18 mm outside of the bare module surface. The length is defined by the different positions of the modules on the active area and of the corresponding connector on the peripheral electronics. The FLEX cables length ranges from 160 to 750 mm.

The study phase and the analysis of the constraints lead to the design of a prototype with the maximum expected length, but only a few lines of each type to address the potential limitations of the technology. To distinguish between design and production effects, the approach to the same design by two different manufacturers was studied.

The prototype consists of a stack-up of four layer of polyimide with a total thickness of 350 μm.

The electrical requirements for the ASIC are two voltage supplies at 1.2 ± 0.2 V and the impedance of the lines to be 80-100 Ω for differential and 45-55 Ω for single-ended lines. The high-voltage to bias the sensor is expected to be in the range 600 −1000 V.

Several electrical and geometrical tests on the prototype show that a behavior within or close to the specifications. The comparison of the discrepancies between two different manufacturer processes gives an overview of the technological limitations.

An exhaustive characterization with static and dynamic tests will be presented. We discuss the details of the Time Domain Reflectometer (TDR) measurements for the transmission lines. We estimate the performance of the data-link in terms of Bit Error Rate (BER) for the longest cable as

well as the influence of the HV bias on the high-speed digital logic. Therefore, a small test setup based on a Kintex FPGA evaluation board emulates the realistic conditions of the cable in normal operations.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **145**   Type: **Poster**

The VRP - a Versatile Readout Platform for the nuclear experiments at HIRFL-CSR

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics and relative applications. The experiments at the HIRFL-CSR drive the development of new detectors. Aiming to reduce the developing time and cost of each detector system, a Versatile Readout Platform (VRP) has been designed as a tentative common readout platform for the detectors at HIRFL-CSR. By adopting the Smartfusion2 FPGA SOC as the main FPGA, the VRP is expected to withstand the radiation environment in the HIRFL-CSR. This paper will discuss the design, implementation and first performance results of the VRP.

Summary

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science and relative applications. The various experiments at the HIRFL-CSR drive the development of different detector systems. The front-end electronics of each detector is specific, but the readout electronics is possible to be commonly shared. Aiming to reduce the developing time and cost of each detector system, the Versatile Readout Platform (VRP) has been designed to serve as a tentative common readout platform for the detectors at the HIRFL-CSR.

The VRP board is a radiation hard, 6U PXI standard, general-purpose platform. By adopting the Smartfusion2 FPGA SOC as the main FPGA, the VRP is expected to withstand the strong radiation in the HIRFL-CSR. The VRP hosts two high-speed fiber optical links, the PXI interface, the Ethernet Interface, the LVDS interface for digital input and the high-speed ADC for analog input. The drivers of each interface have been pre-defined in the firmware, so the user logic can be easily included to realize specific functions.

As of writing, the VRP is being commissioned in the gamma detector in the HIRFL-CSR. This paper will discuss the design, implementation and first performance results of the VRP.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 146   Type: **Poster**

Evaluation of embedded Linux distributions suitable for control and monitoring CMS phase 2 custom electronics

Thursday, September 5, 2019 4:55 PM (20 minutes)

Xilinx Zynq SoCs are used by the CMS TDAQ in its back-end electronics since LHC Run-2, between 2015-2018. For the Phase 2 upgrade of the LHC, about 1000 devices will be deployed, comparable to the number of High Level Trigger (HLT) nodes today. This scale presents challenges for the SoC integration in the experiment network, system administration, network management, booting process and root file system management among others. We present an evaluation of various Linux distributions (PetaLinux, Yocto, ArchLinux, CentOS) and a proposal of how to address the challenges involved in developing and maintaining custom linux distributions for CMS.

Summary

System on Chip (SoC) devices have become popular for custom electronics HEP boards since the advent of FPGAs with integrated CPUs. Advantages include the tight integration between the FPGA and the CPU, high flexibility in terms of hardware design, and the relatively powerful CPUs which are capable of running fully fledged operating systems like CentOS, Archlinux and even Ubuntu.

SoCs provide a powerful hardware fulfilling the needs for configuration, control and monitoring from the perspective of Trigger and Data Acquisition.

The CMS Trigger and Data Acquisition System already features a small number of back-end Xilinx Zynq SoCs, in use since LHC Run-2 in 2015-2018. These are stand-alone and isolated installations. For the High Luminosity phase of the LHC, completely new and upgraded CMS back-end electronics, with auxillary Xilinx Zynq devices, will be built. About 1000 such SoC devices are expected to be deployed. This is comparable to the number of High Level Trigger(HLT) nodes today.

The scale of the project poses challenges for the SoC integration in the experiment network, system administration services, networking configuration and management. Typical challenges like time distribution, IP/Name distribution (DHCP or other), unique identification of the devices, security, remote/authorised access, remote system logs, read-only or read-write root file systems, NFS mounted root or application file systems, local or network system boot, and configuration management form the crux of our research. Furthermore, with the emergence of more powerful embedded CPUs, it will be interesting to assess how much of the data acquisition software stack could, or should, be deployed on those devices compared to server PCs.

A few Linux distributions (compatible with ARM 32 and 64 bit architectures) which could be of interest for SoC devices in the context of CMS, have been indentified. The major distributions include PetaLinux, Yocto, ArchLinux, CentOS.

In this paper we will propose a strategy to address the complexity of building a distribution, discuss the requirements on hardware resources, and aspects related to network and sysadmin integration in the context of CMS.

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Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: **147**   Type: **Poster**

Design and test of current DACs for threshold tuning of front-end channels for the High Luminosity LHC

Thursday, September 5, 2019 4:55 PM (20 minutes)

This work is concerned with the design and the characterization of digital-to-analog current converters, developed in a 65 nm CMOS technology, conceived for threshold tuning of front-end channels at the HL-LHC experiment upgrades.

Two DAC structures were integrated in a small prototype chip, that was submitted in August 2018 in the framework of the RD53 developments. The prototype has been tested before and after exposure to X-rays up to a TID of 460 Mrad(SiO_2).

The main performance parameters of the two structures will be compared and discussed in the conference paper.

Summary

Pixel readout chips at the High-Luminosity LHC will deal with extremely high particle rates in a severe radiation environment. In the phase 2 upgrade, the innermost layers of the ATLAS and CMS tracker detectors will be equipped with readout chips that are required to operate with very low stable threshold (of the order of 1000 electrons), with a per-pixel noise occupancy not exceeding 10^{-6}. In order to achieve this goal, it is vital that the analog front-end features excellent performance from the standpoint of noise and threshold dispersion. Moreover, such performance has to be retained after exposure to total ionizing doses (TIDs) of the order of 500 Mrad($SiO2$). Threshold non-uniformities in a multi-channel readout system can be addressed by means of threshold tuning, a procedure during which the threshold of each pixel is locally adjusted with an in-pixel digital-to-analog converter (DAC).

The CERN RD53 collaboration was founded in 2013 to investigate new technologies and architectures for future readout chips. RD53 identified the 65 nm CMOS technology as the candidate process for the development of mixed-signal integrated circuits for the new generation of tracking systems based on high granularity silicon pixels. This technology features the good degree of tolerance to ionizing radiation that is typical of CMOS processes in the 100 nm regime and enables the integration of advanced in-pixel analog and digital functions. In 2017, the collaboration submitted the RD53A chip, a large-scale chip including a matrix of 400 x 192 pixels (with 50um x 50um pitch), embodying three different analog front-end designs, called Synchronous, Linear and Differential.

A prototype chip including two standalone channels of the Linear front-end has been submitted in August 2018 with the aim of comparing two different DAC designs. Both the submitted channels include a charge sensitive amplifier (CSA) with Krummenacher feedback and a threshold discriminator exploited for time-to-digital conversion. One of the channels is equipped with a 4-bit, binary weighted current DAC featuring cascoded current mirrors, whereas the second one includes a more compact, 5-bit current DAC, with the same binary weighted architecture, but with regular current mirrors.

The performance of the two DACs has been evaluated, in terms of output range, integral and differential non-linearity, before and after the exposure to a total ionizing dose of 460 Mrad($SiO2$) of X-rays. A comparison of the performance of the two DACs will be discussed in the conference paper, in view of their operation in the threshold tuning system of a full-size pixel detector readout chip.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **148**   Type: **Poster**

Qualification of the final LHCb VELO electronics

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Vertex Locator of the LHCb will be upgraded in 2020. As the installation is approaching all the electronics have to be verified and tested. In this poster, the final test setup for all the components and the procedures accomplished will be described. Problems detected and solutions adopted will be explained.

This process goes from visual inspection test of the different boards or bare Asic qualification to a full system test with the final components. The auxiliary boards and specificly designed firmware to properly facilitate the testing will be illustrated.

Summary

The LHCb Vertex Locator will be fully replaced by a new pixel detector in 2020. This new detector is composed of 208 sensors bump bonded to 624 VeloPix Asics (3 Asics per sensor). All these Asics are wire-bonded to 208 hybrids and controlled by 104 GBTx Asics using another specific hybrid. These hybrids are interconnected with 208 flex tapes using 832 connectors (4 each tape) and placed with high precision on a silicon substrate together with the tiles (1 sensor + 3 VeloPix) that are used as a support and as micro-channel CO_2 cooling. The VeloPix Asics readout signals and the GBTx control signals are transmitted via 208 flex tapes divided in two segments: one with low mass in the acceptance area made of micro-strip lines and another made of ˜0.5 metre strip-lines. These readout flex cables are connected to the hybrid using 728 connectors and have to be able to transmit 5.13 Gbps signals. The flex tapes are connected to a Vacuum Feed-through Board and which are then connected to an Opto and Power Board.

Due to the quantity of sensors, Asics, and boards required and the inability to replace most of the components after the installation, precise systematic tests have to be done for all the detector components at each production and assembly step. This poster presents an overview of all tests performed as well as the qualification process accomplished. The problems found and the solutions adopted will be explained. First, the full Asic qualification procedure before and after bump bonded and the results obtained are presented. Second, the visual inspection of all the hybrids and flex cables is described in order to spot any problems that could affect the high speed signal transmission. Third, the tests made on all the boards in terms of high speed communication are illustrated. TDR or eye diagram measurements are used for this test with the help of specifically designed auxiliary boards. Finally, a slice system test is described mentioning the problems found when all the fully tested and validated components are join together.

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Session Classification: Posters

Track Classification: Production, Testing and Reliability

Contribution ID: **149**   Type: **Oral**

Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades

Thursday, September 5, 2019 2:50 PM (25 minutes)

Serial powering is the baseline option for the pixel detectors in both the ATLAS and the CMS experiment targeting the phase II HL-LHC upgrade. The Shunt-LDO regulator is integrated in the front-end chips to generate the required supply voltages. A new compensation scheme has been developed to operate stable with large Low-ESR load capacitances. A two-stage bandgap voltage reference circuit has been implemented to improve regulation performance. Security features have been added to protect against overvoltage and overload. Additional features have been added to allow regulator operation with small supply currents during the installation phase.

Summary

A current based supply scheme of serially connected modules has been chosen as the baseline powering option for the pixel detectors in both the ATLAS and the CMS experiment targeting the phase II HL-LHC upgrade. In this supply scheme the Shunt-LDO regulator is integrated in the pixel front end chips to convert the current supply into the required supply voltages for the analog and digital part. For these regulators parallel operation on chip and module level is required to avoid single points of failure and hot spots to provide redundancy and to increase system reliability. Balanced shunt current distribution across parallel placed devices is reached even if the regulators generate different output voltages by introducing a configurable slope at the Current-Voltage characteristic of the regulator input. The regulator is implemented with cascoded core transistors in 65 nm CMOS technology to tolerate supply voltages up to 2V and high radiation doses at the same time. Due to the large chip size and the large amount of pixels integrated in the front-end chips the regulator needs to deal with a shunt current of up to 2 A and to operate stable even with large Low-ESR capacitances of 300 nF connected to the regulator output. For that purpose, a new compensation scheme has been developed which does not rely on the ESR of the external blocking capacitor which has been successfully applied to the regulator. A two-stage bandgaps scheme has been implemented to improve the PSRR of the regulator reference signals and to reach overall excellent line and load regulation performance. A first untrimmed and 2V-tolerant bandgap reference circuit is supplied by the unregulated input voltages and generates a reference for a linear preregulator. The preregulator supplies a second bandgap reference circuit which is then used to generate the regulator reference voltages. In addition, security features have been integrated which protect against overvoltage and overload conditions. During the installation phase the system will be operated without active cooling. As a result, the regulator needs to startup reliably even with supply currents which are much smaller than the currents reached under nominal working conditions. Therefor a configuration circuit has been developed capable to change the regulator offset voltage which is reached at small input currents. An AC coupled square wave signal is rectified and used as a control signal to change the offset voltage between two values. One value is close to the regulator output voltage for operation with small supply currents and the other value is smaller than the output voltage for efficient operation with large supply currents. For the same reason a startup circuit has been introduced which increases the regulator input impedance and in turn supports the startup procedure. A set of three successive test chips have been produced and tested to validate the proper operation of the circuitry. The

newly introduced Shunt-LDO regulator features will be presented together with simulation and measurement results of the produced prototypes.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power, Grounding and Shielding

Contribution ID: **150**   Type: **Poster**

A 32-channel 1-10 GSa/s Flexible Waveform Recording System using the PSEC4A ASIC

Thursday, September 5, 2019 4:55 PM (20 minutes)

We present a 32-channel data acquisition system using the PSEC4A chip and initial applications as a readout system for neutron detectors at Sandia's Z Pulsed-Power Facility. The PSEC4A is an 8-channel, 10 GSa/s waveform recording ASIC with an analog bandwidth of 1.9 GHz, which also incorporates multi-event buffering to reduce latency induced by close-in-time triggers. In the 32-channel system, four PSEC4As are time synchronized using a common clock delivered from a PLL chip. Triggering can be done using the internal PSEC4A discriminators or via an external input. An optical serial communication link serves as the user interface to the board.

Summary

The PSEC4A ASIC, as reported at TWEPP-18, was designed and fabricated in 2017 as an upgrade to the PSEC4 waveform sampling chip. The PSEC4 offers 10 GSa/s sampling rates, self-triggering, and high bandwidth, but its scope is limited due to a short 256-sample recording length on each channel. To address this issue, PSEC4A combines the PSEC4 digital circuitry with a new analog design, which allows a larger recording window as well as the option for multi-event partitioning of the analog buffer, while keeping high analog bandwidth.

The 32-channel board uses four 8-channel PSEC4A ASICs, with each channel fed from a high-density Samtec (SEAF8) board-to-board connector that mates to the sensor board. The four PSEC4As are synchronized to the same clock through a PLL/jitter-cleaner chip, which may be referenced to an on-board oscillator or an external clock input. The system uses a low-cost Cyclone-V FPGA for system control and data management. To enable operation in the high-EMI environment at the Sandia Z Pulser-Power Facility, the board requires significant shielding and an isolated user interface over optical fiber. The PSEC4A board is designed to a compact size of 70mm by 106mm.

The sensor board is composed of an array of fast scintillator/SiPM detectors. The detector array is designed to measure the total flux and arrival time of 2.45 MeV fusion neutrons produced by deuterium-deuterium interactions in a high temperature plasma. The system can be used in either a particle counting mode for low fluence or in current mode for high fluence. The system response will be measured using a neutron calibration end station at Sandia's Ion Beam Laboratory (IBL). This calibration facility uses the IBL's 300-keV Cockroft-Walton generator to accelerate D+ ions to 175 keV, producing approximately 2.7 µA of beam current onto a 2.5-µm thick ErD2 target. The PSEC4A/SiPM system response will be compared with a standard scintillator/MCP-Photomultiplier/transient-digitizer neutron diagnostic. The PSEC4A system is being constructed for use as a compact and modular neutron time-of-flight (nTOF) spectrometer for Magneto Inertial Fusion (MIF) experiments.

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Presenter: PORTER, John (Sandia National Laboratories)

Session Classification: Posters

Track Classification: ASIC

Contribution ID: **151**   Type: **Poster**

RD53A chip susceptibility to electromagnetic conducted noise

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The RD53A read-out chip (65 nm CMOS) is a large-scale demonstrator for ATLAS and CMS phase 2 pixel upgrades. It is one of the key elements of the serial powering scheme for the next generation of pixel detectors. The susceptibility of the RD53A chip with respect to external EM noise has an impact on the integration strategies (grounding and shielding schemes) and operating conditions of future Pixel detectors. This paper presents a detailed analysis of the RD53A chip susceptibility to RF conducted disturbances in order to understand and address noise issues of RD53A Chip before the pixel upgrade installation.

Summary

The extreme high rate operation of the ROC at the HL-LHC requires the use of 65nm high density low power CMOS technology with low working voltage (1.2V), resulting in a pixel chip that must be supplied with significant current levels (~2A per chip). During the last years, extensive studies have shown that a serial power distribution system is the only feasible scheme to supply the pixel detector with the required power within an acceptable material budget and power cable losses.

From the point of view of electromagnetic interferences (EMI), there are no precedents of this type of powering scheme on a high energy physics detector. In a serial powering scheme, each power group has several modules connected in series and fed with constant current. From the Grounding/EMC point of view this topology is characterized by having only one module connected to the system ground, and the rest floating at different potential levels. In order to avoid EMI problems and define a good grounding strategy, it is important to quantify the noise sensitivity of RD53A chip against EM conducted noise. For that purpose, noise currents at different frequencies are injected with current probes through the power lines of the RD53A chip (both low and high voltage), and then the equivalent noise charge (ENC) per channel is measured. The ratio between the measured noise and the perturbing injected current is used to compute the transfer function of RD53A chip against EM conducted noise.

This paper shows the first part of the EMC studies of RD53 chip to identify potential noise issues and critical elements. EMC tests have been performed using Single chip cards (SCC) prototypes based on RD53A in order to analyze chip configuration, and component level implications (input/output filter characteristics). Several topologies and options have been tested: SCC with and without sensor, analog front-ends (Synchronous, Linear and Differential) and powering conditions, LDO mode (powered in voltage) and Shunt-LDO mode (powered in current). This set of tests will be used on future stages (serial power chain based on SCC and HDI EMC tests) as a reference to quantify the effects of integration strategies on the susceptibility of pixel detector against EM noise.

This is the first time that this kind of tests and analysis has been performed in a readout chip prior to its final integration. The outcomes of this study will allow understanding the coupling mechanisms of electromagnetic noise associated to read-out chip. The resulting susceptibility profiles provide emission requirements for noise sources in the experiment, as well as grounding and shielding guidelines for CMS pixel phase II. This information will help system integration designers to enhance the robustness of the pixel system, and therefore its integration in the whole experiment.

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Session Classification: Posters

Track Classification: Power, Grounding and Shielding

Contribution ID: **152**   Type: **Poster**

ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS

Tuesday, September 3, 2019 5:20 PM (20 minutes)

ALTIROC2 is an ASIC designed to readout a pixel matrix of 15 x 15 Low Gain Avalanche Diodes (LGAD) for the High-Granularity Timing Detector in ATLAS. It measures the TOT and TOA with a resolution of tens of ps for each detected hit. Data are temporally stored in a buffer able to cope with latencies up to 35µs. The ASIC also measures the luminosity of each bunch crossing with two different time windows. Timing and luminosity data are transmitted through two high speed e-links at different rates, depending on the radial position of the ASIC in the detector.

Summary

The increase of pileup will be one of the main challenges in the High-Luminosity LHC. A way to mitigate the effects of the pileup is the use high precision timing information to distinguish between collisions very close in space but well separated in time. A High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase II Upgrade. The detector will be made of hybrid pixels based on Low Gain Avalanche Diode (LGAD) technology.

ALTIROC2 is an ASIC designed to readout modules of 15 x 15 pixels of 1.3 x 1.3 mm2. Each pixel includes an analog front end stage composed of preamplifier, discriminator with a 4-bits DAC to fine tune the threshold level, and two Time to Digital Converters (TDC). The latter will provide the Time Of Arrival (TOA) and the Time Over Threshold (TOT) with a precision of 20 ps. The on-pixel digital electronics include a buffer to store temporally the data generated in each bunch crossing and able to cope with latencies up to 35µs, and a windowing circuit to measure the luminosity. They perform zero-suppression and keep the data on pixel are readout by the electronics on the periphery.

ALTIROC2 receives 8-bits fast commands from the central Trigger Data Acquisition system (TDAQ). This also sources a 320 MHz clock signal, from which an internal 40 MHz clock is generated. Based on this, a phase-locked loop (PLL) produce all the different internal clocks needed to operate the ASIC. A phase shifter aligns the phase of all internal clocks with an accuracy of 100 ps.

The fast commands are processed by a control unit that handles the readout of the pixel matrix. It includes a 12-bits bunch crossing counter to generate a bunch crossing identifier (BCID) and a trigger table to store trigger events. When an L0/L1 accept command is received by the ASIC, the control unit generates an internal trigger signal and a trigger identifier (TrigID) and then they are passed to all the pixels. The TrigID stored with the corresponding BCID in the table. Upon receiving the trigger signal, the control unit retrieves and store the data from the pixels related to the trigger bunch crossing. Then the data are moved into the Hit Data Formatting module, where they are packed in frames, serialised and transmitted to the peripheral on-detector electronics through e-links. The transmission speed of the e-link will depend on the radial position of the ASIC, and will be set via and Inter-Integrated Circuit bus I2C to one of three values: 320 Mb/s, 640 Mb/s and 1.28 Gb/s. The I2C is also used to configure the ASIC.

Another function of ALTIROC2 is to measure the luminosity of each bunch crossing. It sums the 225 luminosity outputs, hit or not, over two time windows of different length centred on the bunch crossing. Both sums are processed and the transferred to the luminosity serializer where are packed in frames and transmitted at 640 MHz through an e-link.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **153**   Type: **Poster**

EureKA-Maru: an ATCA board for the CMS Phase 2 Tracker Upgrade with centralized slow control and board management solution based on a Zynq Ultrascale+ System-on-Chip

Tuesday, September 3, 2019 5:20 PM (20 minutes)

The Phase-2 CMS tracker back-end processing system is composed by two types of Detector, Trigger, and Control (DTC) boards interfacing the inner and outer tracker, and by the Track Finding Processor (TFP) board performing level-1 track reconstruction from the outer tracker data. Several groups are building hardware to prove key and novel technologies needed in the back-end processing system. EureKA-Maru is designed to contribute to the pool of alternatives a design with an improved thermal performance of the optical transceivers as well as an integrated management solution based on a Zynq Ultrascale+ (US+) System-on-Chip (SoC) device.

Summary

The Phase-2 CMS tracker back-end processing system is composed by two types of "Detector, Trigger and Control" (DTC) boards interfacing the inner and outer tracker, and by the "Track Finding Processor" (TFP) board performing level-1 track reconstruction from the outer tracker data. Several groups are building ATCA hardware to prove key and novel technologies needed in the back-end processing system. EureKA-Maru is designed to contribute to the pool of alternatives. The design improves the thermal performance of the optical transceivers as well as integrates a centralized management solution based on a Zynq Ultrascale+ (US+) System-on-Chip (SoC) device.

EureKA-Maru is designed around a single Virtex US+ FPGA with up to 128 high-speed transceivers, each with a line rate of up to 25 Gb/s. 120 high-speed lanes are connected to Samtec Firefly optical transceivers; four are used for the DAQ path and the remaining four for slow-control and management tasks. The placement of components has been done with the primary purpose of keeping the thermally sensitive optical transceivers with the best cooling possible. The placement also allows a single cable length for all transceivers, therefore, minimizing the bulk cost of Firefly components thereby also reducing the number of spare variants.

The design explores the idea of using an integrated solution for board management and slow control having a plug-in module with a Zynq US+ SoC. The management module provides FPGA logic, high-performance ARM-A53 multi-core processors and two ARM-R5 real-time capable processors. The ARM-R5 cores are used to implement the IPMI/IPMC functionality and communicate via backplane with the shelf manager at power-up. The ARM-R5 are also connected to the power supply (via PMBus), to voltage and current monitors, to clock generators and jitter cleaners (via I2C, SPI). Once full power is enabled from the crate, a Linux starts on the ARM-A53 cores. The FPGA on the management module is used to implement the low-level interfaces including IPBus, or glue-logic. The SoC is the central entry point to the Virtex Ultrascale+ FPGA on the motherboard via IPMB and TCP/IP based network interfaces. The communication between the Zynq US+ SoC and the Virtex Ultrascale+ uses the AXI chip-to-chip protocol via MGT pairs keeping infrastructure requirements in the main FPGA to a minimum.

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Presenter: ARDILA, Luis (KIT-IPE)

Session Classification: Posters

Track Classification: Trigger

Contribution ID: **155**   Type: **Oral**

Highly-linear FPGA-based Data Acquisition System for Multi-channel SiPM Readout

Thursday, September 5, 2019 11:55 AM (25 minutes)

A 32 channel, 15ps resolution, Kintex 7 FPGA-based TDC DAQ for time-of-flight and time-over-threshold measurement is demonstrated along with a comparison to previous works. Results include 11ps mean bin size, less than 4ps differential nonlinearity, and less than 10ps of integral nonlinearity. Linearity is improved by multichain averaging with comparison of 1, 2, and 4 chains pre and post-calibration. Implementation difficulties including bubble error, zero length bins, inter-clock region nonlinearity, calibration, chain overflow are discussed with focus on modern FPGA concerns including clock skew and bin realignment. Measurement methods are reviewed as well as a comparison of common TDC methods.

Summary

Use of high linearity, high resolution, multi-channel, data acquisition (DAQ) systems for readout of highly sensitive silicon photomultipliers (SiPMs) is required for many high-energy physics experiments. SiPMs offer distinct advantages compared to photomultiplier tubes (PMTs) including insensitivity to magnetic fields, very fast response, low bias voltage, and miniaturization. FPGA advancements continue to shorten the gap between application specific integrated circuits (ASICs) and FPGA-based TDC performance for use in DAQs. Although FPGAs are limited to predefined fabric structure and architecture, use of linearization improvement techniques including wave union and multi-chain averaging are more easily implemented due to an abundance of carry chains and digital signal processing blocks. Common implementation difficulties have plagued FPGA-based TDCs since the 1990s including bubble error within the thermometer-to-binary encoder, inter-clock region nonlinearity, and calibration. Modern FPGAs exhibit new challenges due to advancements in fabric speed which shorten the difference between gate delay and path delay causing clock skew. As the gate delay of a common carry chain is reduced, small differences in the arrival time of a global clock to each tapped delay register causes a disparity between bin sizes often resulting in zero length bins. The solution is bin realignment and careful selection of a bubble correcting thermometer-to-binary encoder. Within this paper, implementation of a 32 channel, 15ps TDC using a Xilinx Kintex 7 FPGA will be reviewed along with an examination of each difficulty.

First, the standard code density characterization method will be explained along with a description of common TDC methods including advantages and disadvantages. Next, a basic time-of-flight TDC design will be reviewed with an evaluation of the code density histogram outlining each nonlinearity. The cause of each nonlinearity will be addressed with a specific change to the original design including explanation and reasoning. The final design includes a pipeline enabled pulse detector reducing front-end zero bins, a double buffered latching stage for metastability improvement, a fast thermometer-to-binary encoder tailored to handle bin realignment and increase clock speed, and a set of four parallel chains used for multi-chain averaging with focus on linearity improvement. Calibration is accomplished by the code density method using an onboard asynchronous clock fed to each input and storing the known bin lengths into block ram for use on subsequent runs. Use of a multiplexing technique to increase energy measurement channel count is proposed along with a final detailed DAQ design including snapshots of the Xilinx Vivado block design with onboard Microblaze processor. The final design including 32 channels, 15ps of RMS resolution, 11ps mean bin size, less than 4s differential nonlinearity, and less than 10ps of integral nonlinearity is compared to 12 previous publications with this work's linearity superior

to all previous designs.

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Presenter: TOWNSEND , Todd (University of Houston)

Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

Contribution ID: 156   Type: **Poster**

A SiPM Readout Front-end with Fast Pulse Generation and Successive-Approximation Register ADC

Tuesday, September 3, 2019 5:20 PM (20 minutes)

A low-power front-end with on-chip fast pulse generation and customized SAR ADC is developed for SiPM readout design. The on-chip fast pulse generation improves the timing resolution without the need of extra I/O pins. The proposed SAR ADC, reusing the SiPM charge integrator and eliminating the power-hungry charging sensing amplifier, consumes significantly less power compared with conventional solutions. The front-end is designed in a 0.18 μm CMOS technology, achieving a SNDR of 57.53 dB and consumes 3.8 mW of power. The HPF reduces the long-tailed SPE pulse width from 50 ns to 3 ns.

Summary

ASICs for silicon photomultiplier (SiPM) readout with high timing resolution and low power consumption is required for high-energy physics experiments. However, the large quenching RC time constant of SiPM cause a much longer tail in the single photo-electron (SPE) response. As the output pulse of SiPM is formed by superposition of hundreds of SPE responses from triggered microcells, the current pulse is therefore shaped with a slow rising edge. The slow rising edge of the current pulse makes the timing measurement to be sensitive to the noise of the readout electronics. To address the issue, SensL has developed a modification to the standard SiPM structure that results in a third terminal carrying an ultra-fast output signal. In the modified structure, by adding a small capacitor in parallel with the quenching resistor in each microcell, a high-frequency output path is established from the standard path. Nevertheless, the drawback of the SensL's approach is obvious. As both the fast and standard outputs are required, the input pin counts of the readout ASIC is doubled, which results in a costly and cumbersome design, especially for applications where thousands of SiPM detectors and readout circuitries are needed.

In terms of energy measurement, the conventional SiPM readout ASIC often utilizes a power-hungry charge sensitive amplifier (CSA) to integrate the scaled current onto an integration capacitor, and a low speed Wilkinson ADC is then employed to digitize the CSA output voltage. Such an approach unfortunately suffers from high power consumption. The high power dissipation also inevitably leads to a high working temperature, which can cause SiPMs to generate more dark count noises, deteriorating the timing and energy measurement accuracies. Low-power SiPM readout ASIC is required, especially for systems with a large amount of SiPM detector arrays.

In this paper, we report a 16-channel SiPM readout with high timing resolution, low I/O pin counts and low power consumption. An on-chip high-pass filtering approach is adopted to generate the fast current pulse from the standard output of SiPM without the need of extra I/O pins. The fast current pulse significantly helps to improve the timing measurement accuracy. To achieve low power consumption, a customized SAR ADC directly digitizes the output voltage of the charge integrator in each channel by reusing the charge integration capacitor as the sampling capacitor of the ADC. Besides, benefiting from the high sampling rate of the SAR ADC, the 16 SiPM readout channels can share one single SAR ADC for energy digitization, which offers a compact design and lowers the power consumption of the readout ASIC. Designed in a 0.18 μm 1P6M CMOS process, each channel of the readout consumes 3.8 mW of power. The on-chip HPF shortens the long-tailed SPE

pulse width from 50 ns to 3 ns. At 16 MS/s, the SAR ADC consumes 743 µW from a 1.8 V supply, and provides a SNDR of 57.53 dB and a SFDR of 66.31 dB.

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Presenter: TANG , Yuxuan (University of Houston)

Session Classification: Posters

Track Classification: ASIC

Contribution ID: **157**   Type: **Poster**

A 60μm2 HV-CMOS pixel with 0.5 ns timing resolution and 28 μW power consumption for high-density arrays

Thursday, September 5, 2019 4:55 PM (20 minutes)

High Voltage-CMOS (HV-CMOS) sensors are the sensor technology of choice for the pixel tracker in the Mu3e experiment at PSI in Switzerland. In this contribution, timing resolution down to 0.5 ns is obtained. Simultaneously, power consumption is held below 28 μW in a pixel size of 60 μm2, enabling 4D tracking in a high-density array. Timing errors due to signal amplitude variations considered special attention to improve time resolution.

Summary

HV-CMOS technology was developed some years ago. Large arrays of these pixels are being developed as a prove that this technology can be used in several High-Energy Physics experiments [1]. In this step, it is important to reduce both, the timing uncertainty in detecting particle arrival, and power consumption. In this paper, a HV-CMOS pixel was designed in the 150 nm process of LFoundry to increase timing accuracy. It was integrated in only 60 μm2, consuming just 28μW. Hence, 4D tracking is habilitated with this pixelated technology.

The analog readout integrated in-pixel consists of a sensor bias circuit, a Charge Sensitive Amplifier (CSA), a single folded cascode amplifier, a source-follower and a comparator with a 4-bit DAC for offset compensation. To reduce the time walk, the pixel includes an analog buffer, a delay chain and 5 analog memories needed to sample the rising edge of the pre-amplified signal. The analog sampling permits to perform a linear fit over the sampled voltages and to find the time-of-arrival of the particle. These data allow to correct the time walk off-line and to extract the energy information of the detected particle.

The time of the arrival of the particle is digitally added with a time-stamp (TS) running at frequencies from 40 MHz to 200 MHz. To increase timing resolution, a programmable Time-to-digital converter (TDC) common to the whole pixel array is included in the chip. The coarse phase of the TDC is the Least Significant Bit (LSB) of the TS. The fine phases of the TDC are generated through delays implemented by a chain of buffers. The fine TDC generates 5 phases equally delayed from the TS clock with configurable delays from 0.5 ns to 2 ns. Moreover, each phase has the same rise and fall time. The hit time is defined by the values of the TS and the 5 fine phases. Timing corrections of the hit time of the particle are performed off-line as well.

Compared to similar pixel area detectors, simulations show that the time walk is reduced down to 4.1 ns with a power consumption of 28 μW per pixel, and a maximum timing resolution of 0.5 ns. An ASIC including the presented pixel was sent to fabrication.

[1] I. Perić et al., "Overview of HVCMOS pixel sensors,"J. Instrum., vol. 10, no. 5, 2015.

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Session Classification: Posters

Track Classification: ASIC

Contribution ID: **158**   Type: **Oral**

Continuous Integration of FPGA Designs and Automation of the Development Environment

Tuesday, September 3, 2019 2:25 PM (25 minutes)

The high degree of flexibility in the firmware development makes FPGA designs and the development environment vulnerable to errors. Continuous integration is a fast way to detect a majority of such errors. Additionally, simulations and hardware tests can be automated using test methodologies (e.g. unit test). Continuous integration offers the benefits of reproducible results, fast error detection, error tracing, avoiding human errors in the build process, and minimizing the manual verification of the firmware. This comes at the price of setting it up with comprehensive integration tools such as GitLab. We present such an integration flow within the CMS experiment.

Summary

Especially FPGA designs with multiple contributors require comprehensive verification and testing. This process starts with the build environment and ends with the deployment of the firmware (FW). Therefore, Continuous Integration (CI) offers an automated way to set up, build, verify, control, monitor, and deploy the FPGA implementation. CI is widely used and successful in software development. CI is based on uniform build, simulation, and test environments and ensures a correct build of the FPGA design. Additionally, it covers essential functionalities of specified simulations and tests. Human errors in the build process are eliminated, e.g. missing files, wrong tool version, changed global constants, wrong submodule commit. Another main benefit is that the manual verification of the FW can be minimized, especially if different FPGAs and/or configurations are supported.

CI requires a version control system such as git, which is the baseline for most source code projects. In order to seamlessly set up the CI, a Command Line Interface (CLI) for FW builds is recommended. In this talk, we will introduce such CLI tools and present our choice. In our case, we extended the CLI tool by the feature of Xilinx Vivado simulation.

We use a CI system based on GitLab Continuous Integration / Continuous Deployment (CI/CD). We are presenting other CI tools as well and show how to integrate GitHub in the GitLab CI/CD. We show different aspects of CI in the example of the Track Stand-Alone (TSA) object FPGA board in the level 1 correlator. We elaborate on stages, jobs, pipelines, and runners of the CI. In this project, we set up several Hardware Description Language (HDL) simulations, which are performed in parallel, and evaluate their results. Only if this simulation stage is performed successfully the synthesis stage will be triggered.

We are sharing our experience with CI for FPGA designs and discuss tip and tricks as well as potential issues. Furthermore, we show the integration of High-Level Synthesis (HLS) designs and talk about the possibilists of extending CI.

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Session Classification: ASIC

Track Classification: ASIC

Contribution ID: **159**   Type: **not specified**

TUTORIAL: Design of Analog Circuits in Nanoscale CMOS

Monday, September 2, 2019 9:00 AM (3 hours)

Presenter: MURMANN, Boris

Session Classification: Tutorial

Contribution ID: **160**
Type: **not specified**

Welcome 1

Monday, September 2, 2019 2:20 PM (20 minutes)

Presenter: MARCHIORO, Alessandro (CERN)

Session Classification: Welcome

Contribution ID: **161**   Type: **not specified**

Welcome 3

Monday, September 2, 2019 3:10 PM (15 minutes)

Presenter: VAZQUEZ, Pablo (Universidade de Santiago de Compostela (ES))

Session Classification: Welcome

Contribution ID: **162**   Type: **Oral**

Technology development of CMOS Image sensors

After a basic review of the working principles of CMOS image sensor (pinned photodiode device), the main technologies and process modules (such as Back-Side Illumination, integrated lightguides and anti-reflective coatings, buried light shields, hybrid bonding) used in the manufacturing of CMOS Image Sensors (CIS) will be described, focusing on their correlation with the performance of pixel array. The impact of metal contamination in manufacturing line in terms of photodiode dark current will be also briefly covered.

Summary

Presenter: DEL MONTE, Andrea (LFoundry)

Session Classification: Invited

Contribution ID: **163**
Type: **Oral**

Future Prospects of Particle Physics

Tuesday, September 3, 2019 10:45 AM (45 minutes)

An overview will be given where we stand with the fundamental questions in particle physics today, and how we
plan to answer these in future with new projects world-wide, either already planned ones or those still under discussion.
The ongoing European Particle Physics Strategy Update process is currently evaluating possible future programs and their physics merits.
This general seminar will show several highlights from the most prominent future projects proposed for both the so called high
energy and high intensity frontier. We'll look in some detail to the physics questions that these projects will be able to address.
Some of the anticipated new technical challenges will be discussed as well.

Summary

Presenter: DE ROECK, Albert (CERN)

Session Classification: Invited

Contribution ID: **164**   Type: **Oral**

High-speed design : how to successfully address the high speed challenges : 25Gbps and over

Wednesday, September 4, 2019 10:45 AM (45 minutes)

Today communication protocols (32Gbps PCIE Gen5, 112Gbs PAM4, …) and FPGAs transceivers speeds are pushing
designer to hardware designs constraints, PCB material choice and layout constraints that where almost never considered years ago.
This presentation is an extract of a CCES technical training, and its purpose is to cover some of the theorical aspects of "high speed",
as well as some tricks and traps to be successfull in those coming designs.

Summary

Presenter: CAPITAN, Jean-Michel (Hardware Expert, CCES)

Session Classification: Invited

Contribution ID: **166**　　　　　　　　　　　　　　　　　　　　　　　　　Type: **Oral**

Using advanced SoCs at the CERN experiments and accelerator

Tuesday, September 3, 2019 3:45 PM (45 minutes)

Recent hardware developments in the experiments and the accelerators, especially for the detector readout electronics for the High-Luminosity LHC, are using FPGAs with embedded processors (SoCs).

This is very popular with HW developers due to the close integration between the computing element running a unix operating system and the programmable logic part of the FPGA. For the HL-LHC, there will be of order two to four thousand such devices across CERN experiments (mainly ATLAS and CMS), posing a number of questions about networking, security, operating system support, scalability of the infrastructures and maintainability. The use cases and the integration aspects were discussed at a workshop held at CERN mid-June 2019.

This talk gives a brief summary of the workshop, the use cases, and the thrust at CERN to find common solutions to the integration aspects and long term support for these types of devices in the experiments and more generally across CERN.

Presenter:　DOBSON, Marc (CERN)

Session Classification:　Invited

Contribution ID: **167**   Type: **Oral**

Designing advanced SoCs in technologies down to 28nm CMOS: challenges and solutions.

Wednesday, September 4, 2019 3:45 PM (45 minutes)

Sub 65-nm technologies can offer to engineers huge advantages for the design of high-density and low power circuits and for the integration of high complexity System-on-Chips. Transistors and gates are almost free for the creative designer, but yet their correct integration requires an exponentially increasing investment in tools and training, and a totally new approach to verification, all the way from the high level system validation to the low-level physical and manufacturing verification. New challenges appear along the design process and have to be consistently addressed by designers and project managers.

First the direct challenges, strongly linked to the technology itself, which are mainly affecting both analog and digital backend flows in multiple aspects: floor-planning, routing, sign-off, power estimation and area reduction. To further complicate this picture, many of these aspects are also subtly intertwined and require often difficult system level decision.

In addition, there are indirect challenges induced by "more than Moore"technologies (e.g. mixed-signal integration and verification), and higher SoC complexity requiring novel functional verification and prototyping methodologies.

This talk will cover in more detail these challenges, focusing mainly around a 28nm technology and will present some of the solutions available to the IC design community. We will also suggest the adoption of some of the most robust design methodology based on existing CAE tools.

Presenter: CAUSSETTE, Sebastien (Cadence)

Session Classification: Invited

Contribution ID: **168**　　　　　　　　　　　　　　　　　　　　　　　Type: **Oral**

Particle detection and imaging using the Medipix and Timepix ASICS: design, challenges and applications

Friday, September 6, 2019 10:45 AM (45 minutes)

September 2019 marks 20 years since the signature of the Medipix2 Collaboration agreement. Since then 3 generations of pixel detector readout chips have been or are being developed: Medipix2 and Timepix (with recently the addition of Timepix2), Medipix3 and Timepix3 and finally Medipix4 and Timepix4. The Medipix chips have sought to provide high-rate spectroscopic photon counting with hit-by-hit on-pixel energy binning. The Timepix chips, on the other hand, aim to transmit as much hit information as possible off-chip (pixel coordinates, arrival time, time-over threshold). The chip architectures and some of the design choices made will be described. Of course, in spite of our best efforts, we have faced and overcome significant technical challenges over the years and some of these will be discussed. Finally, a large number of applications –both foreseen and unforeseen, within and beyond high energy physics –have been addressed and a selection of those will be described.

Presenter:　CAMPBELL, Michael (CERN)

Session Classification:　Invited

Contribution ID: **169**   Type: **not specified**

Welcome

Wednesday, September 4, 2019 4:30 PM (5 minutes)

Author: KLOUKINAS, Kostas (CERN)

Presenter: KLOUKINAS, Kostas (CERN)

Session Classification: Working groups

Contribution ID: **170**　　　　　　　　　　　　　　　　　Type: **not specified**

CHIPS: CERN-HEP IC design Platform and Services

Wednesday, September 4, 2019 4:35 PM (20 minutes)

Author:　KLOUKINAS, Kostas (CERN)

Presenter:　KLOUKINAS, Kostas (CERN)

Session Classification:　Working groups

Contribution ID: 171   Type: **not specified**

EUROPRACTICE EDA Tools for the HEP Community

Wednesday, September 4, 2019 4:55 PM (25 minutes)

Author: Dr MCLEAN, John

Presenter: Dr MCLEAN, John

Session Classification: Working groups

Contribution ID: **172**

Type: **not specified**

CERN ASIC support News & Radiation Tolerant device models for 65nm technology

Wednesday, September 4, 2019 5:20 PM (20 minutes)

Author: CARATELLI, Alessandro (EPFL, CERN)

Presenter: CARATELLI, Alessandro (EPFL, CERN)

Session Classification: Working groups

Contribution ID: **173**   Type: **not specified**

Library Characterization techniques

Wednesday, September 4, 2019 5:40 PM (30 minutes)

Author: BARBE, Maxime (Cadence VCAD)

Presenter: BARBE, Maxime (Cadence VCAD)

Session Classification: Working groups

Contribution ID: **174**   Type: **Oral**

LASP Test Board cooling simulations - first approach

Wednesday, September 4, 2019 4:30 PM (30 minutes)

Presenter: CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR))

Session Classification: Working groups

Contribution ID: **175**   Type: **Oral**

Thermal study and optimisation of an ATCA card for the Phase-2 Upgrade of LHC experiments

Wednesday, September 4, 2019 5:00 PM (30 minutes)

Presenter: ILES, Gregory Michiel (Imperial College (GB))

Session Classification: Working groups

Contribution ID: **176**   Type: **Oral**

Thermal Design and Test of gFEX

Wednesday, September 4, 2019 5:30 PM (30 minutes)

Presenter: CHEN, Kai (Brookhaven National Laboratory (US))

Session Classification: Working groups

Contribution ID: **177**

Type: **Oral**

Radiation Physics Lab: A TID test installation at USC

Monday, September 2, 2019 3:25 PM (40 minutes)

Radiation Physics Laboratory (http://www.usc.es/rpl) is an accredited Secondary Standard Dosimetry Lab in the University of Santiago with more than 10 years of experience on photon and electron TID experiments. Currently the laboratory has a high dose rate 60-Co unit together with an electron linal able to produce 6 MV and 15 MV photon beam qualities and electron beams with 6, 9, 12, 16 and 20 MeV energy. Dose rates at 1 m from focus have a range between 1 Gy/min to 10 Gy/min. The lab works mainly for the aerospace insdustry in the test of components and systems from earth orbit to deep space missions. Additionally at 15 MV photon mode we are able to produce photonuclear neutrons through evaporation process with primary energies around 1 MeV. During the presentation will discuss the conditions to ensure a proper dosimetry evaluation in the irradiation tests.

Authors: PAZOS ALVAREZ, Antonio (Universidade de Santiago de Compostela (ES)); GONZALEZ DIAZ, Diego (Universidade de Santiago de Compostela (ES)); GOMEZ, Faustino (Universidad de Santiago de Compostela); GÓMEZ, Nicolás

Presenter: GOMEZ, Faustino (Universidad de Santiago de Compostela)

Session Classification: Invited

Contribution ID: **178**   Type: **Oral**

Focal plane processing in standard CMOS technologies

Monday, September 2, 2019 4:05 PM (40 minutes)

The new paradigm of Analog to Information Conversion (AIC) aims at extracting information from the environment rather than simply massive amounts of raw data. Focal plane processing is a way of doing so by means of processing the sensed data at the acquisition stage, efficiently reducing bandwidth and power consumption. The use of standard CMOS technologies favours the development of low cost solutions.

Author: LÓPEZ MARTÍNEZ, Paula (University of Santiago de Compostela (ES))

Presenter: LÓPEZ MARTÍNEZ, Paula (University of Santiago de Compostela (ES))

Session Classification: Invited

Contribution ID: **179**									Type: **Oral**

Time Resolution of Large Area Low Light Level Sensors

Monday, September 2, 2019 5:05 PM (40 minutes)

Large area photo-detectors with time resolution of the order of 10 ps for low lights levels, down to the single photon, would bring a revolution in many fields. In medical imaging would enable real time PET, in LIDAR would make possible achieving millimetric spatial resolution requiring no averaging and would have a strong impact in other fields as fluorescence imaging and, of course, in high luminosity experiments in particle physics. Although some Microchannel plate photomultipliers (MCP - PMT) may approximate this performance, a solid-state sensor is often preferred. Silicon Photomultipliers (SiPMs) have been able to replace PMTs in many applications as they have significant advantages in some key aspects: higher Photo Detection Efficiency, robustness and insensitivity to magnetic fields. However, application of SiPMs in large area and fast detectors is an open question as the detector capacitance severely degrades performances: lower signal to noise ratio, worse timing resolution, wider pulse shape and therefore higher pile-up. Neither analog nor digital large area SiPMs achieve a Single Photon Time Resolution below 100 ps. We will discuss how detector segmentation can help in this direction and we will present different techniques, ranging from Application Specific Circuits (ASICs) to a proposal for new generation of hybrid photosensors.

Author: GASCON, David (University of Barcelona (ES))

Presenter: GASCON, David (University of Barcelona (ES))

Session Classification: Invited

Contribution ID: **180**   Type: **Oral**

The lonely perpetrator in the DCDC FEAST2 case: how an individual transistor threatened the operation of the CMS pixel detector

Thursday, September 5, 2019 3:45 PM (45 minutes)

The failure of a first DCDC converter in the power distribution network of the CMS pixel detector system on October 5th, 2017, might have been due to a single failure and did not raise particular concern. However, it was soon followed by a steady rate of failures of DCDCs in random positions in the detector. Projections of this rate to the future led to an ominous scenario where, without resolving interventions, the 2018 data taking would be jeopardised. This talk will report the evolution of the long investigation aimed at uncovering the origin of the problem, to propose temporary patches for the 2018 run and, eventually, a cure to achieve long-term functionality of the power distribution system.

Author: FACCIO, Federico (CERN)

Presenter: FACCIO, Federico (CERN)

Session Classification: Invited

Contribution ID: **181**   Type: **not specified**

Opening act

Monday, September 2, 2019 2:00 PM (20 minutes)

Presenter: KLUGE, Alex (CERN)

Session Classification: Welcome

Contribution ID: **182**   Type: **not specified**

Welcome 2

Monday, September 2, 2019 2:40 PM (30 minutes)

Presenter: GALLAS TORREIRA, Abraham Antonio (Universidade de Santiago de Compostela (ES))

Session Classification: Welcome

Contribution ID: **183** Type: **Oral**

Closing

Friday, September 6, 2019 11:55 AM (20 minutes)

Presenter: KLUGE, Alex (CERN)

Session Classification: Closure