TWEPP 2019 Topical Workshop on Electronics for Particle Physics

Tuesday 3 September 2019

Posters (17:20 - 18:50)

time	[id] title	presenter
17:20	[80] CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade	CMS COLLABORATION, CMS collaboration GEVIN, Olivier
17:20	[156] A SiPM Readout Front-end with Fast Pulse Generation and Successive-Approximation Register ADC	TANG , Yuxuan
17:20	[153] EureKA-Maru: an ATCA board for the CMS Phase 2 Tracker Upgrade with centralized slow control and board management solution based on a Zynq Ultrascale+ System-on-Chip	ARDILA, Luis
17:20	[152] ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS	CASANOVA MOHR, Raimon
17:20	[151] RD53A chip susceptibility to electromagnetic conducted noise	PRADAS LUENGO, Alvaro
17:20	[148] Qualification of the final LHCb VELO electronics	Dr LEMOS CID, Edgar
17:20	[145] The VRP - a Versatile Readout Platform for the nuclear experiments at HIRFL-CSR	Prof. ZHAO, Chengxin
17:20	[144] Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector	ROBLES MANZANO, Maria
17:20	[143] A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePlx4	CASANOVA MOHR, Raimon
17:20	[141] The first ASIC prototype of a 28 nm time-space front-end electronics for real-time tracking	Mr PICCOLO, Lorenzo
17:20	[139] Overview of Electronics Developed by ISE for the European Spallation Source Project	Mr RUTKOWSKI, Igor
17:20	[133] The Firmware for the European Spallation Source Cavity Simulator	GRZEGRZÓŁKA, Maciek
17:20	[122] Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs	CARATELLI, Alessandro
17:20	[120] 20 Mrad-TID Effects on Time over Threshold performance of GEMINI chip	MANGIAGALLI, Luca
17:20	[118] Triple-Modular Redundancy Deployment Optimization in the Sensor Readout System of the CBM Micro Vertex Detector	ZHAO, Yue
17:20	[107] A Monolithic Active Pixel Sensor for CEPC vertex detector	Mr WU, Tianya
17:20	[102] FAST: a front-end readout ASIC for a 30 ps time resolution with 6 pF UFSD sensors	Dr FAUSTI, Federico
17:20	[97] Upgrade of the ATLAS TileCal High Voltage system	DA SILVA GOMES, Agostinho
17:20	[95] Readiness of the ATLAS Tile Calorimeter link daughterboard for the High Luminosity LHC era	VALDES SANTURIO, Eduardo
17:20	[93] Design of Finite State Machines for SRAM-based FPGAs operated in radiation field	LUPI, Matteo
17:20	[92] LpGBT Tester: an FPGA based test system for the lpGBT ASIC	MENDEZ, Julian Maxime

TVVLI	2015 Topical Workshop on Electronics for Function Hydroxy Trogramme	ruesday 5 September 201
17:20	[90] The powering concept of the CBM Silicon Tracking System	Dr KOCZON, Piotr
17:20	[85] Analog front-end characterization of the RD53A chip	EMRISKOVA, Natalia
17:20	[82] Design of the Back end card for the JUNO experiment	Dr YANG, Yifan
17:20	[73] Processing of the Liquid Xenon Calorimeter's Signals for Timing Measurements	Mr EPSHTEYN, Leonid
17:20	[69] The eTx line driver and the eRx line receiver: two building blocks for data and clock transmission using the CLPS standard	GUO, Di
17:20	[67] Proton-Induced Radiation Effects in MAROC3, a full readout 0.35 μm SiGe ASIC	Dr COJOCARIU, Lucian Nicolae
17:20	[64] GE1/1 Sustained Operations Investigations	STARLING, Elizabeth Rose
17:20	[60] Multi-threaded TCP hardware stack for pixel detector readout on 10 Gigabit Ethernet	Dr ZHANG, Jie
17:20	[50] The ETROC Project: ASIC development for CMS Endcap Timing Layer (ETL) upgrade	Dr LIU, Tiehui Ted
17:20	[39] New Quench Detection System to Enhance Protection of the Individually Powered Magnets in the Large Hadron Collider	HAAS, Severin
17:20	[27] Triggering on electrons, photons, tau leptons, jets and energy sums with the CMS Level-1 trigger	LAURILA, Santeri Henrikki
17:20	[25] Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase-II upgrade	TRONCON, Clara
17:20	[24] A High Speed Programmable Analog-to-Digital Conversion System Based On System in Package	Mr JIN, Ruyi
17:20	[18] VMM3a, an ASIC for tracking detectors	BAKALIS, Christos
17:20	[17] COLDATA Architecture, Design and Verification	HOFF, James
17:20	[15] A custom FPGA mezzanine card for crosstalk measurements of low-mass cables for the high luminosity upgrade of the ATLAS Pixel detector.	DUNNE, Katherine
17:20	[6] Radiation damage of Silicon Photomultipliers by irradiated fast neutrons	Mr TOPKO, Bogdan
17:20	[5] The hardware demonstrator of the Phase II ATLAS Level-0 MDT Trigger processor	Dr CIERI, Davide
17:20	[4] A NEW COMPACT ELECTRONICS FOR CALICE SIW CALORIMETER READOUT	JEGLOT, Jimmy
17:20	[3] Development of a high bandwidth PCIe card for the ATLAS HL-LHC Upgrade and DUNE experiment	CHEN, Kai
17:20	[2] Innovative and Expandable Physical Implementation Method for High-Speed Triple Modular Redundant Digital Integrated Circuits in Radiation-Hard Designs	VAN BOCKEL, Bjorn

Thursday 5 September 2019

Posters (16:55 - 18:30)

time	[id] title	presenter
16:55	[157] A 60 μ m2 HV-CMOS pixel with 0.5 ns timing resolution and 28 μ W power consumption for high-density arrays	MORENO, Sergio
16:55	[150] A 32-channel 1-10 GSa/s Flexible Waveform Recording System using the PSEC4A ASIC	PORTER, John
16:55	[147] Design and test of current DACs for threshold tuning of front-end channels for the High Luminosity LHC	GAIONI, Luigi
16:55	[146] Evaluation of embedded Linux distributions suitable for control and monitoring CMS phase 2 custom electronics	Dr ZEJDL, Petr
16:55	[142] VICE++: a building block of the debug and quality control systems for CMS ECAL upgrade on-detector electronics	Mr SINGOVSKI, Alexander
16:55	[137] MARTA's DAQ system	LUZ, Ricardo
16:55	[134] Simulation of new charge summing and hit allocation algorithm	JIRSA, Jakub
16:55	[129] A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature	Mr KUGATHASAN, Ramshan
16:55	[128] Back-end firmware for the LHCb VELO upgrade phase I	FERNANDEZ PRIETO, Antonio
16:55	[119] Throttling Studies for the CBM Self-triggered Readout	Dr GAO, Xin
16:55	[114] Design and operation of radiation hard 65 nm drivers for Silicon Photonics based optical links	CIARPI, Gabriele MAGAZZU, Guido
16:55	[113] KARATE - a setup for high rate tests on the CMS Outer Tracker 2S module readout chain	MAIER, Stefan
16:55	[110] First 10Gb/s Transmission with radiation-hardened Silicon Photonic Mach-Zehnder Modulators in a Full Transmission System	SCHNEIDER, Marc
16:55	[104] Study of a triggered, full event zero-suppressed front-end readout chain operating up to 1 MHz trigger rate and 300 pile-up for CMS Outer Tracker upgrade at HL-LHC	SCARFI, Simone
16:55	[101] Measurement results for AARDVARC: Waveform Sampling System On Chip with Picosecond Timing Resolution	MOSTAFANEZHAD, Isar
16:55	[100] Design of a radiation hardened TDC with a resolution of 4 ps and an improved interpolation technique	Mr VAN BOCKEL, Bjorn
16:55	[89] X-ray measurements of the effects of radiation damage in the miniMALTA DMAPS prototype	SIMON ARGEMI, Lluis
16:55	[87] Methods for Clock Signal Characterization using FPGA Peripherals	BIEREIGEL, Stefan
16:55	[81] First results of CIC data aggregation ASIC for the future CMS Tracker	CMS COLLABORATION, CMS collaboration NODARI, Benedetta
16:55	[74] The trigger system for the electromagnetic calorimeter of the COMET experiment.	EPSHTEYN, Leonid
16:55	[68] Calibration of Active Pixel Sensor based on TowerJazz 0.18 µm Technology with X-ray	Mr LI, Long
16:55	[66] Study of SEU effects in circuits developed in 110 nm UMC technology	CALVO, Daniela

16:55	[58] ATLASpix3 : A high voltage CMOS sensor chip designed for ATLAS Inner Tracker	PRATHAPAN, Mridula
16:55	[57] Implementation of a CANbus interface for the Detector Control System in the ALICE ITS Upgrade	NESBO, Simon Voigt
16:55	[53] Analysis of Time of Arrival Measurement with Low-Gain-Avalanche-Diode Sensor	Dr DEPTUCH, Grzegorz
16:55	[47] Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade	RASEVIC, Nikola
16:55	[43] CaRIBOu – A versatile data acquisition system based on programmable hardware	VANAT, Tomas
16:55	[37] Hardware production quality control for the ATLAS Phase-I readout upgrade	ALFONSI, Fabrizio
16:55	[33] Key Building Block Upgradation and Optimization for High-performance Transceivers: Multimode Interferometers from Conventional to Sub-wavelength Regime	Mr ZHANG, Yunlong
16:55	[31] Automated assembly of large double-sided microstrip detectors of the CBM Silicon Tracking System at FAIR	Mr PFISTNER, Patrick
16:55	[30] Readout and Trigger Electronics for the Triple-GEM Detectors of the CMS GE2/1 System	Mr MATVEEV, Mikhail
16:55	[28] A multi-channel trigger and acquisition board for TDC-based readout: application to the cosmic rays detector of the PolarQuEEEst 2018 project.	TRAVAGLINI, Riccardo
16:55	[22] A Fault-tolerance Readout Network for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC	XIAO, Le
16:55	[14] ATLAS Level-0 Endcap Muon Trigger for HL-LHC	KANO, Yuya
16:55	[9] Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments	PLACINTA, Vlad-Mihai
16:55	[8] FELIX – Commissioning the new detector interface for ATLAS trigger and readout	CHEN, Kai
16:55	[1] Coming challenges for Photon Science detectors: an ASIC designer perspective	Dr MARRAS, Alessandro
16:55	[11] A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector	Mr WALSEMANN, Alexander