Session Program

2–6 Sept 2019

TWEPP 2019 Topical Workshop on Electronics for Particle Physics

Posters

Tuesday 3 September

17:20

Posters

Session |
Location: Facultad de Química de la Universidad de Santiago de Compostela Avda. das Ciencias, s/n. (Campus Vida) 15782 Santiago de Compostela - Spain

17:20–17:40

Radiation damage of Silicon Photomultipliers by irradiated fast neutrons

Speaker
Mr Bogdan Topko

17:20–17:40

The hardware demonstrator of the Phase II ATLAS Level-0 MDT Trigger processor

Speaker
Dr Davide Cieri

17:20–17:40

A NEW COMPACT ELECTRONICS FOR CALICE SIW CALORIMETER READOUT

Speaker
Jimmy Jeglot

17:20–17:40

Development of a high bandwidth PCIe card for the ATLAS HL-LHC Upgrade and DUNE experiment

Speaker
Kai Chen

17:20–17:40

Innovative and Expandable Physical Implementation Method for High-Speed Triple Modular Redundant Digital Integrated Circuits in Radiation-Hard Designs

Speaker
Bjorn Van Bockel

17:20–17:40

A High Speed Programmable Analog-to-Digital Conversion System Based On System in Package

Speaker
Mr Ruyi Jin

17:20–17:40

CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade

Speakers
CMS collaboration CMS collaboration, Olivier Gevin

17:20–17:40

A SiPM Readout Front-end with Fast Pulse Generation and Successive-Approximation Register ADC

Speaker
Yuxuan Tang

17:20–17:40

EureKA-Maru: an ATCA board for the CMS Phase 2 Tracker Upgrade with centralized slow control and board management solution based on a Zynq Ultrascale+ System-on-Chip

Speaker
Luis Ardila

17:20–17:40

ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS

Speaker
Raimon Casanova Mohr

17:20–17:40 **RD53A chip susceptibility to electromagnetic conducted noise**

Speaker
Alvaro Pradas Luengo

17:20–17:40 **Qualification of the final LHCb VELO electronics**

Speaker
Dr Edgar Lemos Cid

17:20–17:40

The VRP - a Versatile Readout Platform for the nuclear experiments at HIRFL-CSR

Speaker
Prof. Chengxin Zhao

17:20–17:40

Test results of a Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

Speaker
Maria Robles Manzano

17:20–17:40

A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePIx4

Speaker
Raimon Casanova Mohr

17:20–17:40

The first ASIC prototype of a 28 nm time-space front-end electronics for real-time tracking

Speaker
Mr Lorenzo Piccolo

17:20–17:40

Overview of Electronics Developed by ISE for the European Spallation Source Project

Speaker
Mr Igor Rutkowski

17:20–17:40 **The Firmware for the European Spallation Source Cavity Simulator**

Speaker
Maciek Grzegrzółka

17:20–17:40

Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs

Speaker
Alessandro Caratelli

17:20–17:40

20 Mrad-TID Effects on Time over Threshold performance of GEMINI chip

Speaker
Luca Mangiagalli

17:20–17:40

Triple-Modular Redundancy Deployment Optimization in the Sensor Readout System of the CBM Micro Vertex Detector

Speaker
Yue ZHAO

17:20–17:40 **A Monolithic Active Pixel Sensor for CEPC vertex detector**

Speaker
Mr Tianya Wu

17:20–17:40

FAST: a front-end readout ASIC for a 30 ps time resolution with 6 pF UFSD sensors

Speaker
Dr Federico Fausti

17:20–17:40 **Upgrade of the ATLAS TileCal High Voltage system**

Speaker
Agostinho Da Silva Gomes

17:20–17:40

Readiness of the ATLAS Tile Calorimeter link daughterboard for the High Luminosity LHC era

Speaker
Eduardo Valdes Santurio

17:20–17:40

Design of Finite State Machines for SRAM-based FPGAs operated in radiation field

Speaker
Matteo Lupi

17:20–17:40 **LpGBT Tester: an FPGA based test system for the lpGBT ASIC**

Speaker
Julian Maxime Mendez

17:20–17:40 **The powering concept of the CBM Silicon Tracking System**

Speaker
Dr Piotr Koczon

17:20–17:40 **Analog front-end characterization of the RD53A chip**

Speaker
Natalia Emriskova

17:20–17:40 **Design of the Back end card for the JUNO experiment**

Speaker
Dr Yifan Yang

17:20–17:40
Processing of the Liquid Xenon Calorimeter’s Signals for Timing Measurements

Speaker
Mr Leonid Epshteyn

17:20–17:40
The eTx line driver and the eRx line receiver: two building blocks for data and clock transmission using the CLPS standard

Speaker
Di Guo

17:20–17:40
Proton-Induced Radiation Effects in MAROC3, a full readout 0.35 µm SiGe ASIC

Speaker
Dr Lucian Nicolae Cojocariu

17:20–17:40 **GE1/1 Sustained Operations Investigations**

Speaker
Elizabeth Rose Starling

17:20–17:40
Multi-threaded TCP hardware stack for pixel detector readout on 10 Gigabit Ethernet

Speaker
Dr Jie Zhang

17:20–17:40
The ETROC Project: ASIC development for CMS Endcap Timing Layer (ETL) upgrade

Speaker
Dr Tiehui Ted Liu

17:20–17:40
New Quench Detection System to Enhance Protection of the Individually Powered Magnets in the Large Hadron Collider

Speaker
Severin Haas

17:20–17:40
Triggering on electrons, photons, tau leptons, jets and energy sums with the CMS Level-1 trigger

Speaker
Santeri Henrikki Laurila

17:20–17:40
Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase-II upgrade

Speaker
Clara Troncon

17:20–17:40 **VMM3a, an ASIC for tracking detectors**

Speaker
Christos Bakalis

17:20–17:40 **COLDATA Architecture, Design and Verification**

Speaker
James Hoff

17:20–17:40
A custom FPGA mezzanine card for crosstalk measurements of low-mass cables for the high luminosity upgrade of the ATLAS Pixel detector.

Speaker
Katherine Dunne

18:50

Thursday 5 September

16:55

Posters

Session |
Location: Facultad de Química de la Universidad de Santiago de Compostela Avda. das Ciencias, s/n. (Campus Vida) 15782 Santiago de Compostela - Spain

16:55–17:15 **Study of SEU effects in circuits developed in 110 nm UMC technology**

Speaker
Daniela Calvo

16:55–17:15
Calibration of Active Pixel Sensor based on TowerJazz 0.18 µm Technology with X-ray

Speaker
Mr Long LI

16:55–17:15
The trigger system for the electromagnetic calorimeter of the COMET experiment.

Speaker
Leonid Epshteyn

16:55–17:15 **First results of CIC data aggregation ASIC for the future CMS Tracker**

Speakers
CMS collaboration CMS collaboration, Benedetta Nodari

16:55–17:15 **MARTA's DAQ system**

Speaker
Ricardo Luz

16:55–17:15
VICE++: a building block of the debug and quality control systems for CMS ECAL upgrade on-detector electronics

Speaker
Mr Alexander Singovski

16:55–17:15
Evaluation of embedded Linux distributions suitable for control and monitoring CMS phase 2 custom electronics

Speaker
Dr Petr Zejdl

16:55–17:15
Design and test of current DACs for threshold tuning of front-end channels for the High Luminosity LHC

Speaker
Luigi Gaioni

16:55–17:15

A 32-channel 1-10 GSa/s Flexible Waveform Recording System using the PSEC4A ASIC

Speaker
John Porter

16:55–17:15

A 60µm2 HV-CMOS pixel with 0.5 ns timing resolution and 28 µW power consumption for high-density arrays

Speaker
Sergio Moreno

16:55–17:15

KARATE - a setup for high rate tests on the CMS Outer Tracker 2S module readout chain

Speaker
Stefan Maier

16:55–17:15

A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector

Speaker
Mr Alexander Walsemann

16:55–17:15

Coming challenges for Photon Science detectors: an ASIC designer perspective

Speaker
Dr Alessandro Marras

16:55–17:15

FELIX – Commissioning the new detector interface for ATLAS trigger and readout

Speaker
Kai Chen

16:55–17:15

Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments

Speaker
Vlad-Mihai Placinta

16:55–17:15 **ATLAS Level-0 Endcap Muon Trigger for HL-LHC**

Speaker
Yuya Kano

16:55–17:15

A Fault-tolerance Readout Network for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

Speaker
Le Xiao

16:55–17:15

A multi-channel trigger and acquisition board for TDC-based readout: application to the cosmic rays detector of the PolarQuEEEst 2018 project.

Speaker
Riccardo Travaglini

16:55–17:15
Readout and Trigger Electronics for the Triple-GEM Detectors of the CMS GE2/1 System

Speaker
Mr Mikhail Matveev

16:55–17:15
Automated assembly of large double-sided microstrip detectors of the CBM Silicon Tracking System at FAIR

Speaker
Mr Patrick Pfistner

16:55–17:15
Key Building Block Upgradation and Optimization for High-performance Transceivers: Multimode Interferometers from Conventional to Sub-wavelength Regime

Speaker
Mr Yunlong Zhang

16:55–17:15
Hardware production quality control for the ATLAS Phase-I readout upgrade

Speaker
Fabrizio Alfonsi

16:55–17:15
CaRIBOu – A versatile data acquisition system based on programmable hardware

Speaker
Tomas Vanat

16:55–17:15
Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade

Speaker
Nikola Rasevic

16:55–17:15
Analysis of Time of Arrival Measurement with Low-Gain-Avalanche-Diode Sensor

Speaker
Dr Grzegorz Deptuch

16:55–17:15
Implementation of a CANbus interface for the Detector Control System in the ALICE ITS Upgrade

Speaker
Simon Voigt Nesbo

16:55–17:15
ATLASpix3 : A high voltage CMOS sensor chip designed for ATLAS Inner Tracker

Speaker
Mridula Prathapan

16:55–17:15 **Methods for Clock Signal Characterization using FPGA Peripherals**

Speaker
Stefan Biereigel

16:55–17:15
X-ray measurements of the effects of radiation damage in the miniMALTA DMAPS prototype

Speaker
Lluis Simon Argemi

16:55–17:15
Design of a radiation hardened TDC with a resolution of 4 ps and an improved interpolation technique

Speaker
Mr Bjorn Van Bockel

16:55–17:15
Measurement results for AARDVARC: Waveform Sampling System On Chip with Picosecond Timing Resolution

Speaker
Isar Mostafanezhad

16:55–17:15
Study of a triggered, full event zero-suppressed front-end readout chain operating up to 1 MHz trigger rate and 300 pile-up for CMS Outer Tracker upgrade at HL-LHC

Speaker
Simone Scarfi

16:55–17:15
First 10Gb/s Transmission with radiation-hardened Silicon Photonic Mach-Zehnder Modulators in a Full Transmission System

Speaker
Marc Schneider

16:55–17:15
Design and operation of radiation hard 65 nm drivers for Silicon Photonics based optical links

Speakers
Gabriele Ciarpi, Guido Magazzu

16:55–17:15 **Throttling Studies for the CBM Self-triggered Readout**

Speaker
Dr Xin Gao

16:55–17:15 **Back-end firmware for the LHCb VELO upgrade phase I**

Speaker
Antonio Fernandez Prieto

16:55–17:15 **Simulation of new charge summing and hit allocation algorithm**

Speaker
Jakub Jirsa

16:55–17:15
A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature

18:30

Speaker
Mr Ramshan Kugathasan