System-on-Chip Workshop
12-14 June, CERN

WELCOME!

https://indico.cern.ch/event/799275

System-on-Chip Workshop

This workshop wants to be a forum
to exchange experience and ideas,
to identify commonality and differences,
to propose common solutions wherever applicable,
and to point out issues that need follow up.

Interest Group "System-on-Chip for Electronics"
→ Mailing list: system-on-chip@cern.ch

Organisation of the Workshop

Organising Committee

Marc DOBSON
CMS TDAQ SysAdmin

Revital KOPELIANSKY
ATLAS TDAQ DCS

Frans MEIJERS
CMS DAQ

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ATLAS TDAQ SysAdmin

Ralf SPIWOKS
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- We wish you a warm WELCOME!

- If you have questions on the organisation of the workshop or on your presentations, etc. please contact any of us.
- You can also send and email to the organizers: SoC-Workshop-Organisers@cern.ch or if it is of general interest: System-on-Chip@cern.ch

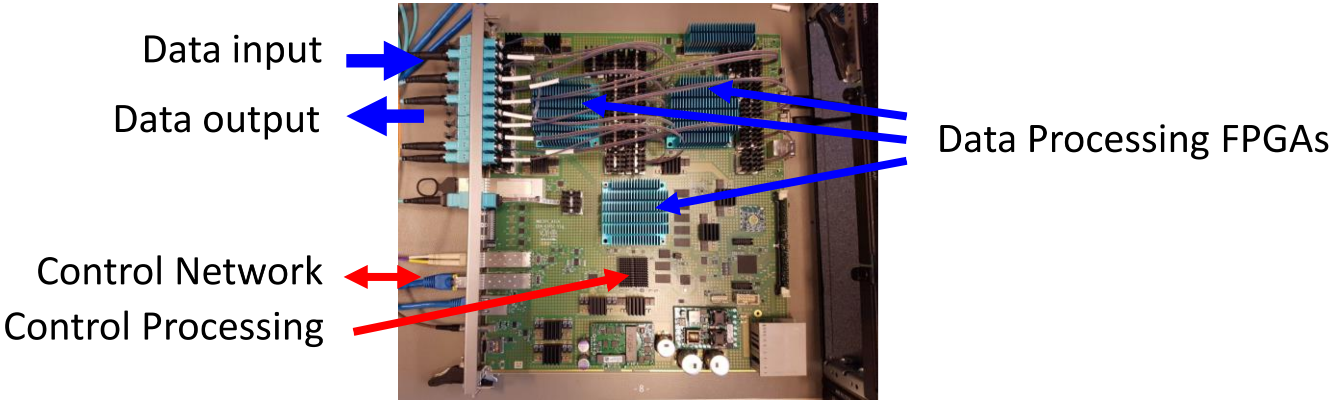
Overview of the Workshop

	WED, June 12 Room 30/7-018	THU, June 13 Room 40/S2-B01	FRI, June 14 Room 40/S2-C01
Morning	Manufacturer Presentations 1	Tutorials & Presentations 1	Tutorials & Presentations 3
	Coffee/tea break	Coffee/tea break	Coffee/tea break
	Manufacturer presentations 2	Tutorials & Presentations 2	Tutorials & Presentations 4
	Lunch	Lunch	Lunch
Afternoon	Overview and Use Cases 1	Use Cases 3	System Aspects 1
	Tea/coffee break	Tea/coffee break	Tea/coffee break
	Use Cases 2	Use Cases 4	System Aspects 2

- **Please have a look at https://indico.cern.ch/event/799275**
- **Note: use different rooms: WED: bldg. 30/7-18, THU&FRI: bldg. 40/Salle Bohr and Salle Curie.**
- **Rooms in bldg. 40 are limited to a capacity of 100 – apologies! We will use Vidyo …**
- **Coffee/tea is kindly offered by EP-ESE, EP-CMD and ATLAS.**
- **We will take minutes, in particular of discussions, which will be published later in Indico.**
- **Hope to have lively discussions …**

Motivation for the Workshop

Electronics Modules



Data input

Data output

Control Network

Control Processing

Data Processing FPGAs

Many electronics modules for trigger and readout in particle physics experiments have a similar structure:

- Several high-end FPGAs for processing, usually 1 to 5.
- Many high-speed links for data input and output, usually ~10 to ~500 links of 1 to 28 GBits/s (planned) .
- Something for control … a System-on-Chip

Control (send commands), Configuration (load data), Monitoring (collect data):

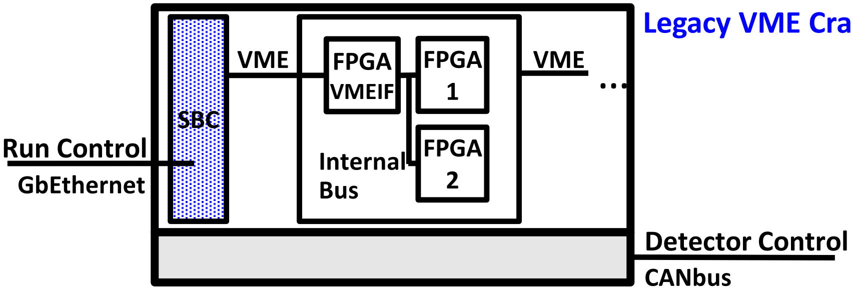
- **Hardware related**, e.g. settings and actual values of power, clock, optical chips, FPGAs, etc., usually using industry standard protocols like I2C, SPI, JTAG, etc.
- **Run control related**, i.e. related to physics/run (functionality implemented in firmware of FPGAs), e.g. control and status registers, memories, look-up tables, counters, physics data, etc.

Electronics Systems

In the past, very popular - VME:

Hardware control: CANbus

Run control: Single-Board Computer (SBC) or VME bridge and PC



Legacy VME Crate

Today, many new projects use ATCA:

Control is oriented towards GbEthernet:

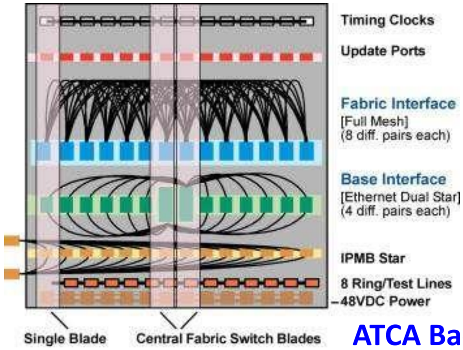
Hardware control:

Blade → IPMI → shelf manager → SCADA*

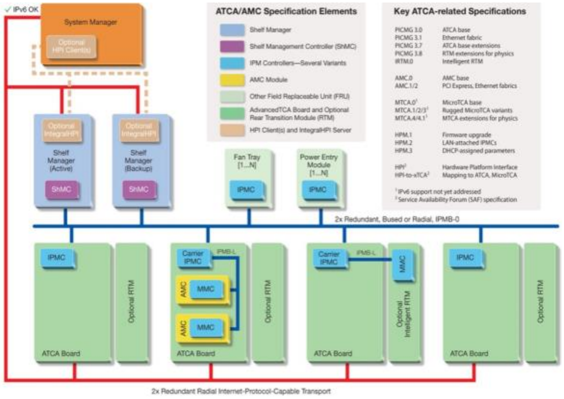
Run control:

Via hub module and base interface, or directly to each ATCA blade …

⇒ **Need a new control strategy!**



ATCA Backplane


✓ IPv6 OK
System Manager
Optional HPI Client(s)
Optional IntegralHPI
Shelf Manager (Active)
ShMC
Optional IntegralHPI
Shelf Manager (Backup)
ShMC
Fan Tray [1...N]
IPMC
Power Entry Module [1...N]
IPMC
2x Redundant, Bused or Radial, IPMB-0
IPMC
Optional RTM
ATCA Board
Carrier IPMC
IPMB-L
AMC
MMC
AMC
MMC
Optional RTM
ATCA Board
Carrier IPMC
IPMB-L
MMC
Optional Intelligent RTM
ATCA Board
IPMC
Optional RTM
ATCA Board
2x Redundant Radial Internet-Protocol-Capable Transport
ATCA/AMC Specification Elements
Shelf Manager
Shelf Management Controller (ShMC)
IPM Controllers—Several Variants
AMC Module
Other Field Replaceable Unit (FRU)
AdvancedTCA Board and Optional Rear Transition Module (RTM)
HPI Client(s) and IntegralHPI Server

Key ATCA-related Specifications

PICMG 3.0	ATCA base
PICMG 3.1	Ethernet fabric
PICMG 3.7	ATCA base extensions
PICMG 3.8	RTM extensions for physics
IRTM.0	Intelligent RTM
AMC.0	AMC base
AMC.1/2	PCI Express, Ethernet fabrics
MTCA.0[1]	MicroTCA base
MTCA.1/2/3[1]	Rugged MicroTCA variants
MTCA.4/4.1[1]	MTCA extensions for physics
HPM.1	Firmware upgrade
HPM.2	LAN-attached IPMCs
HPM.3	DHCP-assigned parameters
HPI[2]	Hardware Platform Interface
HPI-to-xTCA[2]	Mapping to ATCA, MicroTCA

[1] IPv6 support not yet addressed

[2] Service Availability Forum (SAF) specification

ATCA Hardware Platform Management

*SCADA = Supervisory Control And Data Acquisition

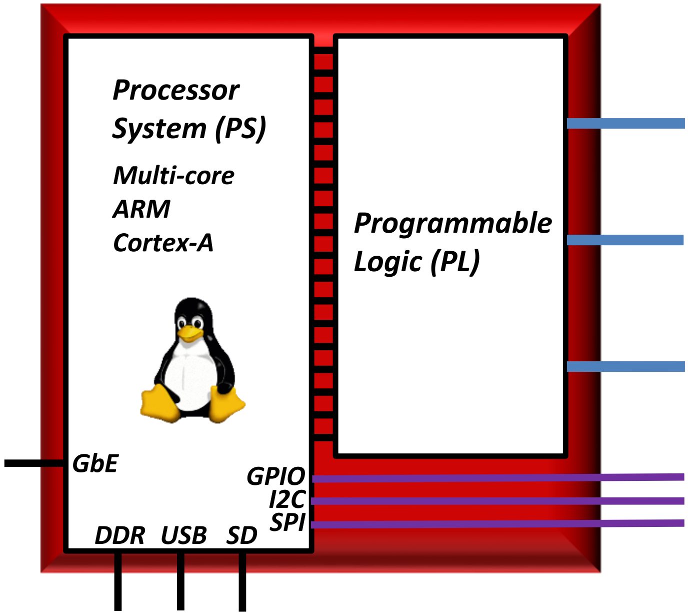
System-on-Chip

System-on-Chip:

Processor system + programmable logic ⇒ ***"CPU and FPGA"***

This definition of SoC is more restrictive than in Wikipedia

- **Processor system (PS) =** like CPU:
  - Currently all are multi-core ARM processors
  - Has memory and peripherals, e.g. GbEthernet, I2C, SPI, GPIO, etc.
  - Runs software: "bare-metal" application or operating system, e.g. Linux



- **Programmable logic (PL) =** like FPGA:
  - Has logic cells, memory blocks, and I/O links, e.g. Multi-Gigabit Transceivers (MGTs)
  - Implements real-time data logic, interfaces to the other processing FPGAs, can implement more peripherals, e.g. 10GbEthernet, etc.

→ Examples of SoCs:

Xilinx Zynq SoC, Xilinx Zynq UltraScale+ MPSoC, Intel Stratix 10 SoC

We will hear from the manufacturers during this morning's session

Use of System-on-Chip

- **Interface between hardware and software**
- **Programmable Logic part of SoC very well known to hardware designers**
- **Processor System of SoC provides a lot of flexibility and integrates the electronics modules into the control network(s)**
- **Possibility to push more "intelligence" into the electronics modules**
- **Typical use cases for SoCs:**
  - **Interactive tools**
  - **Integration with Detector Control System for hardware control**
  - **Integration with Run Control System for operational control**
  - **Trigger processing**
  - **Readout of physics data**
  - **Physics-oriented calibration and monitoring tasks**
  - **Etc.**

We will see many examples during the "Use cases" and "Tutorials&Presentations" sessions

System-on-Chip Workshop

Concerns and issues on use of SoCs:

- Hardware/firmware part:
  - Exchange of experience and of solutions:
    Can we provide a common repository of IP blocks?
  - Provide common hardware solutions:
    Can we provide recommendation on the hardware choice?
    Is possible to build or purchase a common SoC mezzanine card for control?
- Software part: flexibility has a cost = support and maintenance
  - How to organise network, in particular, with many , o(100-1000), SoCs:
    Network switches, IP numbers, boot services, etc.
  - How to provide network security:
    Technical control networks for experiments and beams have strict security requirements.
  - Provide common software solutions:
    Common support for operating system, drivers, libraries, tools?
  - Provide long-term maintenance:
    Can a common SoC mezzanine card address this issue?

Many of these issues will be discussed during the "System Aspects" sessions

… and probably more. Your input is important!

Have a good workshop!