System-on-Chip Workshop
12-14 June, CERN

WELCOME!

https://indico.cern.ch/event/799275
System-on-Chip Workshop

This workshop wants to be a forum to exchange experience and ideas, to identify commonality and differences, to propose common solutions wherever applicable, and to point out issues that need follow up.

*Interest Group “System-on-Chip for Electronics”*

→ Mailing list: system-on-chip@cern.ch
Organisation of the Workshop
We wish you a warm WELCOME!

If you have questions on the organisation of the workshop or on your presentations, etc. please contact any of us.

You can also send and email to the organizers: Soc-Workshop-Organisers@cern.ch or if it is of general interest: System-on-Chip@cern.ch
**Overview of the Workshop**

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- Please have a look at [https://indico.cern.ch/event/799275](https://indico.cern.ch/event/799275)
- Note: use different rooms: WED: bldg. 30/7-18, THU&FRI: bldg. 40/Salle Bohr and Salle Curie.
- Rooms in bldg. 40 are limited to a capacity of 100 – apologies! We will use Vidyo ...
- Coffee/tea is kindly offered by EP-ESE, EP-CMD and ATLAS.
- We will take minutes, in particular of discussions, which will be published later in Indico.
- Hope to have lively discussions ...

SoC Workshop - 12-JUN-2019
R. Spiwoks
Motivation for the Workshop
Many electronics modules for trigger and readout in particle physics experiments have a similar structure:

- Several high-end FPGAs for processing, usually 1 to 5.
- Many high-speed links for data input and output, usually ~10 to ~500 links of 1 to 28 GBits/s (planned).
- Something for control ... a System-on-Chip

**Control (send commands), Configuration (load data), Monitoring (collect data):**

- **Hardware related**, e.g. settings and actual values of power, clock, optical chips, FPGAs, etc., usually using industry standard protocols like I2C, SPI, JTAG, etc.

- **Run control related**, i.e. related to physics/run (functionality implemented in firmware of FPGAs), e.g. control and status registers, memories, look-up tables, counters, physics data, etc.
Electronics Systems

In the past, very popular - **VME**:

**Hardware control**: CANbus

**Run control**: Single-Board Computer (SBC) or VME bridge and PC

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Today, many new projects use **ATCA**:

Control is oriented towards GbEthernet:

**Hardware control**:

Blade → IPMI → shelf manager → SCADA*

**Run control**:

Via hub module and base interface, or directly to each ATCA blade ...

⇒ **Need a new control strategy!**

*SCADA = Supervisory Control And Data Acquisition
System-on-Chip

**System-on-Chip:**
Processor system + programmable logic ⇒ “CPU and FPGA”

- **Processor system (PS) =** like CPU:
  - Currently all are multi-core ARM processors
  - Has memory and peripherals, e.g. GbEthernet, I2C, SPI, GPIO, etc.
  - Runs software: “bare-metal” application or operating system, e.g. Linux

- **Programmable logic (PL) =** like FPGA:
  – Has logic cells, memory blocks, and I/O links, e.g. Multi-Gigabit Transceivers (MGTs)
  – Implements real-time data logic, interfaces to the other processing FPGAs, can implement more peripherals, e.g. 10GbEthernet, etc.

→ **Examples of SoCs:**
Xilinx Zynq SoC, Xilinx Zynq UltraScale+ MPSoC, Intel Stratix 10 SoC

This definition of SoC is more restrictive than in Wikipedia

We will hear from the manufacturers during this morning’s session
Use of System-on-Chip

• Interface between hardware and software
• Programmable Logic part of SoC very well known to hardware designers
• Processor System of SoC provides a lot of flexibility and integrates the electronics modules into the control network(s)
• Possibility to push more “intelligence” into the electronics modules
• Typical use cases for SoCs:
  – Interactive tools
  – Integration with Detector Control System for hardware control
  – Integration with Run Control System for operational control
  – Trigger processing
  – Readout of physics data
  – Physics-oriented calibration and monitoring tasks
  – Etc.

We will see many examples during the “Use cases” and “Tutorials&Presentations” sessions
Concerns and issues on use of SoCs:

• **Hardware/firmware part:**
  – **Exchange of experience and of solutions:**
    Can we provide a common repository of IP blocks?
  – **Provide common hardware solutions:**
    Can we provide recommendation on the hardware choice?
    Is possible to build or purchase a common SoC mezzanine card for control?

• **Software part: flexibility has a cost = support and maintenance**
  – **How to organise network, in particular, with many o(100-1000), SoCs:**
    Network switches, IP numbers, boot services, etc.
  – **How to provide network security:**
    Technical control networks for experiments and beams have strict security requirements.
  – **Provide common software solutions:**
    Common support for operating system, drivers, libraries, tools?
  – **Provide long-term maintenance:**
    Can a common SoC mezzanine card address this issue?

... and probably more. Your input is important!
Have a good workshop!