SoC R&D for CMS Phase-2 Tracker Back-end Electronics

Luis Ardila, Oliver Sander, Matthias Balzer
Slow Control at Tracker R&D Boards

Enclustra ZX1
- AXI-C2C
- TCDS (TTS)
- Eth

CERN-IPMC
- IPMI
- Eth
- PMBus

Artix 7
- TCDS
- Eth
- I2C
- PMBus

Com-Express
- PCIe
- Eth

See D. Gastler’s talk tomorrow

Institute for Data Processing and Electronics (IPE)
SoC on Serenity

Trenz ZynqUS+ 4EG

Com-Express
- PCIe
- Eth

CERN-IPMC
- IPMI
- Eth
- PMBus

Artix 7
- TCDS
- Eth
- I2C
- PMBus

This Talk
We believe that not only a single specification could be reached but as well the use of a single device… a Zynq US+ (integrating IPMC, SC and FPGA)
Integrated Management Architecture

- **IPMI** (standalone/RTOS) on ARM-R5 processor
- **Slow Control** (Linux) on ARM-A53 Cores
- **TCDS** in PL-FPGA
- Xilinx Virtual Cable (**XVC**) JTAG
- **Link to main FPGAs via PL-MGTs** (PCIe-IPBus or AXI C2C)
- **I2C-SPI** to configure Optics/Clocks
- **PMBus** to configure Power Supplies
- **Eth** and **I2C** backplane connection
Current Hardware Setup

- Trenz TE0803 Module (Zynq Ultrascale+ XCZU4EG)
  - 2 GB RAM / quad core A53 / dual core R5 / 4 GTH
- Dimm Adapter for (CERN/LAPP) IPMC footprint
- Trenz to Com-Express adapter v1.0 [link]
  - USB 2.0 phy
  - Ethernet phy
  - PS_PCIE to FPGA_X0
  - PS_PCIE and UART to Artix
  - PL_PCIE/PL_C2C to FPGA_X1
  - IPMC to backplane
Pigeon Point IPMC SW

- ✔ Test and debug interfaces (ETH, I2C, UART, JTAG)
- ✔ Boot standalone application from QSPI flash
- ✔ Petalinux running on the ARM-A53 Processors
  - ✔ SSH to Linux on ZynqUS+
- ✔ Pigeon Point IPMC standalone software compiled for the ARM-R5 processors
  - ✔ Build FSLB, PMU & PP_IPMC + Petalinux in one image
  - ✔ Boot FSLB, PMU & PP_IPMC software from QSPI flash
  - ✔ Test connection with shelf manager
  - □ Test power cycle from shelf manager and PMBus access
Pulsar IIb IPMC SW

Avnet Ultra96 board

- SPRACE porting the Pulsar IIb IPMC software to ZynqUS+ architecture.
- Setting up library for peripheral abstraction
  #include IPMC_periphs.h
- ✔️ Fundamental communication tests performed
  - IPMB, HA[0..7], Handle,

Work from André Cascadan
IPbus on ZynqUS+

- Chip-To-Chip AXI IP core with a single-lane multi-gigabit transceiver (64b/66b Aurora)

Work by Paschalis Vichoudis and Tom Williams
uHAL on CentOS

- Tested uHAL ↔ Zynq-based IPbus FW
  - uHAL: mmap-based IPbus client updated to be able to specify base address offset in file mapping
    - URI:ipbusmmap-2.0:///dev/mem?offset=0xa0010000
  - Standard uHAL-based soak test ran against IPbus transactors in ‘local’ & ‘remote’ parts of Zynq FW
    - Random sequence of 1M transactions with no errors
- Cross-compiling uHAL (for Petalinux)
  - Makefiles updated to support cross compilation out of the box (without any modifications)

Work by Paschalis Vichoudis and Tom Williams
Limitations on power consumption

Maximum standby power from PIM module ~\textbf{11 W} (~\textbf{8 W at 70%})

- Full powered device with Petalinux or IPMC software is well within this power limit
  - Boot of full powered device much simpler than partially switching powers

Boot of only low power domain (LPD) supported by ZynqUS+ and Pigeon Point SW

- Successful boot of First Stage Boot Loader (FSBL) of the ZynqUS+ with only LPD
  - Programmable logic (PL), Full Power Domain (FPD), DDR powered off

Full-fledged PL design and busy processors might consume more!

- Auxiliary power supplies might be required → ✔️ will be integrated in next version of adapter
Trenz-Serenity Adapter v1.1 “Extended” [link]

- Priority power multiplexer with seamless switchover
- Trenz to Com-Express adapter v1.1
  - USB 2.0 phy
  - Ethernet phy
  - Display Port
  - MicroSD Card
  - PL_MGT AXI-C2C
    - FPGA_X0, FPGA_X1, Artix7
- IPMC
  - Hot Swappable 2-WireBus Buffers
  - HA[0...7] via I2C I/O expander
  - EEPROM
  - Other recommendations from Pigeon Point

Fully routed → in review/tuning process
Management module v2.0 [link]

- Working together with Imperial College (IC) on a connector interface which could be used by either Com-Express or ZynqUS+
- All slow control interfaces on this interface
- Crystal ATCA board from IC will have this connector
  - MM70-314-310B1-1-R300
- Majority of components placed
  - validation of power mux and IPMI hot-swap from Adapter v1.1 needed
- Placement on Z3 area of ATCA blade possible
Summary

- Trend to integrate more infrastructure slow control functionality on ATCA boards
  - (e.g. X86 based ComExpress on Serenity, Zynq on Apollo, ...)
- We explore the integration of IPMC, Slow Control functionality and FPGA in one single heterogeneous device (Zynq Ultrascale+)
- Utilizing a single device propose long term maintenance benefits

- Required components successfully tested (IPMC, AXI-C2C, Power Modes, CentOS, IPBus)
- Components that need testing (TCDS on PL)
- Integration of tested components in a single device to be done
- Integration needs updated Adapter v1.1 due in July

So far everything looks promising
Questions ?