The Zynq MPSoC of the ATLAS L1Calo TREX

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Overview

- L1Calo PreProcessor
- TREX module
- Usage of Zynq MPSoC on TREX
- Zynq MPSoC Development & Plans
L1Calo in Phase-I

- New Feature Extractor (FEX) processors
  - improved object-finding algorithms
- Digital super-cells from LAr
  - ≤ 12.8 Gbps optical links
- Analogue trigger-towers from Tile
  - Tile Rear Extension (TREX) modules in the PreProcessor
    - provide Tile digitised results to FEXes
    - maintain legacy trigger data path
  - replaced by digital Tile PreProcessor in Phase-II
The PreProcessor

8 VME crates [6 LAr + 2 Tile]

124 hardware-identical PPMs [~16 PPMs/crate]

Legacy PreProcessor Module (PPM) (2007)
The PreProcessor in Phase-I

2 VME crates [Tile]

32 PPMs + 32 TREXes

TREX – RTM in the ‘Tile’ crates [acts as physical extension of the ‘front’ PPM]
TREX Module

• 18-layer PCB [9U VME height]

• Kintex UltraScale FPGA [PREDATOR]
  – xcku115 (prototype), xcku085 (pre-production)
  – real-time, readout, control, monitoring

• Artix-7 FPGAs (4x) [XC7A35T] [DINOs]
  – LVDS fan-out

• Samtec FireFly Transceivers (6x)
  – four 12-chan transmitters to FEXes
  – one 4-chan bidirectional [out – readout; in – TTC]
  – one 12-chan receiver [optical loopback tests]

• PLLs, power managers, monitoring ADCs, etc.

• Zynq UltraScale+ MPSoC [XCZU2CG]
  – from pre-production only

13/06/2019  V. Andrei - TREX Zynq+ MPSoC
Zynq MPSoC on the TREX pre-production (v2)

• TREX v2 currently being produced
• Zynq US+ based SoM [System-on-Module]
  – commercial mezzanine [details below]
  – usage
    • slow-control
    • communication with DCS
    • board control & monitoring
  – interface to VME/RunControl
    • configuration/control, monitoring, debugging, etc.

TE0820-03-02CG-1EA [Trenz Electronic]
- Zynq UltraScale+ XCZU2CG-1SFVC784E
  - dual-core ARM Cortex-A53 APU (64-bit)
- 2 GB DDR4 SDRAM (32-bit)
- 128 MB QSPI Boot Flash, 4 GB eMMC
- Gigabit Ethernet transceiver PHY
- MAC address EEPROM (EUI-48)
- USB 2.0 transceiver
- Plug-on module (3x B2B connectors)
- All power supplies on board
- Size: 50x40 mm
- etc.
Zynq MPSoC – Slow-Control

• PL: retrieve periodically environmental parameters from the board
  – T, V, I, alarms, etc. [~200 pars from 16 devices]
  – one I2C bus, two masters [arbitration from VME/RunControl]
    • Zynq [default]
    • VME/PPM [testing/debugging only]
  – data stored locally
    • accessible from PS and VME

• PS: communicate with DCS
  – OPC UA Server & TCP/IP
  – send slow-control data
    • upon requests from Client

13/06/2019
V. Andrei - TREX Zynq+ MPSoC
Zynq MPSoC – Board Control & Monitoring

- Power off & on the board
  - when requested from DCS or VME
- Configure on-board devices
  - FPGAs
    - JTAG [via Xilinx Virtual Cable on PS]
    - Master SPI [from PL, via I2C]
  - PLLs [via I2C]
    - PL: two PLLs on TREX
    - PS: one PLL on Zynq SoM
  - Power Managers [PL, via I2C]
- Build monitoring data
  - logs, diagnostic histograms, etc.
  - mostly based on slow-control data
  - stored on external devices, e.g.:
    - SD card, USB Flash [via PS]
    - TREX on-board EEPROM [via PL]
Zynq MPSoC - Development

• PL design
  – well established
  – available development
    • interface to PPM/VME, I2C interface to on-board devices
    • (VME) register model
    • Makefile and Tcl scripts for automatic build [non-project mode]
  – in progress
    • I2C bus arbitration [Zynq vs VME]
    • local storage of slow-control data
    • XML register files
      – generate HDL include files & basic documentation [e.g. and/or: md/xlsx/pdf/…]
  – only a standalone PL design needed for initial tests of TREX v2 modules
    • slow-control functionality, board control & monitoring (all steered from VME)
    • bitstream → load via JTAG
    • fsbl → boot from QSPI/SD card
PS: OS + application software
  - development not yet started
  - Linux-based OS
    - start with Petalinux
    - Yocto + CentOS preferred
  - Software
    - OPC UA SRV
    - Xilinx Virtual Cable (XVC)
    - custom monitoring apps

Boot options (OS)
  - SD card
    - not very efficient when having to update the system → 32 TREQes
  - Net booting (TFTP) → preferred
    - get quickly the latest development builds [e.g. during commissioning phase]
    - hopefully possible/allowed
• Questions?