Status of simulations of CMOS sensors with a small collection electrode

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Outline:

1.) Introduction

2.) CLICTD related simulations - open questions and answers

3.) Future developments

4.) Summary

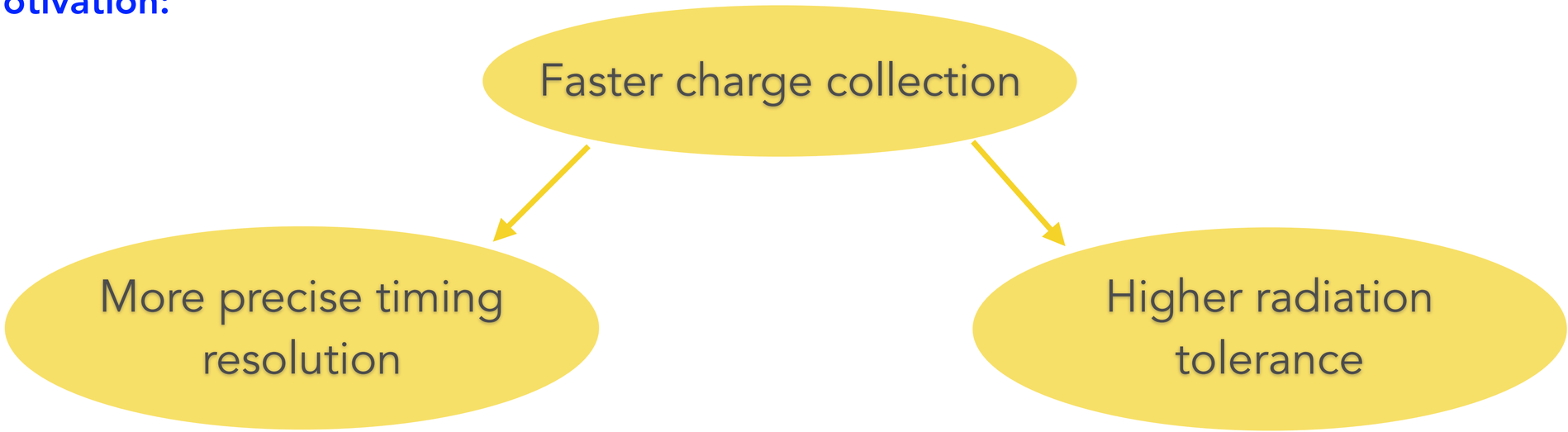
Introduction

Process modifications for CMOS sensors with a small collection electrode

Aim:

Faster charge collection in CMOS sensors with a small collection electrode

Motivation:



Benefit of small collection electrode is small capacitance

—> Precise time stamping

—> Process modifications optimise sensor layout to small collection electrode design

Process modifications

Modified process:

Gap in n-layer:

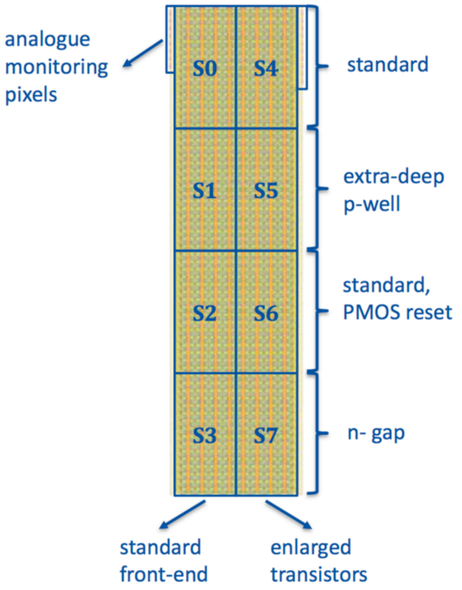
Additional p-implant:

Speed up charge collection by shaping field lines towards collection electrode

<u>All 3 versions have been implemented in ATLAS ITk Mini-Malta submission:</u>

- Fully integrated test-chip implemented in this technology with 16 x 16 pixels with a size of 36.4 um x 36.4 um
- Un-irradiated and irradiated chips currently under investigation in lab
- The chip is alive and very very preliminary results (electrical tests, source measurements) indicate significant differences between the different sensor versions
- They have Test-beam (DESY, ELSA) Mid-April

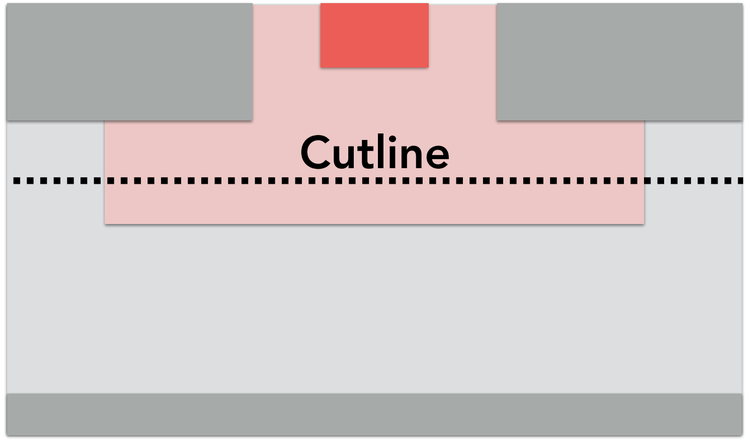
Mini-Malta:



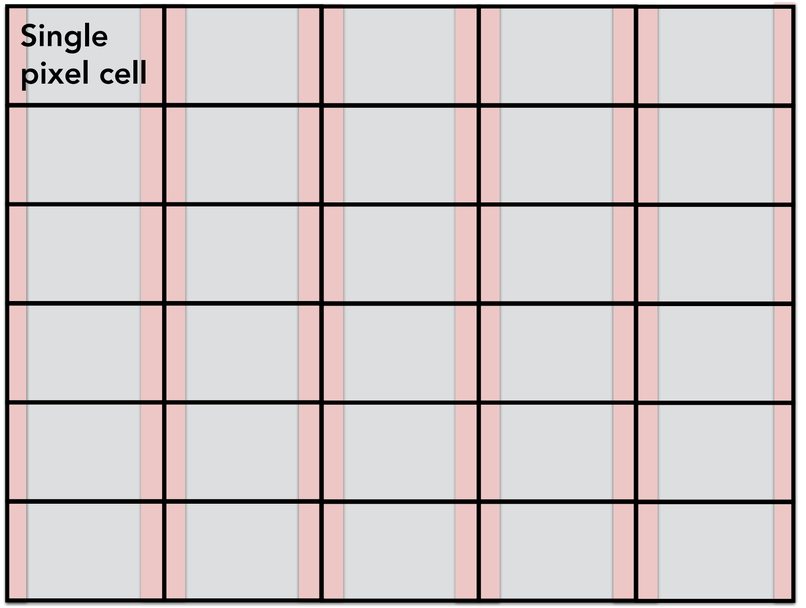
CLICTD

Modified process:

Gap in n-layer:



Profile of part of matrix along cutline:



Gap in n-layer implemented in process split:

- Selection of gap instead of additional p-implant to reduce uncertainties in doping
- Elongated pixels with sub-pixels of 37.5 um x 30 um, epi-thickness of 30 um
- Gap only crossing long dimensions as compromise between precise spatial resolution in short dimension and fast charge collection in long dimension
- Chip submitted ~ month ago (see next talk from Iraklis)

CLICTD -
Which n-layer dose?

Disclaimer:
simulations of CLICTD with 25 um epi-thickness

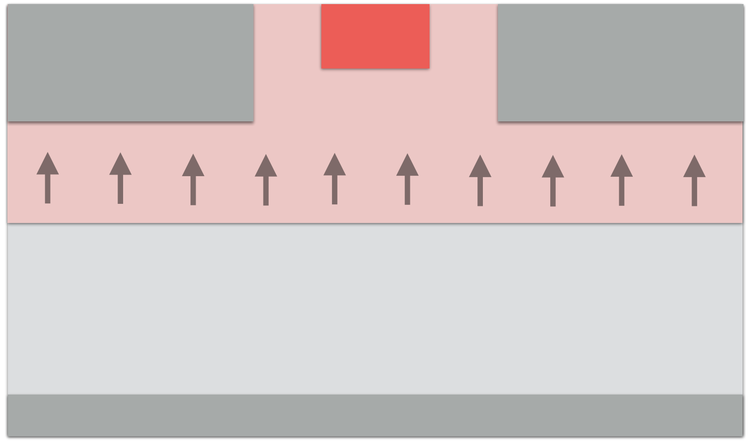
CLICTD - which n-layer dose?

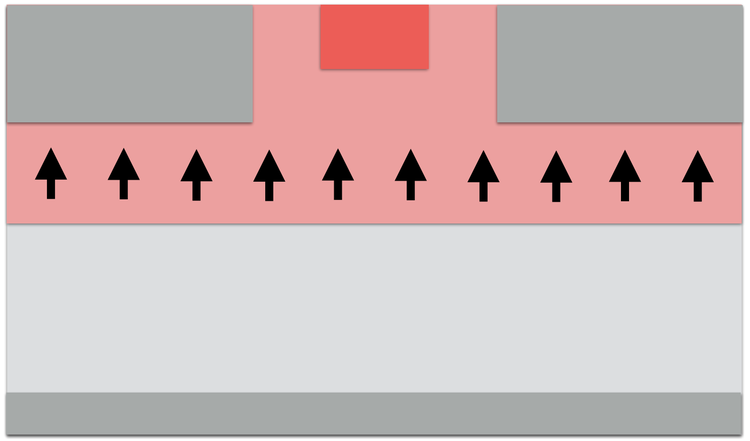
Some considerations

Low dose
(used for our Investigator studies):

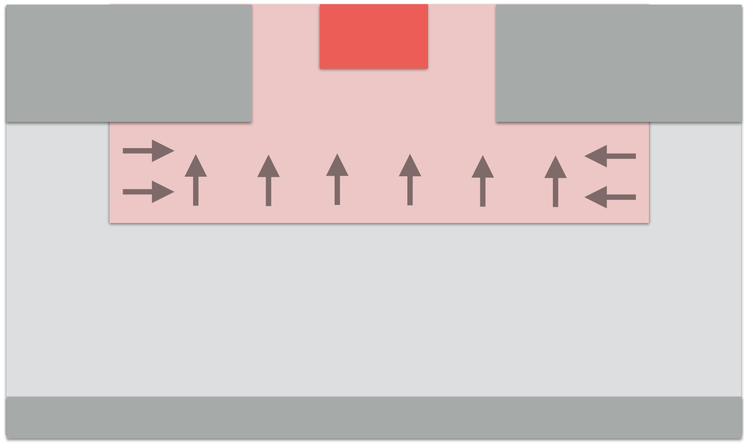
High dose:

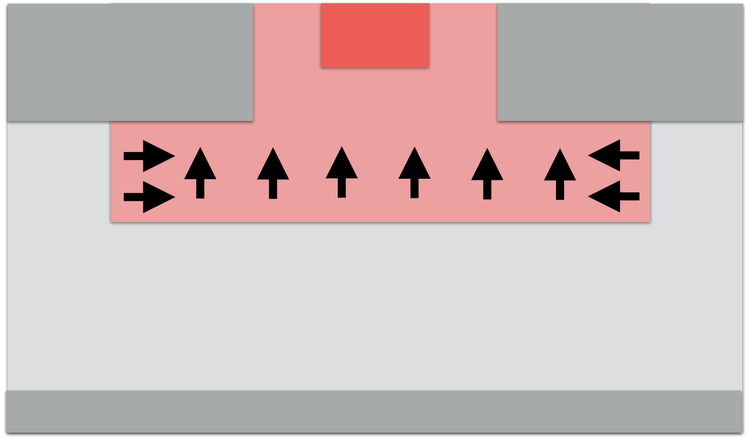
Modified process:





Gap in n-layer:





Black arrows indicate relevant electric field component:

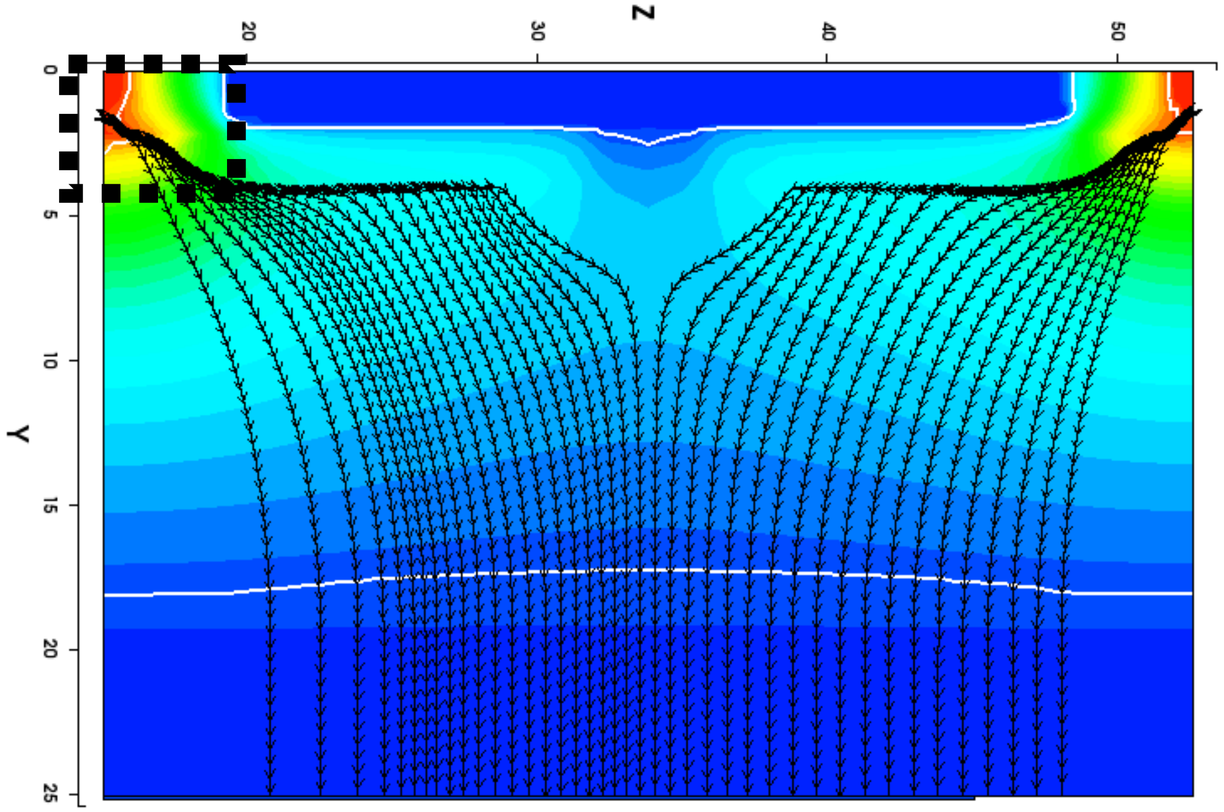
Modified process - higher dose:
Higher ***vertical*** field in pixel corner?
😢

Gap in n-layer - higher dose:
Higher ***lateral*** field in pixel corner?
😊

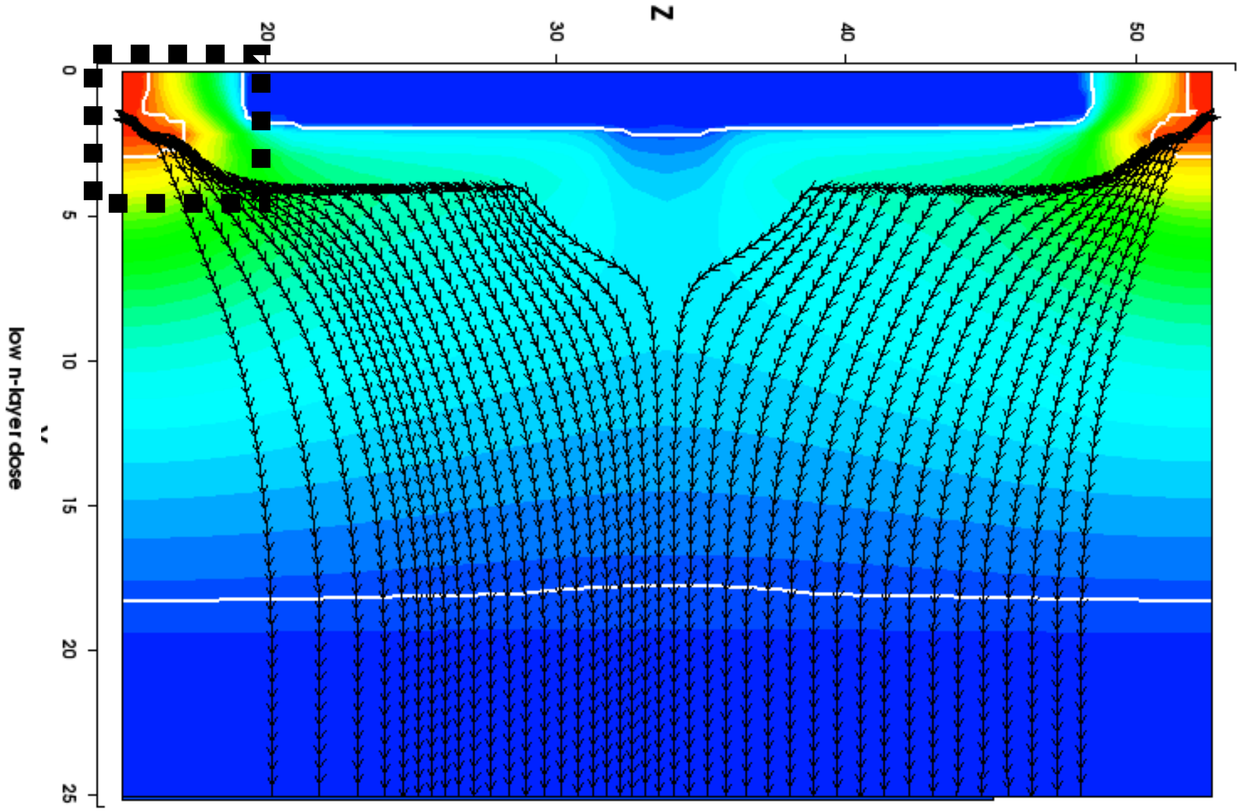
CLICTD - different n-layer doses for gap in n-layer

Lateral field:

Low dose (used for our Investigator studies):



High dose:



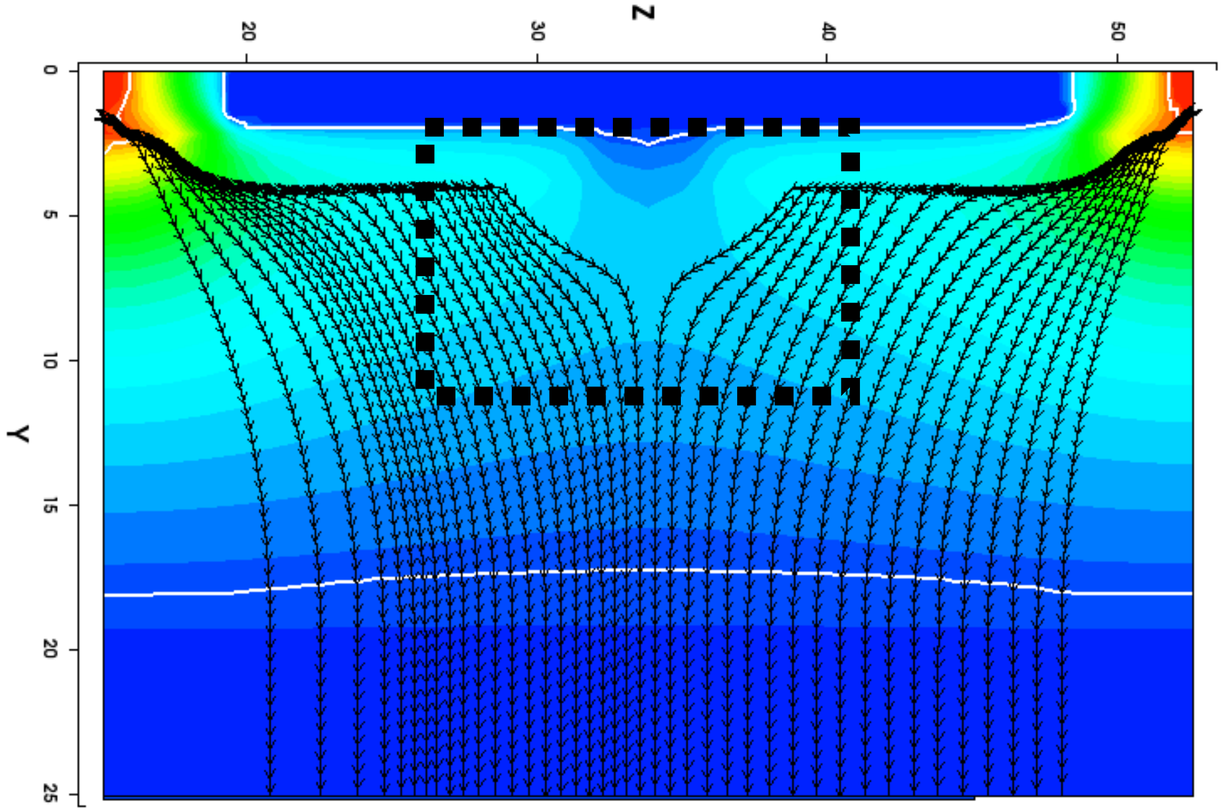
- Less depletion around collection electrode for higher dose

↳ Impact on capacitance of ~ 30 % (electrostatic TCAD simulations and 55Fe measurements)

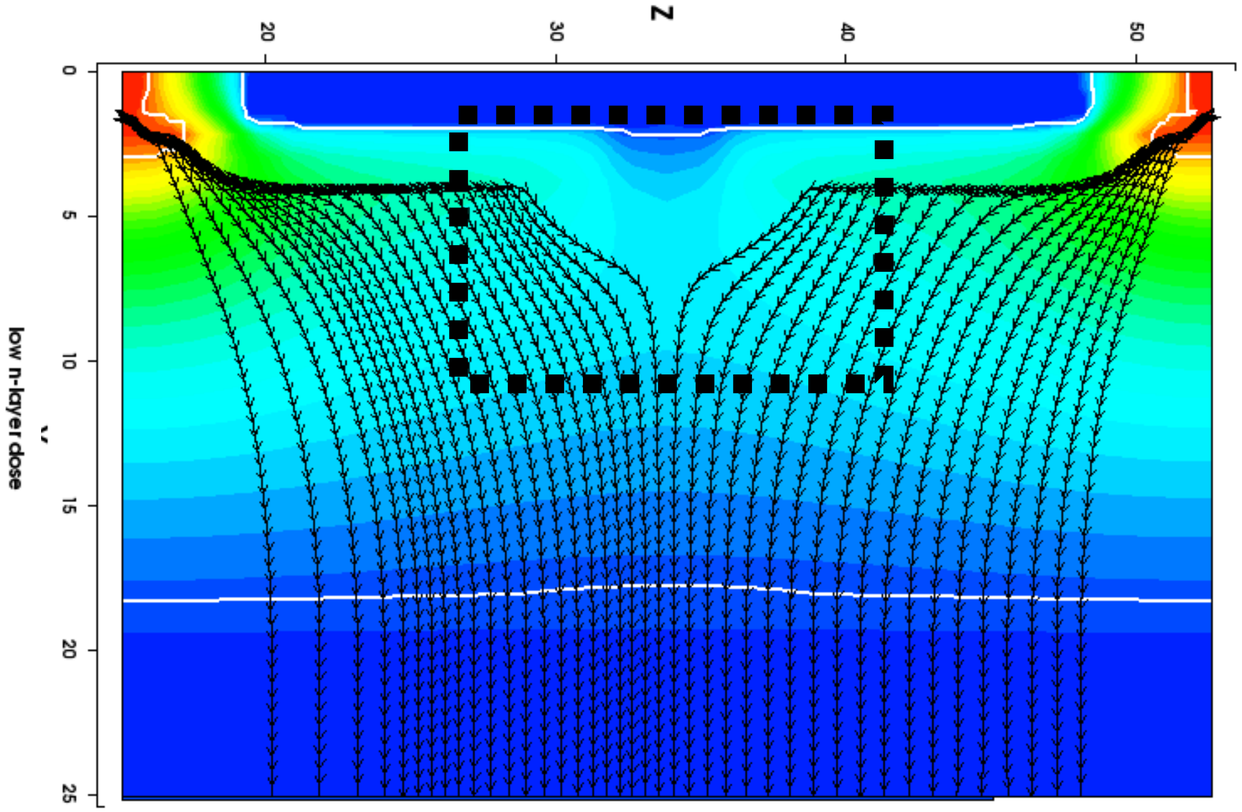
CLICTD - different n-layer doses for gap in n-layer

Lateral field:

Low dose (used for our Investigator studies):



High dose:

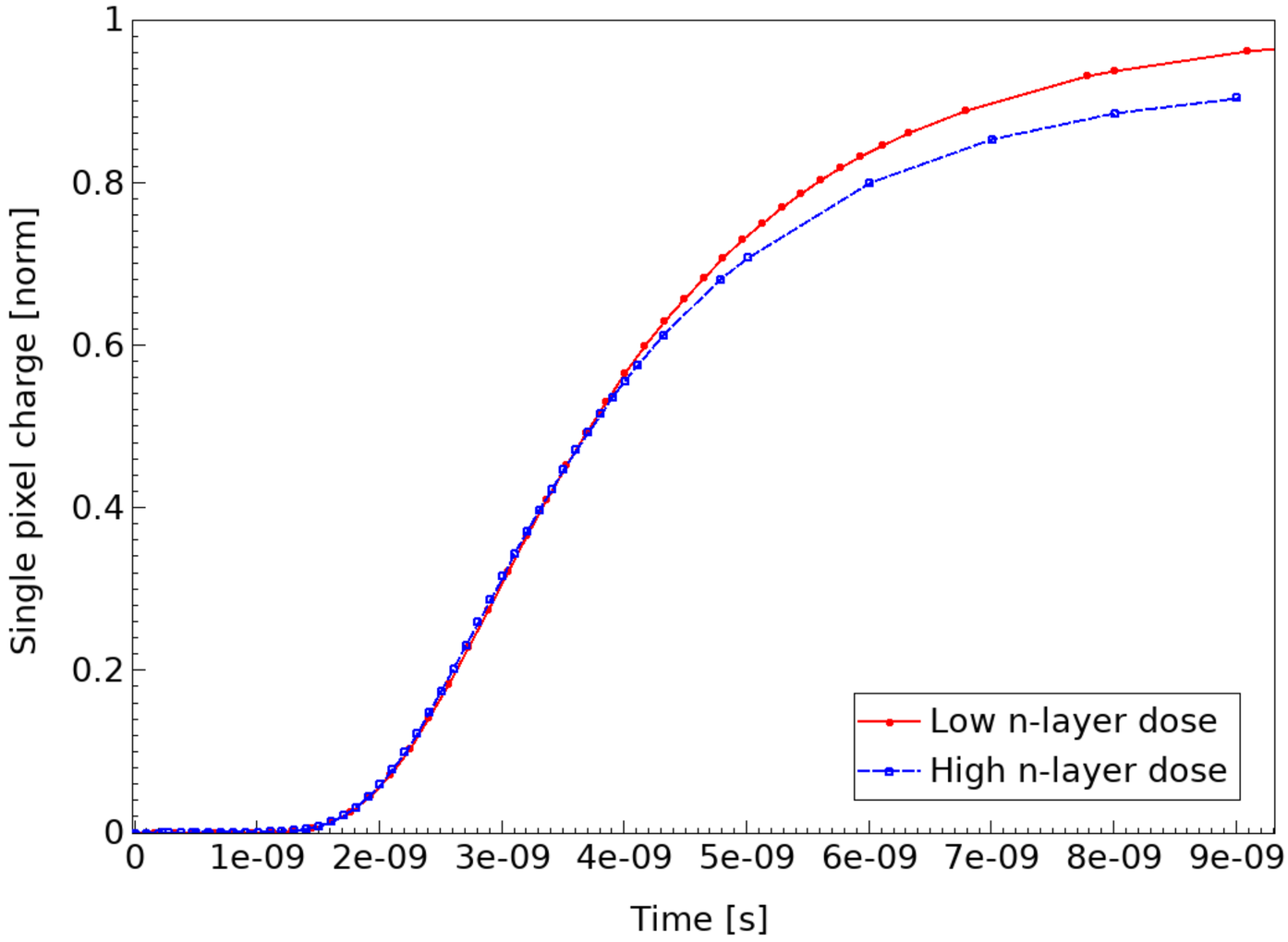


- Slight change of potential

↳ Impact on charge collection in pixel corner?

CLICTD - different n-layer doses for gap in n-layer

Slightly higher lateral electric field - Impact on charge collection in pixel corner:

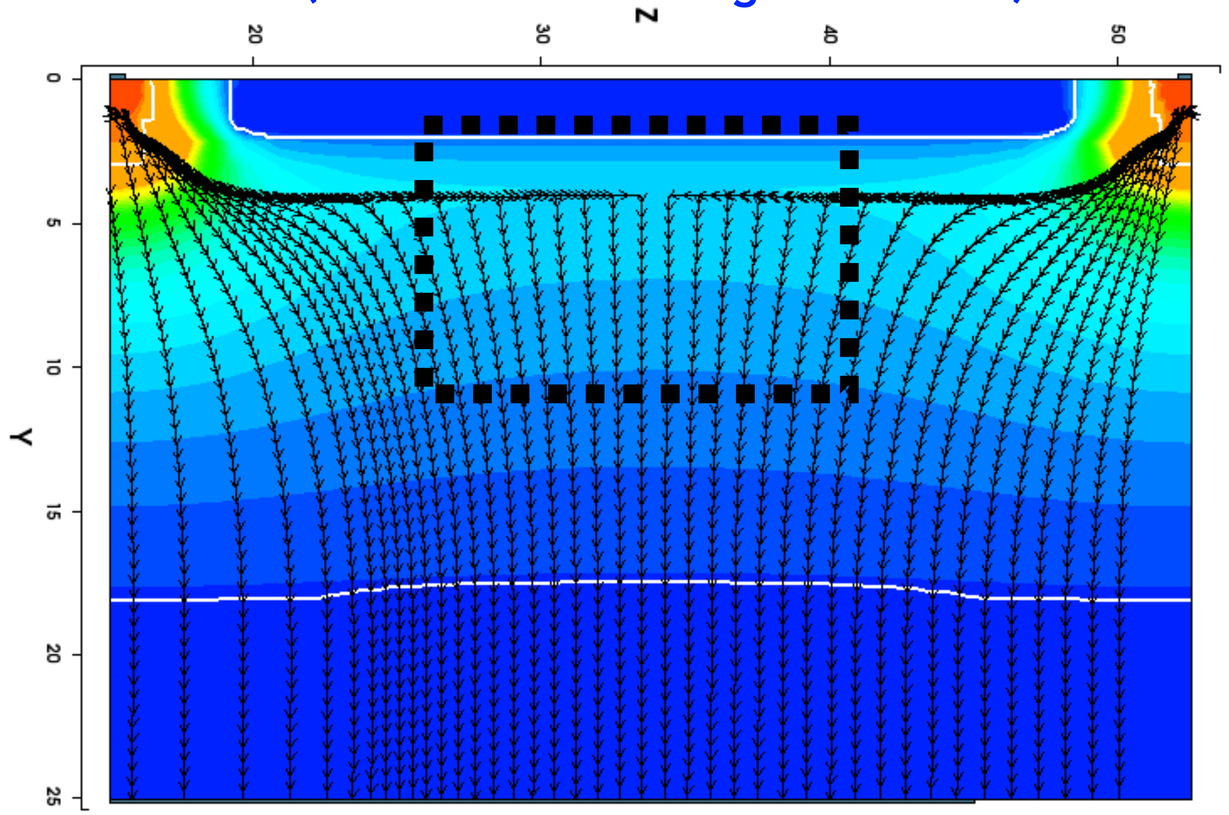


Impact of n-layer dose variations on charge collection time for gap in n-layer process negligible.

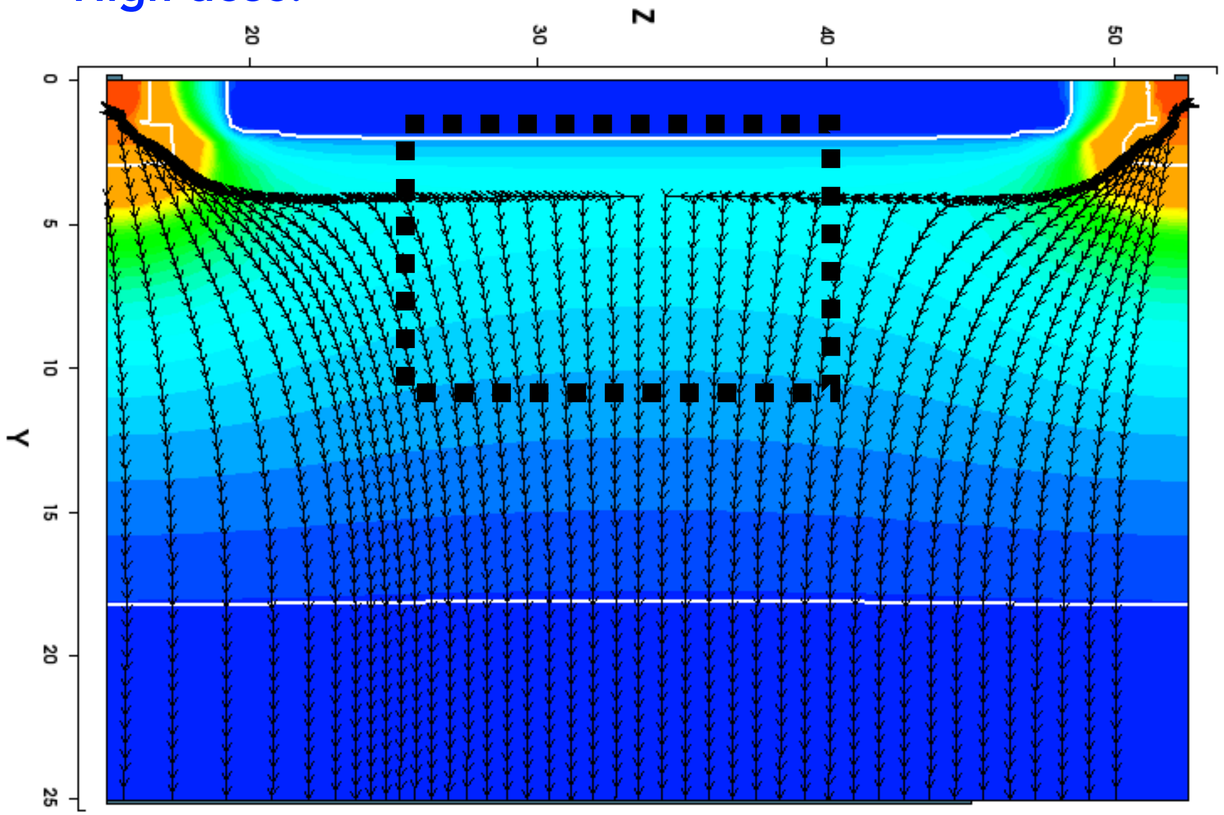
CLICTD - different n-layer doses for modified process

Electrostatic potential:

Low dose (used for our Investigator studies):



High dose:

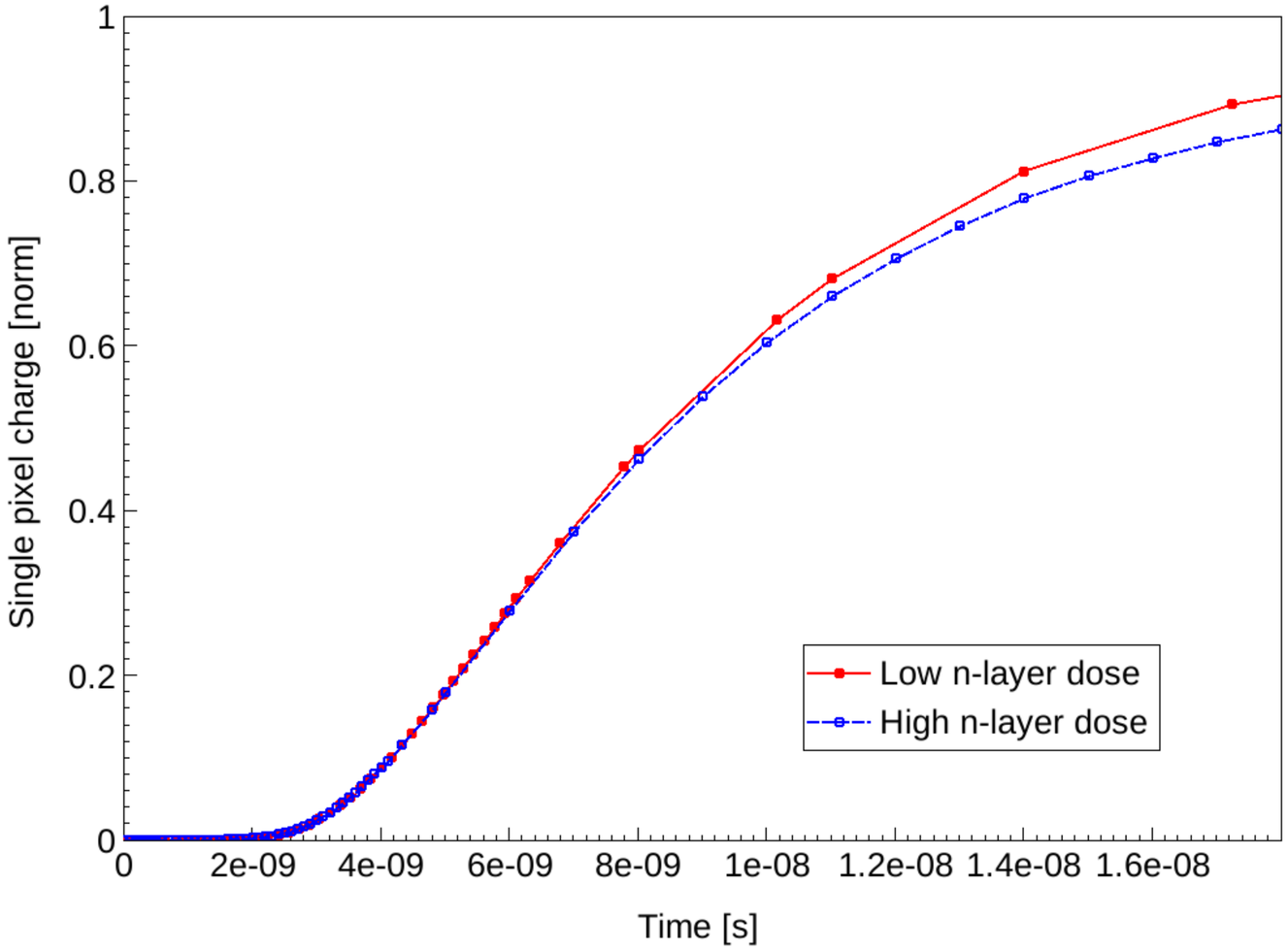


- Slight change of potential

↳ Impact on charge collection in pixel corner?

CLICTD - different n-layer doses for modified process

Slightly higher vertical electric field - Impact on charge collection in pixel corner:



Impact of n-layer dose variations on charge collection time for modified process negligible.

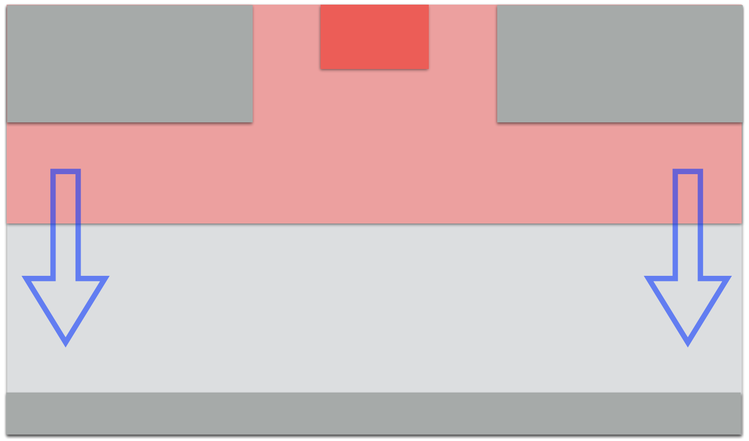
CLICTD - which n-layer dose?

Some further considerations

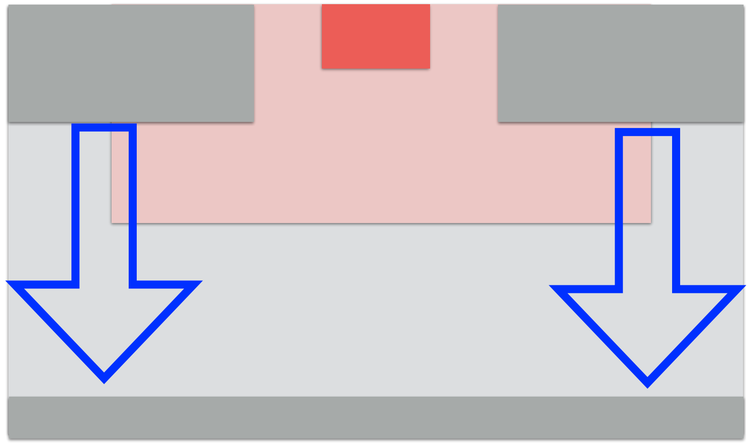
Low dose
(used for our Investigator studies):

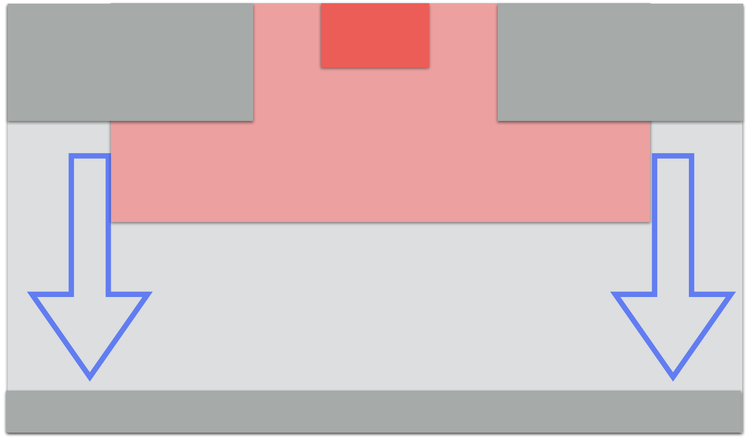
High dose:

Modified process:



Gap in n-layer:



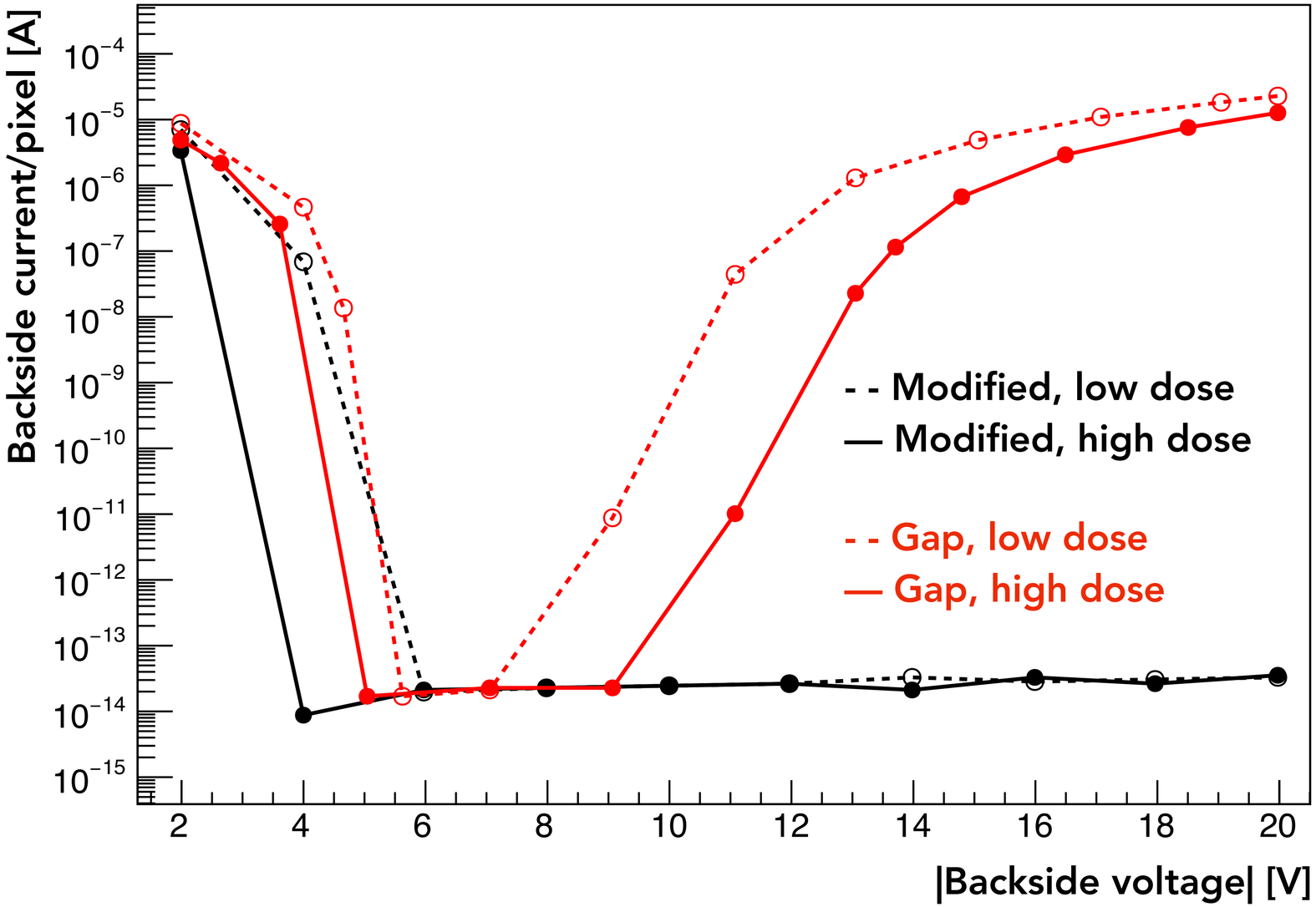


Blue arrows indicate current flow between p-wells and backside at high substrate voltage:

Higher dose:

Better isolation of p-wells from substrate? 🤔

CLICTD - punch through for different n-layer doses



- Better isolation of p-wells from backside voltage for higher n-layer dose
- However, previous simulations indicate that a higher backside voltage is not necessarily good for a faster charge collection in the pixel corners…

Future sensor developments

Thicker sensors *(Heinz Pernegger)*

Motivation:
More signal —> more charge sharing & better radiation tolerance for given threshold

Fabrication:
Use high resistivity Cz wafers instead of epi —> thicker active material

Challenges:
Full depletion —> isolation of p-wells from substrate voltage, especially for new sensor concepts

Question:
If we manage to fully deplete sensor with e.g. additional p-implant, does this modification still improve charge collection?

Thicker sensors

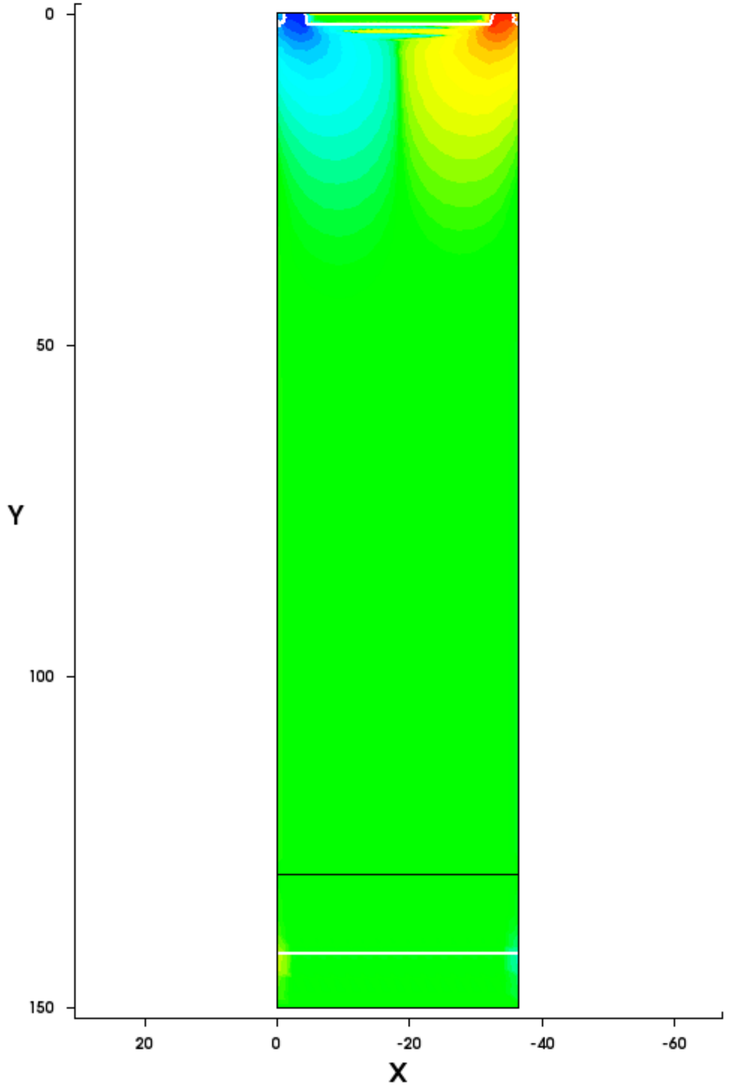
Simulation parameters:

- Simulation for modified process and additional p-implant
- Pixel size of 36.4 um x 36.4 um
- Thickness of 150 um
- Substrate bias of -50 V
- Resistivity ~ 1 kOhm cm

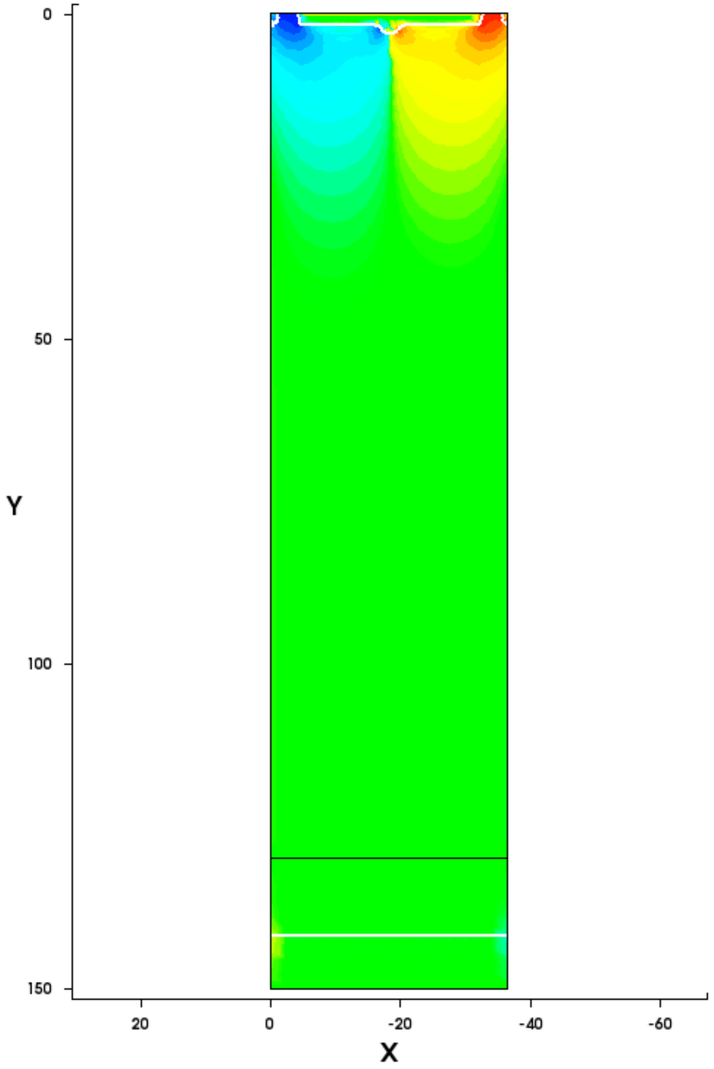
Electrostatic solution

- Full depletion for design with additional p-implant
- Change of lateral field only in very small part of sensor

Lateral field modified process:

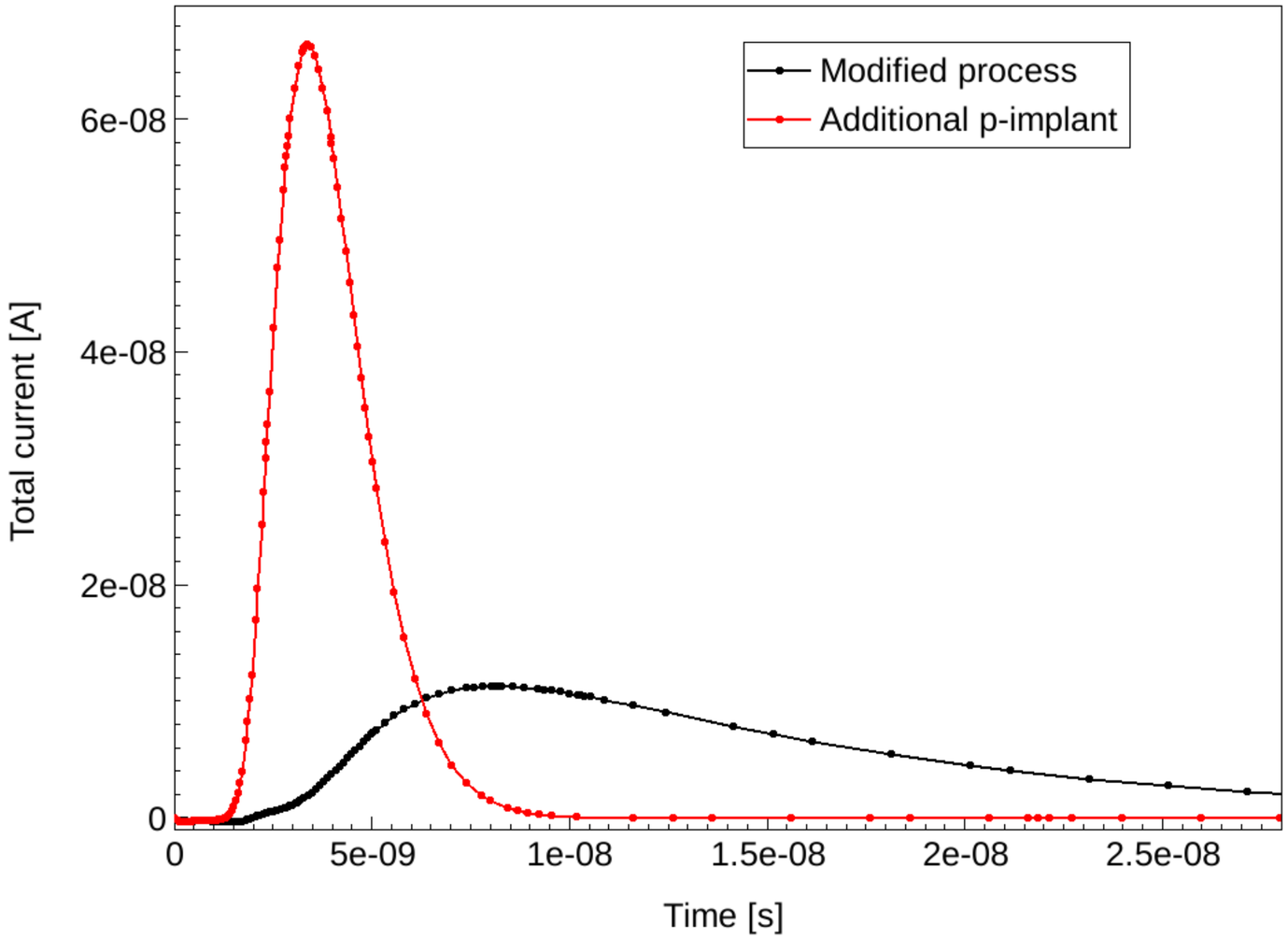


Lateral field additional p-implant:



Thicker sensors

Current pulse for incident at pixel corner:



- Even for 150 um thick sensors the additional p-implants speeds up the charge collection by a few ns

—> Induced current dominated by contribution close to collection electrode

Summary

3d transient TCAD simulations of CMOS sensors with a small collection electrode:

- Answer ***specific design questions for CLICTD***:
  - High n-layer dose allows for higher substrate voltages 😊
  - **High n-layer dose increases capacitance by ~ 30 %** 😢
  - We did not test high n-layer dose so far 😢
  - Transient response very similar 🤔
- Optimise ***underlying general design***
- First measurements of new sensor layouts proposed according to these simulations are currently ongoing

Next steps:

- Simulations of CLICTD for 30 um epi-thickness
- Further optimisation of design for faster charge collection
- Measurements?