Qualification of the data transmission chain of the ATLAS ITk Pixel detector

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The need for a new Inner Tracker (ITk) for ATLAS

- The LHC will be upgraded to the High Luminosity-LHC (HL-LHC).
- This will ensure greater precision measurements in many physics channels
- And allow studies of rare processes

https://cds.cern.ch/record/1419213?ln=en
The need for a new Inner Tracker (ITk) for ATLAS

- Increased data rate
- Therefore we need a faster readout and more storage
- More accumulation of data and need of increased radiation hardness
- Therefore we need finer granularity for high precision tracking
- All silicon inner tracker (ITk) with strips and pixels

Increased Luminosity

HL-LHC simulated 230 pile-up events

https://cds.cern.ch/record/1419213?ln=en

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Validation of the read-out chain for the ITk detector

- Validation of the signal integrity from the sensor front-end to the counting room and vice-versa over the full chain
- Qualification of each part of the data transmission chain
- Improvement of the FELIX software for tuning front-ends
- Validation of the communication between the FELIX system and the ITk front-end chips (RD53).
Validating the Uplink
The Optoboard

**Optoboard** is a PCB populated with:

- **4 GigaBit Cable Receivers (GBCR)** for recovery of uplink signals
- **4 Low Power Giga Bit Transceivers (lpGBT)** for multiplexing and splitting of downlinks
- **1 VTRX+** for electrical/optical conversion

### Electrical

- **Uplink 1.28 Gbps**
- **Flex cable (~1 m)**

### Optical

- **Downlink 160 Mbps**
- **Twinax Cable (~6 m)**
- **Optoboard**
- **Connection**: Electrical → Optical

### Flex Cable Specifications

<table>
<thead>
<tr>
<th>AWG</th>
<th>Width/mm</th>
<th>Height/mm</th>
<th>Mass (kg/km)</th>
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<tbody>
<tr>
<td>34</td>
<td>1.12</td>
<td>0.64</td>
<td>1.1</td>
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</tbody>
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Testing inner part of the data transmission chain: The Set-up

2 GHz oscilloscope

Flex

TWINAX AWG 34

CDR (Clock Data Recovery Chip) of RD53B FE

BDAQ (Sends commands to the CDR)

Arduino

GBCR testboard
Schematic representation of the set-up

- Validation of the uplink signal integrity through jitter analysis tests

Devices under test

For configuring and sending commands

PCs

Oscilloscope (2 GHz, 10 Gs/s) → GBCR v1 → Arduino → PC (To communicate via I2C to GBCR)

PC (To communicate to CDR via BDAQ) → CDR RD53B → BDAQ

TWINAX AWG 34

Stave Flex (L3 AX-ISF)
What is jitter?

Signal is digital: series of 0s and 1s
Data rate 1.28 Gbps i.e 640 MHz clock

Schematic of ideal clock and signal:

Clock

Data

~ 780 ps

Voltage (mV)

Time (ps)

Very low jitter
Large jitter
Eye closed
Results from the jitter analysis tests

- CDR
  - TJ = 100.89 ps

- CDR + Flex
  - TJ = 275.75 ps

- CDR + Flex + Twinax
  - TJ = 263.87 ps

- No pre-emphasis

- Pre-emphasis

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Configuring FEs using Downlink
The Front-End Link eXchange (FELIX) Read-out system

- New detector readout component being developed as the interface between the data acquisition system and the trigger and detector front-end electronics.
- Sends commands, timing and trigger information to the front-end electronics through downlink channels.
- Receives data through uplink channels from the detector front-end electronics.

VHDCI: A Very High Density Cable Interconnect, GBTX: 2 GigaBit Transceivers + 1 VTRx+, implements multipurpose high speed bidirectional optical links, SFP: Small from Pluggable for optical cables.
Tuning FEs using FELIX
Threshold Tuning

- Initial Scan
- After Global Threshold Tuning
- After Pixel Threshold Tuning

Thr 3234 e → Thr 2981 e → Thr 3104 e

The mean value shifts closer to target threshold 3000 e
The width of the distribution decreases

Time Over Threshold Tuning

- Initial Scan
- After Global Preamp Tuning
- After Pixel Preamp Tuning

Tot 8.1
Tot 10.31
Tot 9.94

The mean value shifts closer to target Tot 10
Most of the pixels are tuned to the target Tot

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• Successfully set up the two separate set-ups to test the uplink signal integrity and the downlink from FELIX to tune Fes
• Configuration of CDR, GBCR and the FEI4 Fes using their respective software
• Tests are still ongoing to obtain lower jitter in the inner part of the data transmission chain and optimization of related configuration parameters of the CDR and GBCR
• Parts of this chain will be irradiated and will require more testing before and after irradiation
• Successfully able to perform the complete tuning on single FEI4 front-end chip at Bern and on a multi-chip system at CERN.
• The work on FELIX is ongoing and will culminate in integration with the inner part of the transmission chain
• Bern will have a prototype of a fully functioning data transmission chain as in the ITk
Back-up
The Optoboard
• A Twinax is a dual coaxial cable with a common shield ("Extension" of TWP).
• Currently Cu wire (later CCAI), low density polyethylene dielectric, Al foil shield, PU or polyester jacket.

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<tr>
<td>34</td>
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</table>
Next cable run will have polyimide shield with the same jacket
Relation between Threshold and TOT

Charge Q

Voltage V

Threshold Value

TOT

Time t
Testing inner part of the data transmission chain: The Set-up

- Validation of the uplink signal integrity through jitter analysis tests
Oscilloscope (2 GHz, 10 Gs/s)

PC (To communicate via I2C to GBCR)

PC (To communicate to CDR via BDAQ)

GBCR v1

Arduino

CDR RD53B

BDAQ

Stave Flex (L3 AX-ISF)

TWINAX AWG 34
Tuning FEs using FELIX

- Selecting the masking pattern
- The scans to tune the FE
- Commands to run a tuning procedure
- The configuration files of the FEs to be tuned

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Tuning FEs using FELIX

Check threshold before and after tuning

Check TOT before and after tuning

Digital Scan Checks pixel response

Analog Scan Checks pixel response

Global Threshold Tune Global threshold tuned

In pixel threshold adjusted

Global TOT Tune Global TOT tuned

In pixel TOT adjusted

Pixel Preamp Tune Noise Masking of noisy pixels

Threshold

TOT
Pre-emphasis

gradient input current

eddy currents

distorted by eddy currents

input current with pre-emphasis modification

desired gradient output
Working point

• General:
  • The TWINAX AWG34 cable is 6 m long and the L3 A X- ISF stave flex is 1 m long
  • The differential signal of the DAQ1 on the stave flex was tested

• CDR chip of RD53B:
  • Input command of PRBS 5 from FPGA, AC coupled to chip (I’m using the setup as described in https://gitlab.cern.ch/prymasze/cdr53bdaq/wikis/home - permission required for access)
  • Differential signal from GTX_NEW SMA (PRBS15, 1.28 Gbps) used for testing
  • Oscilloscope input terminated at 50 Ω
  • Current consumption between 47 mA to 66 mA (varies when the CDR is connected to other devices or if it is directly connected to the oscilloscope)
  • Settings in the CDR53BDaq software programme:
    • SEL_CMD_PATTERN = 5 (to have PRBS5 input)
    • SER_SEL_OUT_NEW = 1 and LFSR_SEL = 0 (to have PRBS15 in output)
    • EN_GTX_NEW = 1, SER_EN_TAP = 1, SER_INV_TAP = 1, DAC_CML_BIAS_1 = 1023, DAC_CML_BIAS_2 = 500, DAC_CML_BIAS_3 = 0 (with pre-emphasis)
    • EN_GTX_NEW = 0, SER_EN_TAP = 0, SER_INV_TAP = 0, DAC_CML_BIAS_1 = 500, DAC_CML_BIAS_2 = 0, DAC_CML_BIAS_3 = 0 (without pre-emphasis)
  • The powering in this test is different to the set up used in Bonn so the part of the software has been commented out
Working point cont.

• GBCR v1:
  • Arduino DUE used to initialise and configure the GBCR using the I2C protocol
  • The bit AFCcalSrc in Register 0 (used to choose the clock) is set to internal clock from PRBS signal
  • The Equaliser settings are optimal i.e EquSC = 3b’011 and EquSR = 4b’0000 (recommended by SMU)
  • The CDR of the GBCR is enabled, Decision Feedback Equaliser (DFE) of the GBCR is disabled and tests are conducted using Channel 4
  • GBCR is powered using DCDC converter (FEAST 1.2V module)
  • Though the design frequency is 5.12 Gbps, tests are conducted at 1.28 Gbps as per the uplink requirements

• Oscilloscope settings:
  • Bandwidth 2 GHz
  • Sample rate 10 Gs/s
  • Trigger mode Normal
  • Acquisition HiRes and Roll mode off
  • Channel Math 1 = Channel 1 – Channel 2
  • Signal type Data
  • Clock Recovery – PLL Standard or Constant Clock Mean (set while One Touch Jitter auto references before measurement) and bit rate set to “Auto” instead of specifying 1.28 Gbps
The present centre of mass energy for pp collisions is $\sqrt{s} = 13$ TeV with a peak instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in the current running in 2018. The quantity that measures the ability of a particle accelerator to produce the required number of interactions is called the luminosity and is the proportionality factor between the number of events per second and the cross section. The number of interactions per second is the instantaneous luminosity. However the final figure of merit is the so-called integrated luminosity as it directly relates to the number of observed events. For a given physics process with a cross-section $\sigma_{\text{process}}$, the number of events $N_{\text{event}}$ occurring is given by [14],

$$N_{\text{event}} = L\sigma_{\text{process}}$$  \hspace{1cm} (1.2)

where $L$ is the integrated luminosity.