New developments in silicon pixel detectors

Daniela Bortoletto

Vertex Detectors for e+e- Colliders

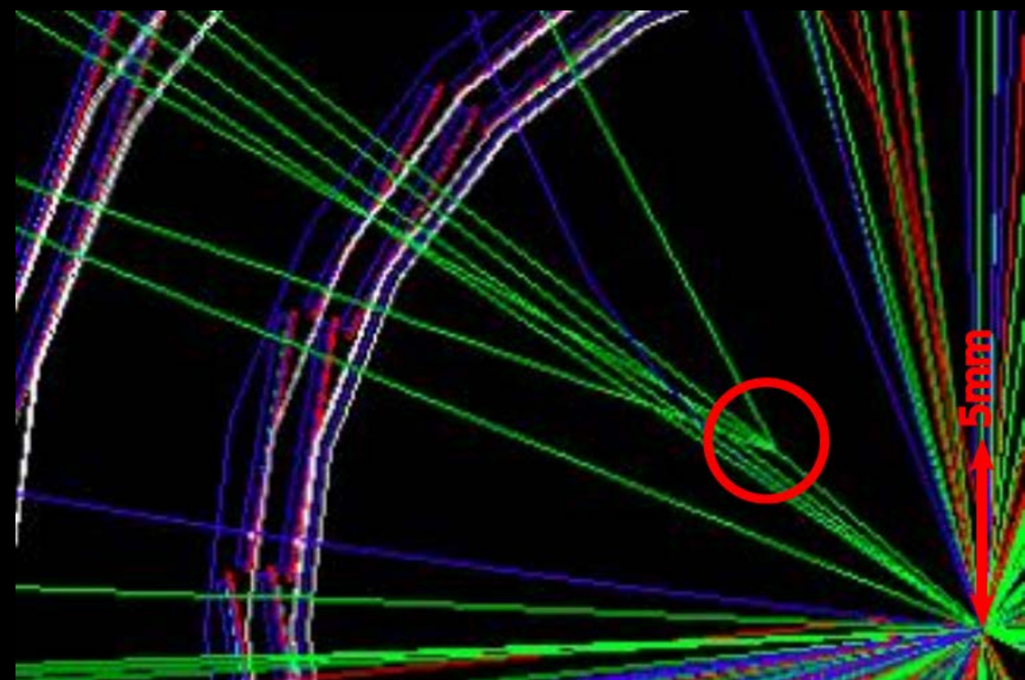
- Efficient tagging of heavy quarks through precise determination of displaced vertices required for many physics goals

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \sim 5\ \mu m,\ \ b \sim 15\ \mu m$$

- Good single point resolution: σ_{SP}~3 μm
  - Small pixels <~25x25 μm^2, analog readout
- Low material budget: X $\lessapprox$ 0.2% X_0 / layer
  - Corresponds to ~200 μm Si, including supports, cables, cooling
  - Low-power ASICs (~50 mW/cm^2)

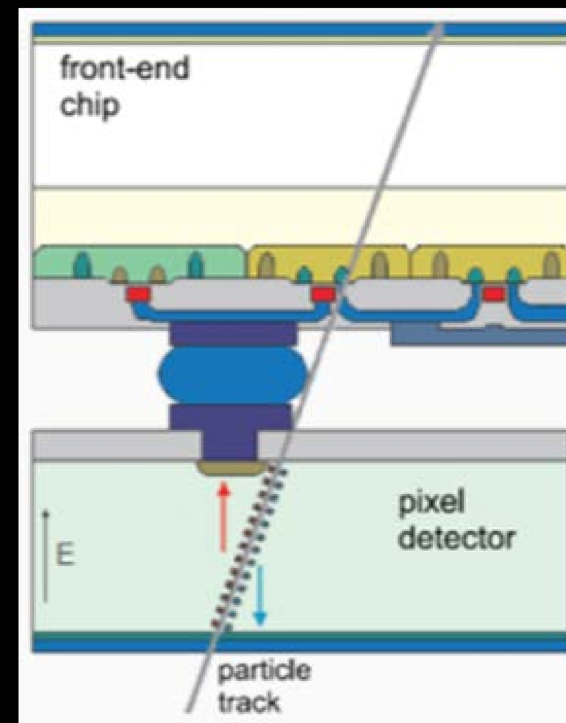
Excellent impact parameter resolution for c/b-tagging

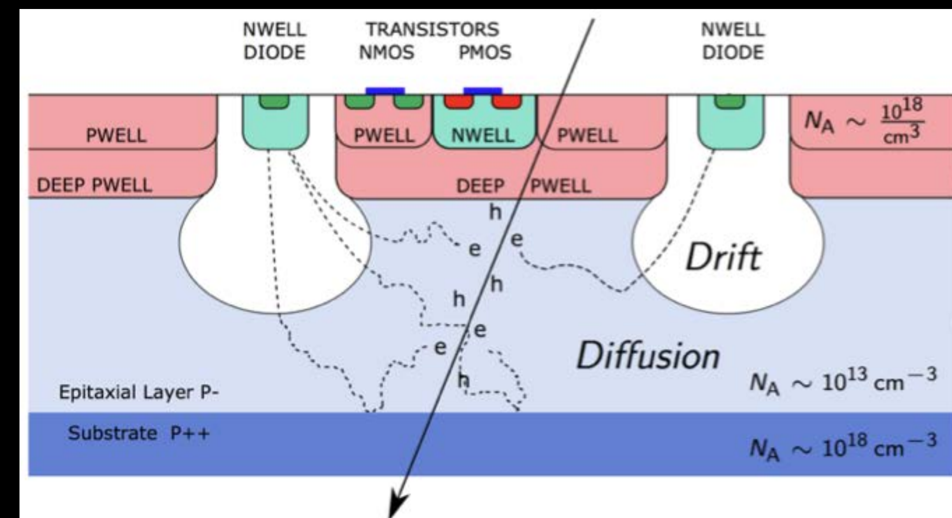


Pixel Detectors

- Hybrid Pixel sensors
- Monolithic active pixel sensors (MAPS)
  - Sensor and readout electronic on the same wafer
  - Charge collection by diffusion
  - Low material
  - Low cost
- Fully Depleted CMOS technology (DMAPS)
  - Fast Charge collection by drift (<10 ns)
  - High radiation tolerance
  - Good SNR
- Silicon on insulator
- Vertically integrated pixels ("3D")

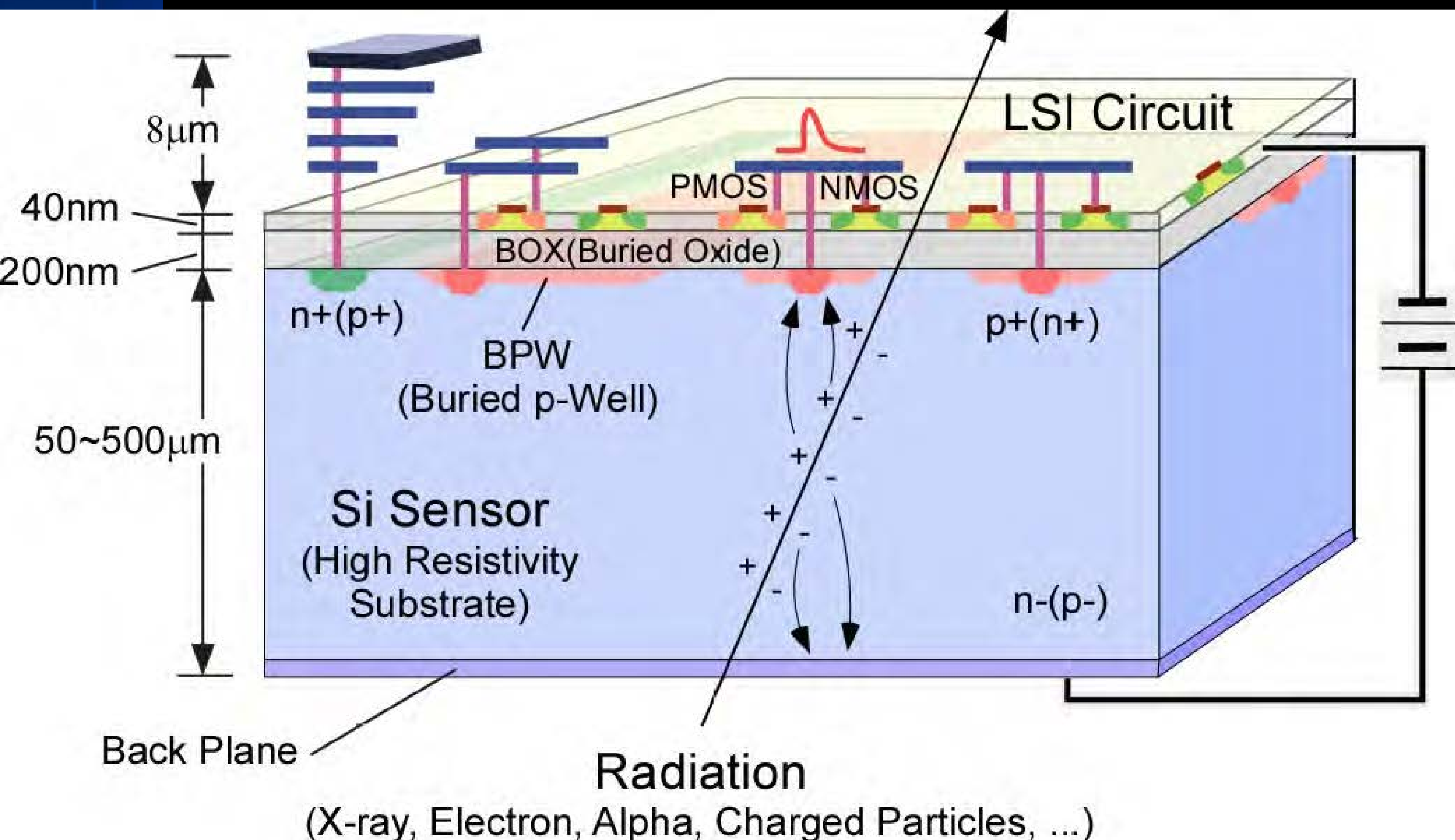
$$d \propto \sqrt{\rho V}$$





3D Integrated Silicon on Insulator

Yasuo Arai



- Features of SOI Pixel Detector
  - High Resistive fully depleted sensor (50 μm~700 μm thick) with low capacitance ➟Large S/N.
  - Full CMOS processing
  - Can be operated in wide temperature (1 K-570 K) range.
  - Based on Industry Standard Technology.

- SOI pixel technology provides Monolithic Detectors with fine resolution and high functionality CMOS .

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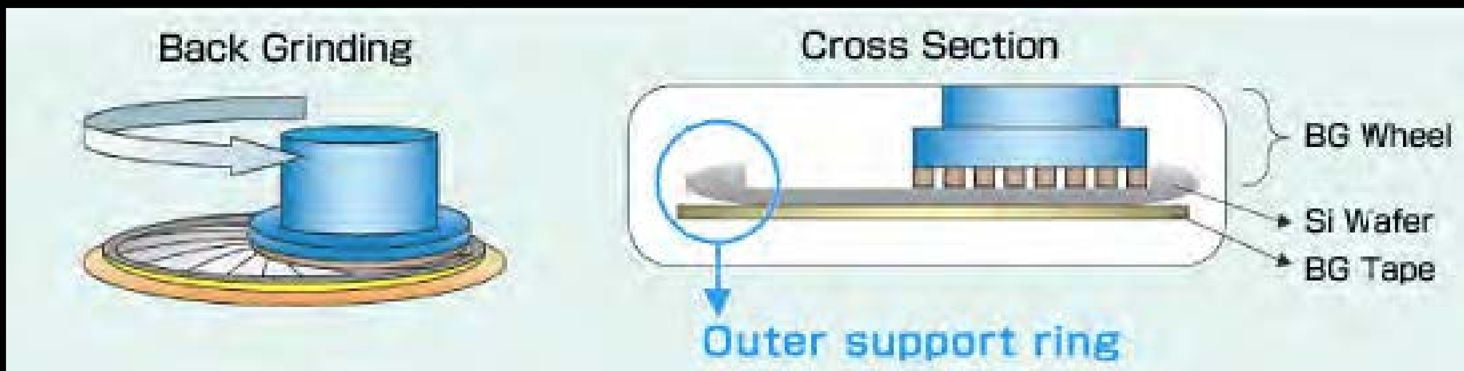
Lapis Semi. Co., Ltd 0.2 μm FD-SOI Pixel Process

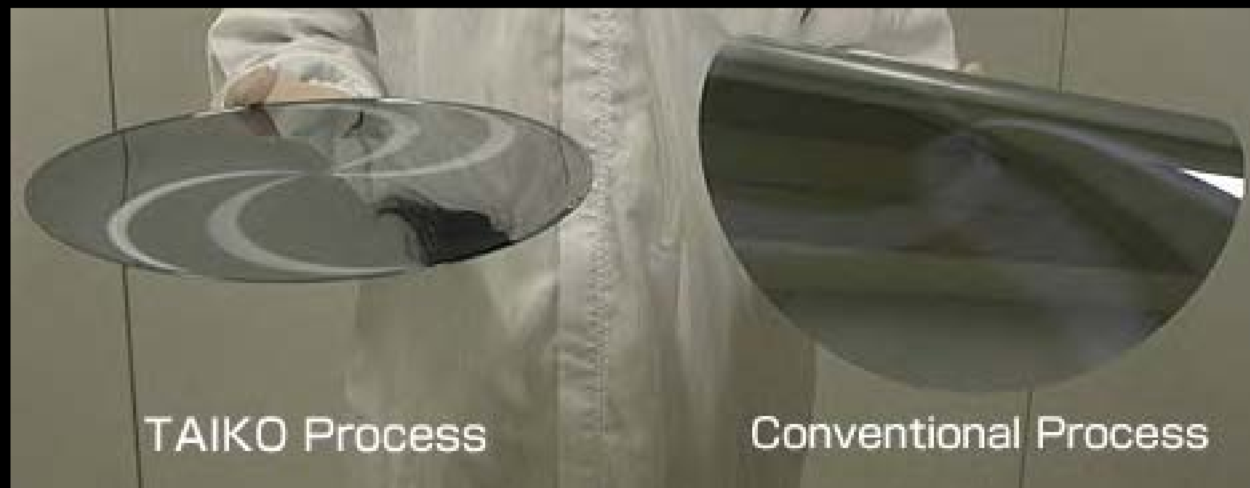
Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

8

Wafer Thinning

- With outer support ring
  - Lower wafer warpage
  - Improve wafer strength
  - Easy wafer handling
  - Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning

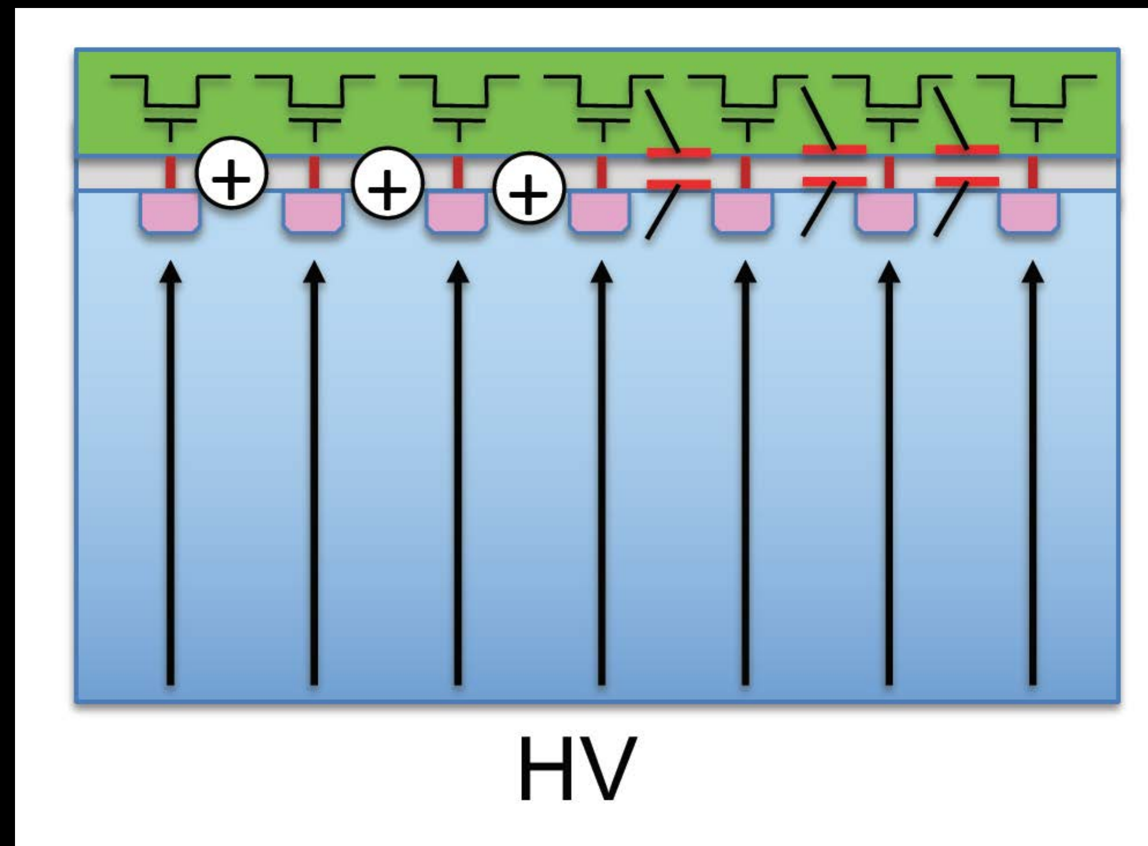




Successful thinning of SOI wafers down to ~75 μm

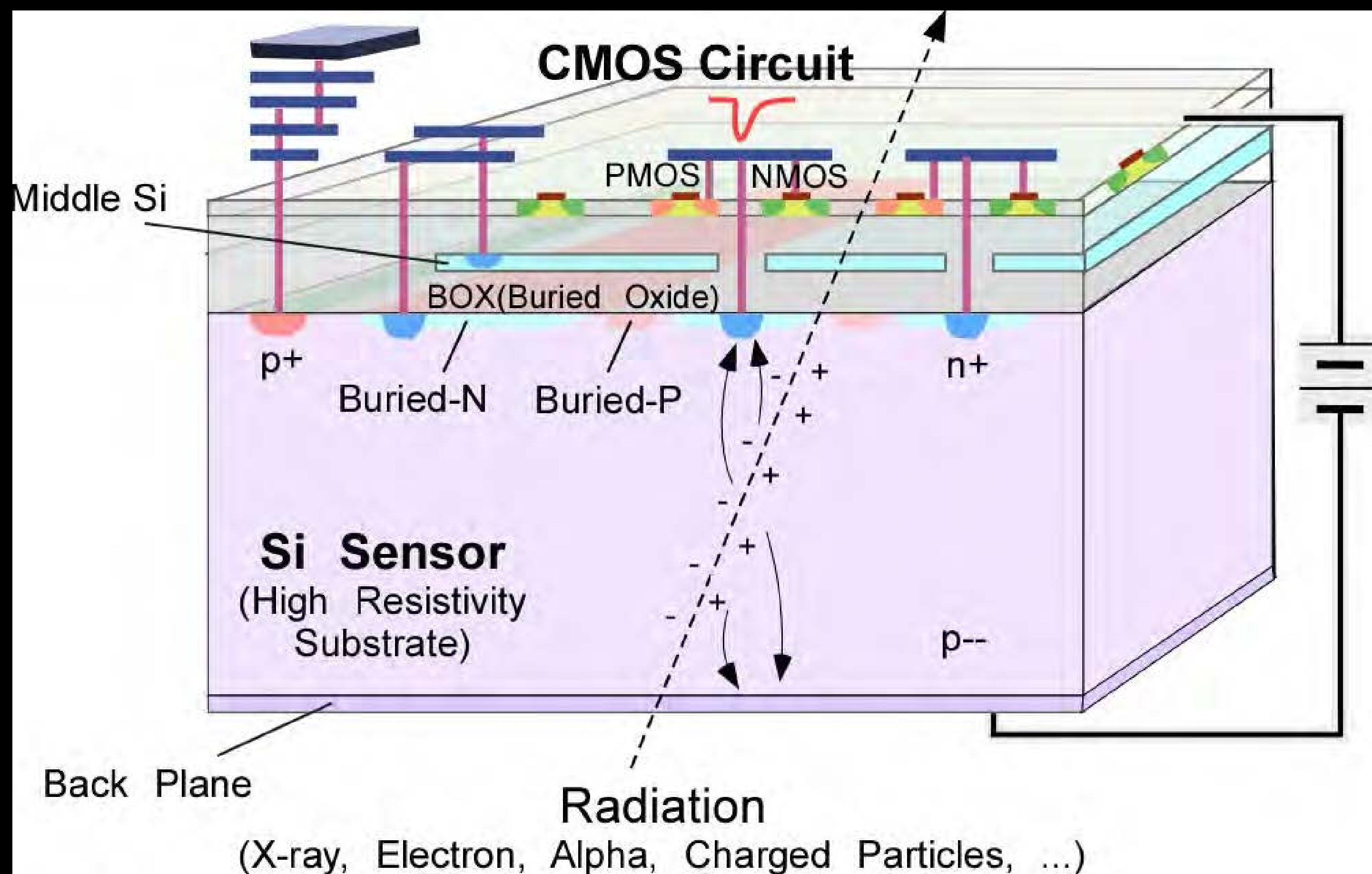
Issues with SOI

- CMOS electronics affected by Detector High Voltage. (Back-Gate Effect)
- Coupling between Circuit signal and sense node. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)



Double SOI Detector

- Middle Si layer shields coupling between sensor and circuit.
- It compensate E-field generated by radiation trapped holes.
- Can be used in High radiation environment.
- DSOI is not a standard process
  - Small number of produced wafers
  - Process issues (void, bending,,,)
  - Long delivery time



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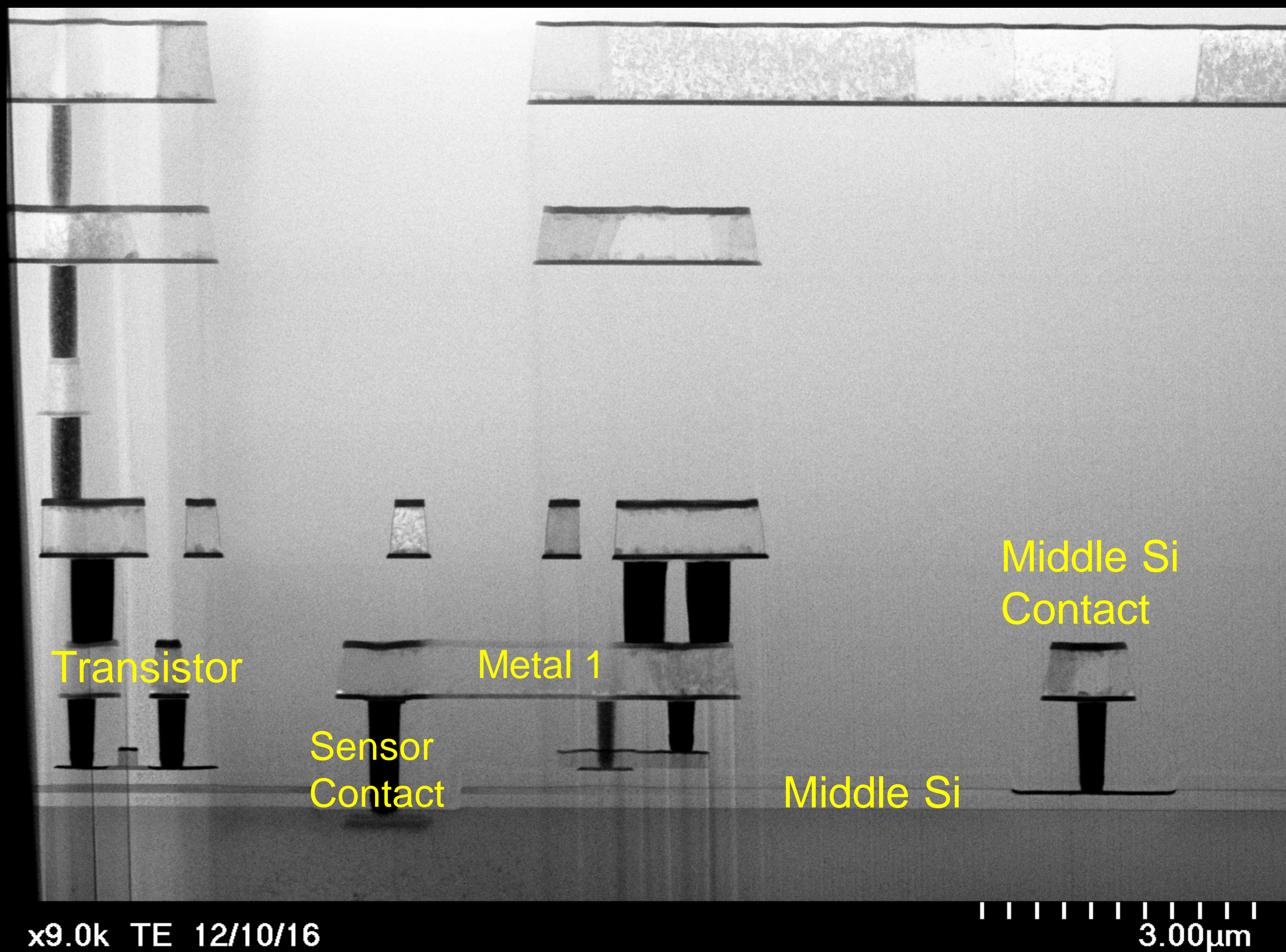
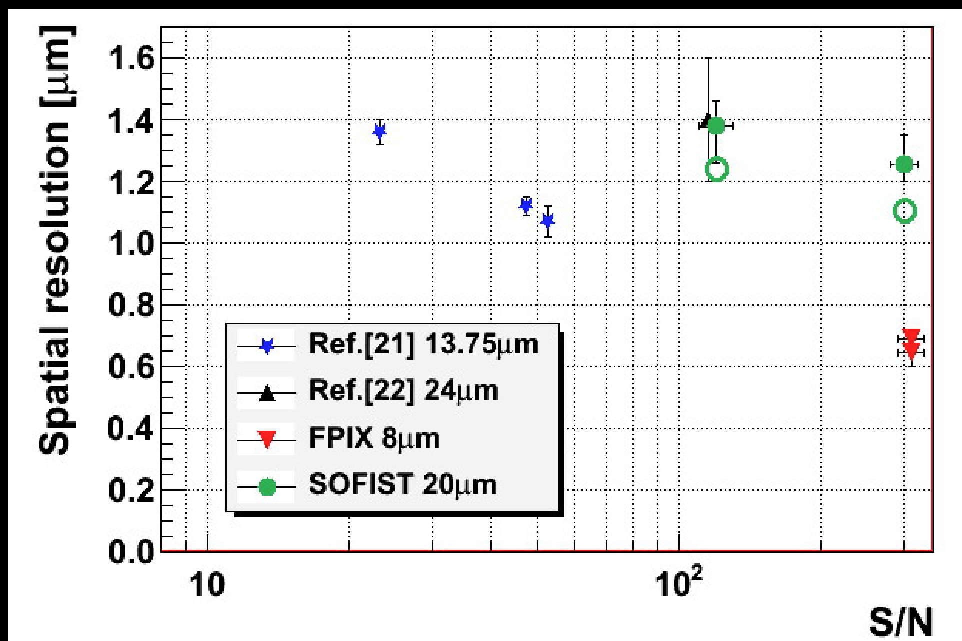
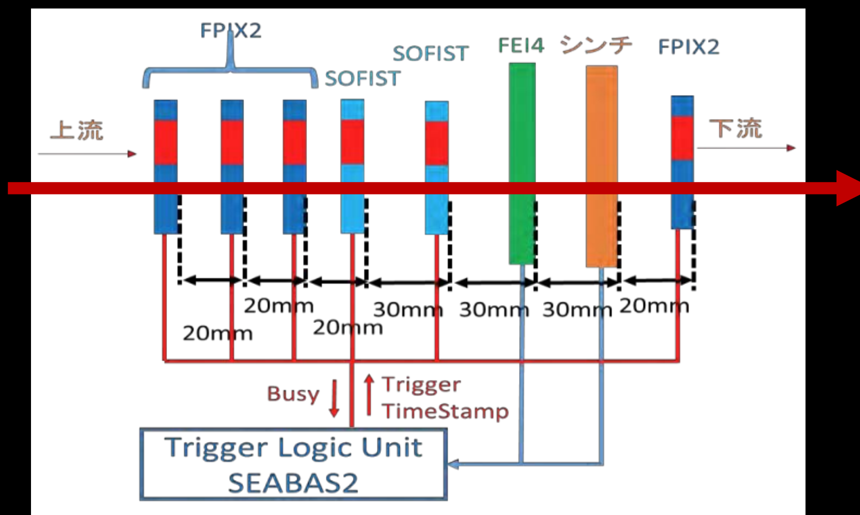


Studies for ILC

- Two kinds of SOIPIX-DSOI detectors used:
  - FPIX2 x 4: 8 μm square pixel detector
  - SOFIST(v.1 & 2) x 2: 20 μm square pixel detector
- Beam tests at FNAL with 120 GeV Protons



(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)



Less than 1 μm Position Resolution for high-energy charged particle is achieved

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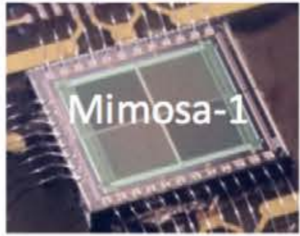
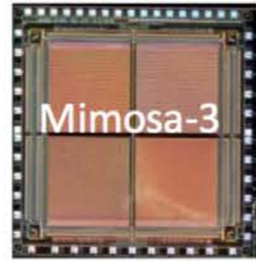
Monolithic Pixel Detector Evolution

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)





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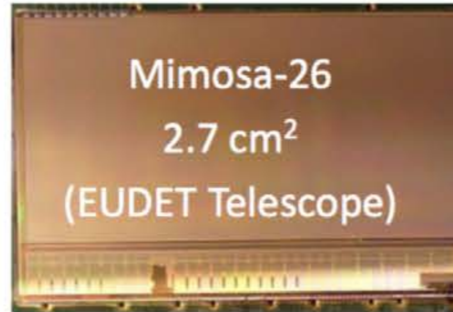
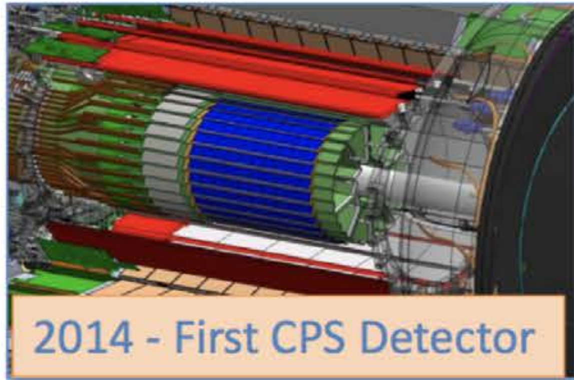
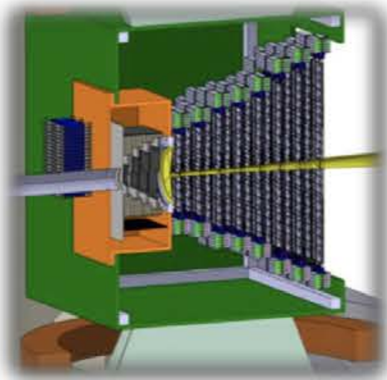


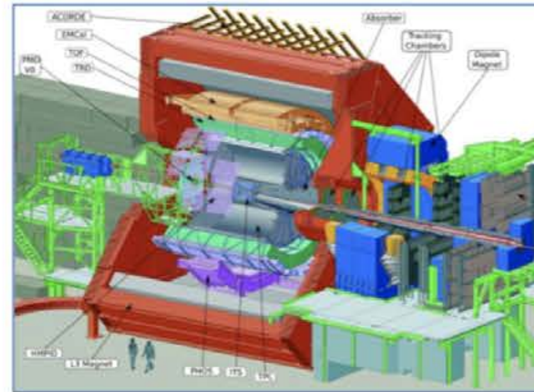
... several HI experiments have selected CMOS pixel sensors for their inner trackers



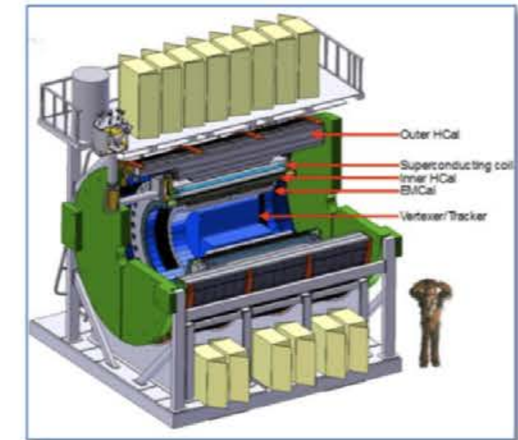
STAR HFT
$0.16\ m^2$ – 356 M pixels



CBM MVD
$0.08\ m^2$ – 146 M pixel



ALICE ITS Upgrade (and MFT)
$10\ m^2$ – 12 G pixel

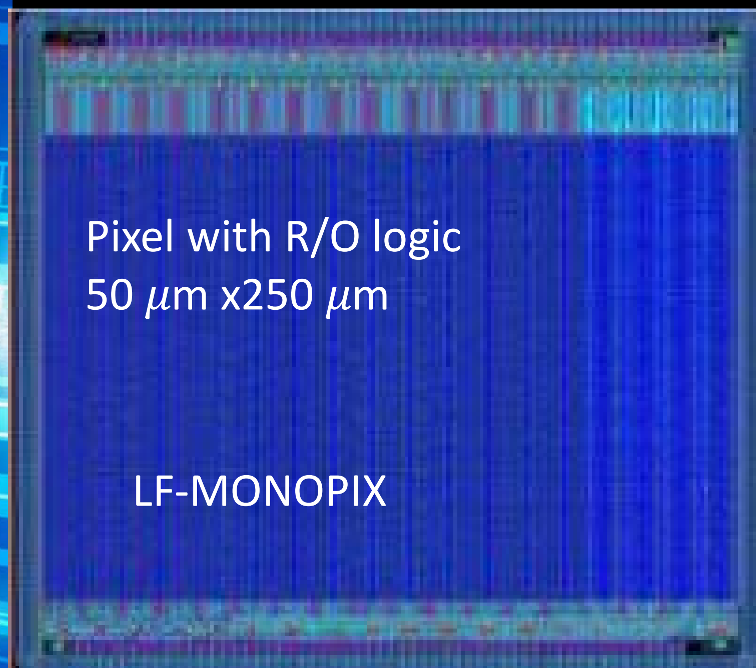


sPHENIX
$0.2\ m^2$ – 251 M pixel

ATLAS CMOS DEMONSTRATOR PROGRAM

WITH SEVERAL FOUNDRIES

LFOUNDRY



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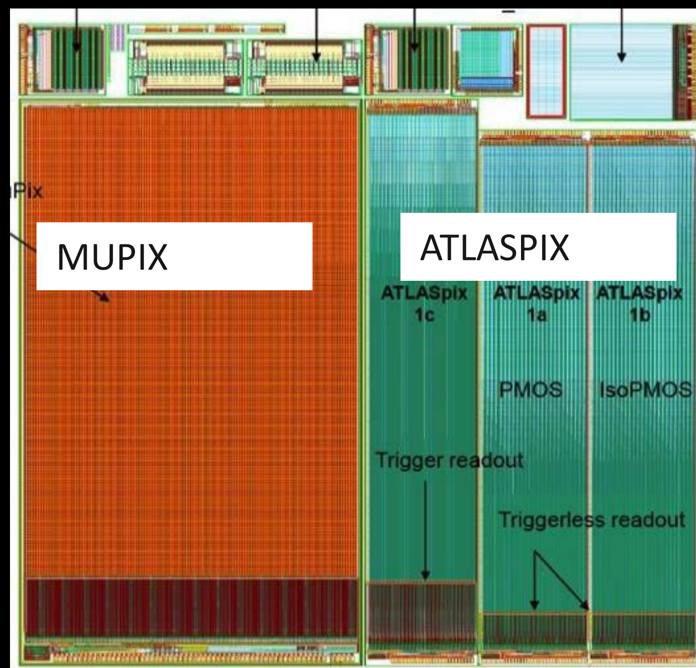
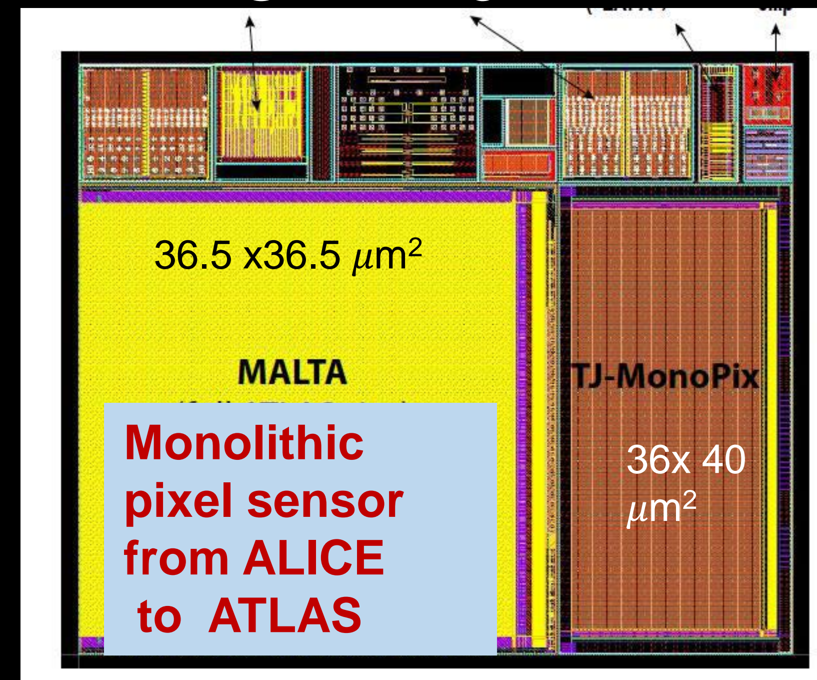


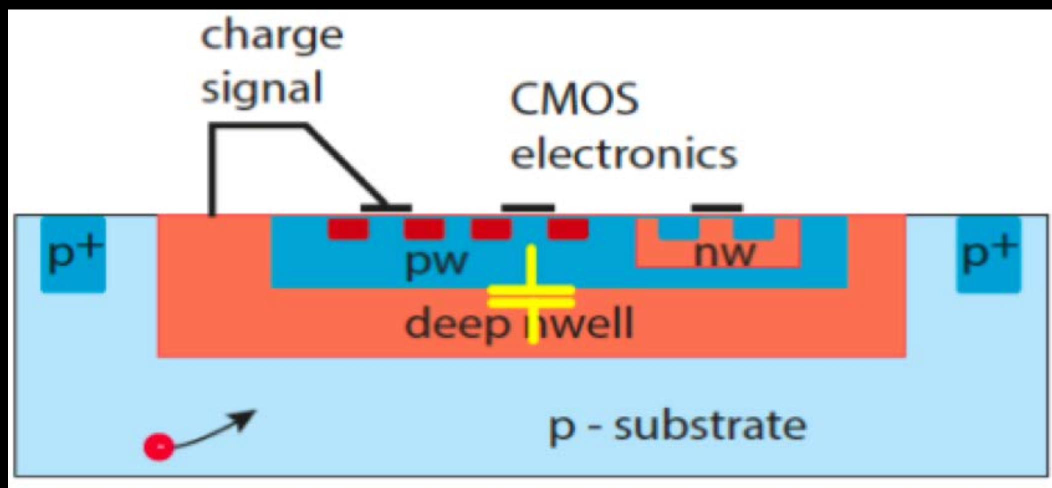
TOWERJAZZ



DMAPS development important for LHCb upgrade II, CepC, CLIC, ILC, FCC-ee and FCC-hh

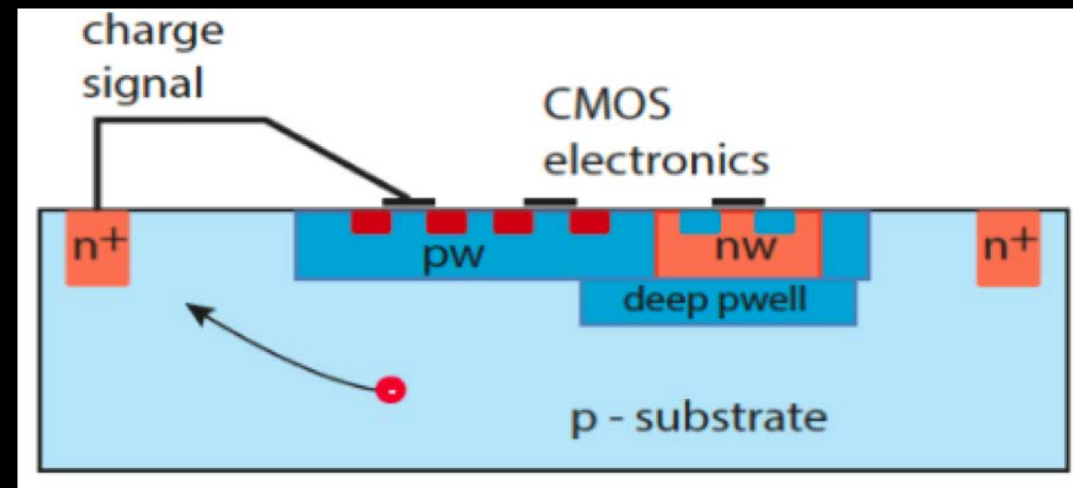
CMOS Design Choices

- Large electrodes



- Electronics in collection well
- No or little low field regions & short drift path ➠ High radiation hardness
- Large(r) sensor capacitance ➠higher noise and slower @ given power
- Potential cross talk between analog and digital sections

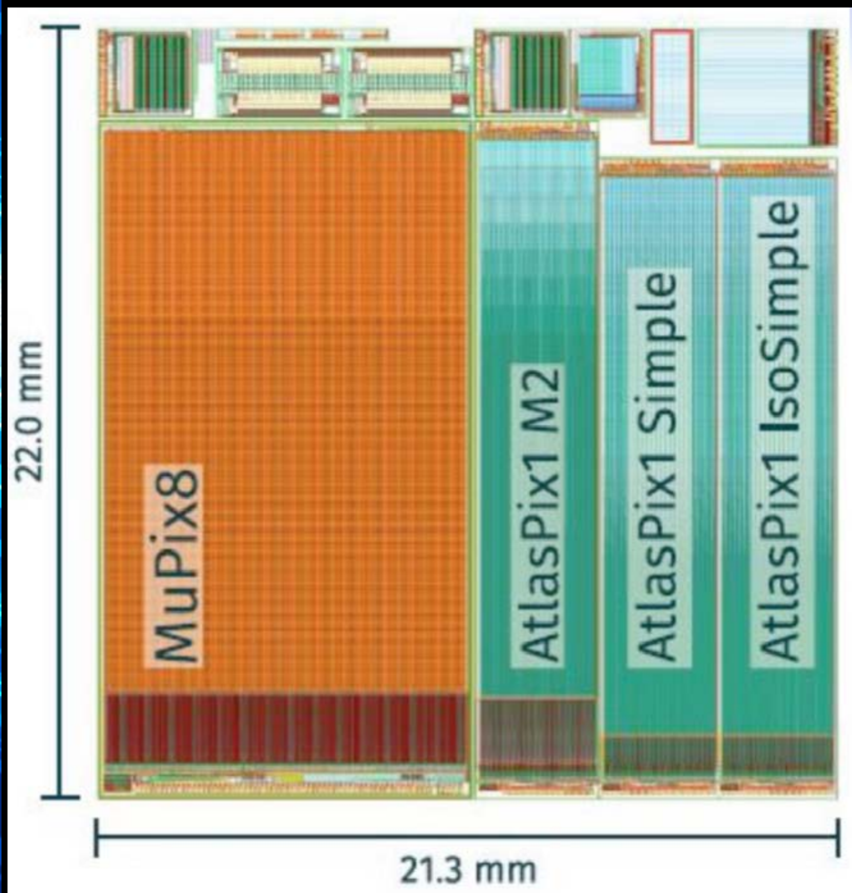
- Small electrodes



- Electronics outside collection well
- Large drift path ➠ need process modification to standard CMOS processes for radiation hardness
- Small capacitance for high SNR and fast signals
- Separate analog and digital electronics

HVCMOS AMS 180nm

- Developments for ATLAS and mu3e using different HR substrates 80/200 Ωcm



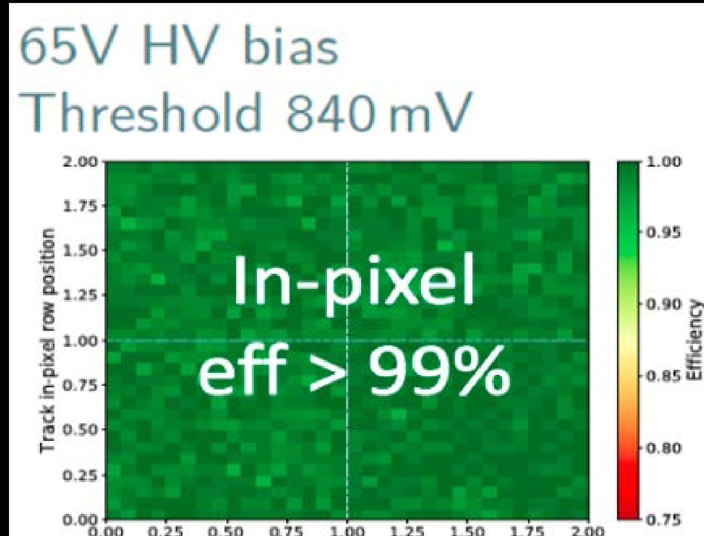
ATLASPix1 M2

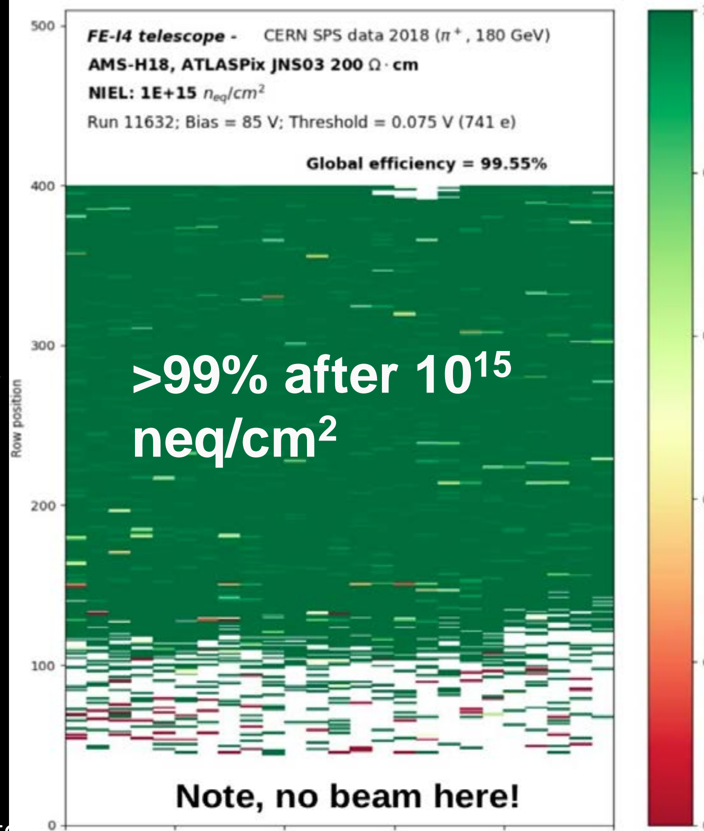
- 320 X 56 pixel Matrix
- 50x60 μm^2 pixel Size
- triggered readout

ATLASPix1 Simple

- 400x25 pixel matrix
- 40x130 μm^2 pixel size
- asynchronous

Readout of signal to periphery with "column drain"-type buffer/ToT in periphery

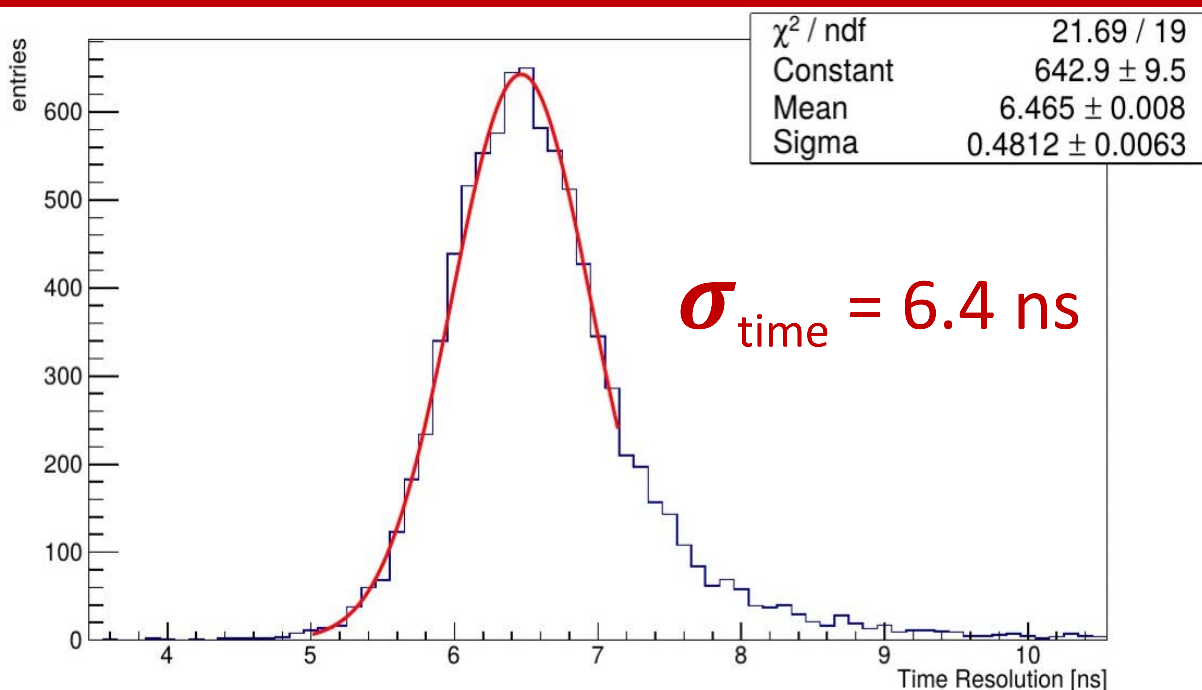




HVCMOS AMS 180nm

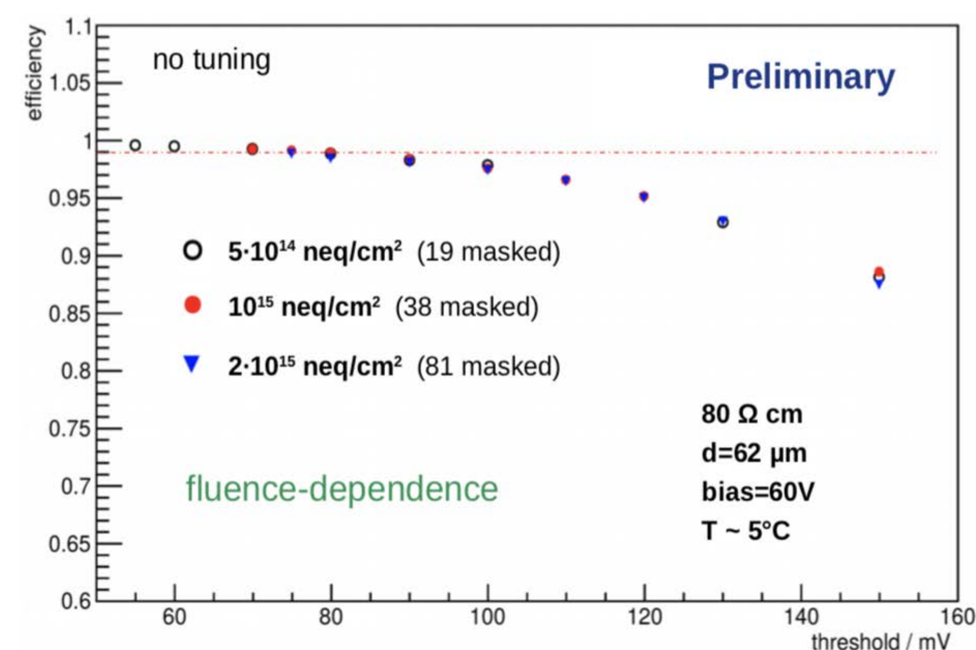
- Developments for ATLAS and mu3e using different HR substrates 80/200Ωcm

Time resolution with time walk correction



σ_{time} = 6.4 ns

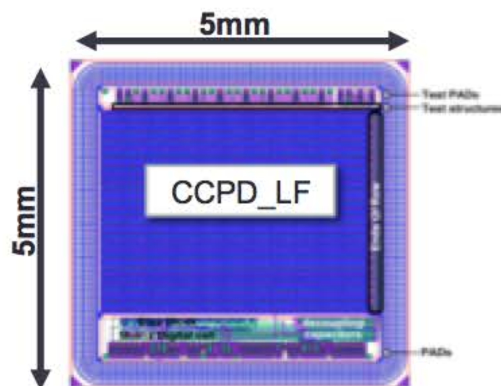
Efficiency and fake hit rate



LFOUNDRY

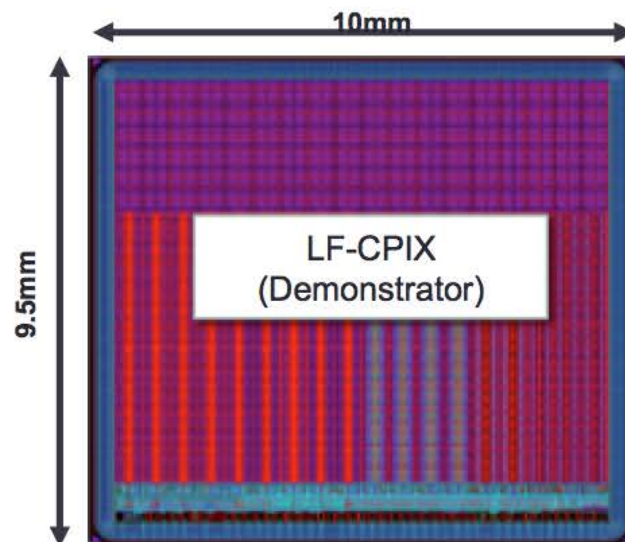
2014~2015
Small size demonstrator

CCPD_LF:
33×125μm² pix ; 6pix → 2 FEI4 pix
5×5 mm² IC, **bondable to FE-I4**
Bonn / CPPM / KIT



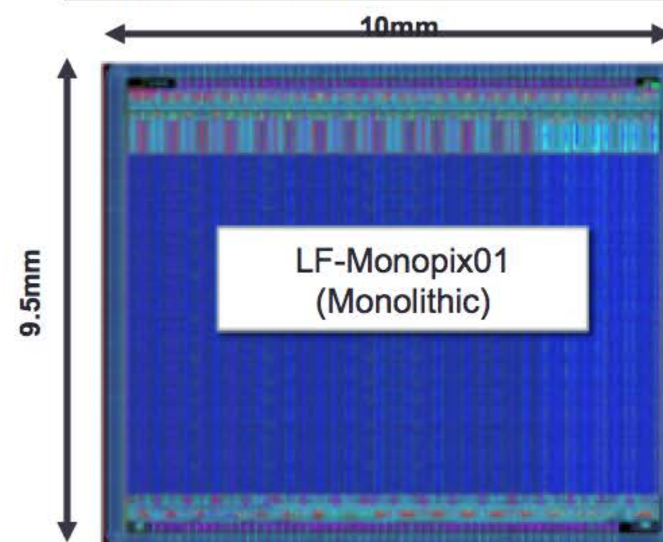
2016~2017
Large size demonstrator

LF-CPIX:
50×250μm² pix ; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring-
Bonn / CPPM / IRFU



2017~Present
Large Monolithic demonstrator

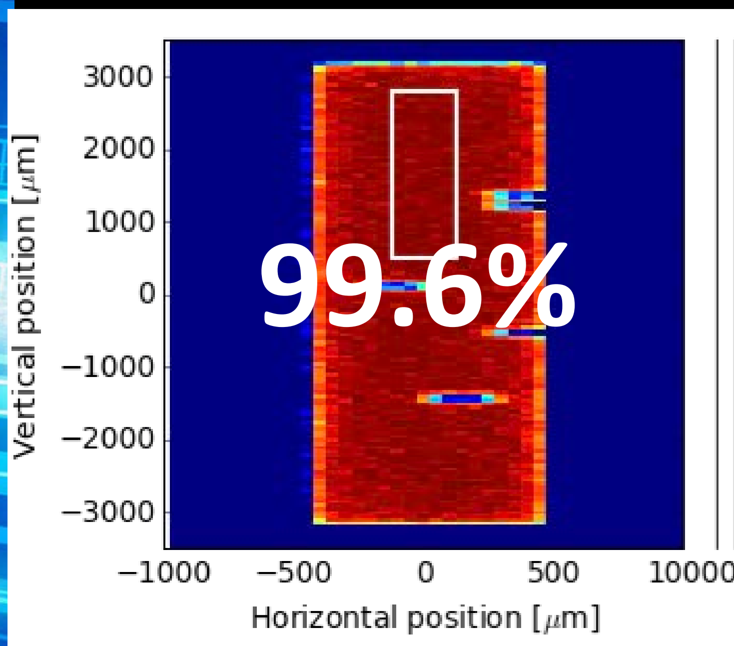
LF-Monopix:
50×250μm² pix.
Analog pixel part from LF-CPIX
10×10 mm².
1st **full monolithic** demonstrator
Bonn / CPPM / IRFU

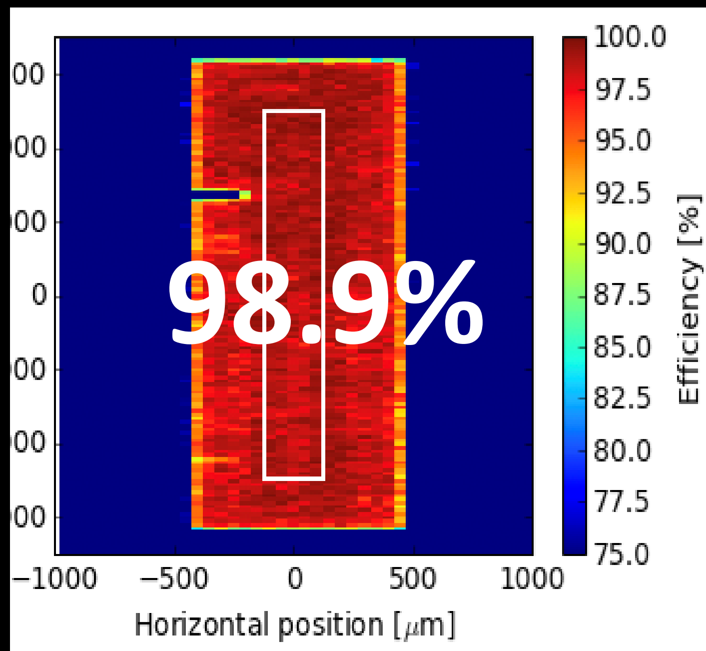


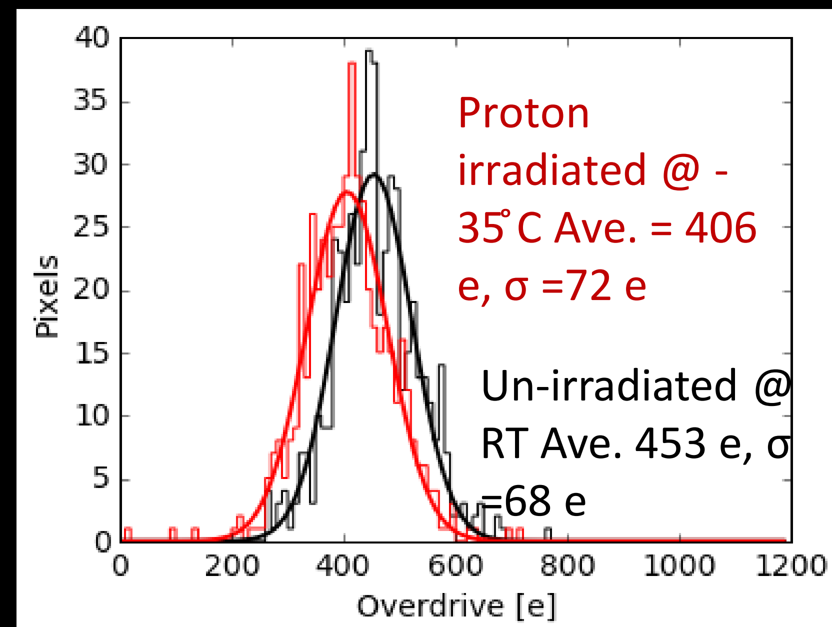
LFMonoPix before/after irradiation

- Unirradiated: Noise < 1.2 Hz/pix
- Neutron irradiation: Noise < 0.1Hz/pix

No degradation in timing performance





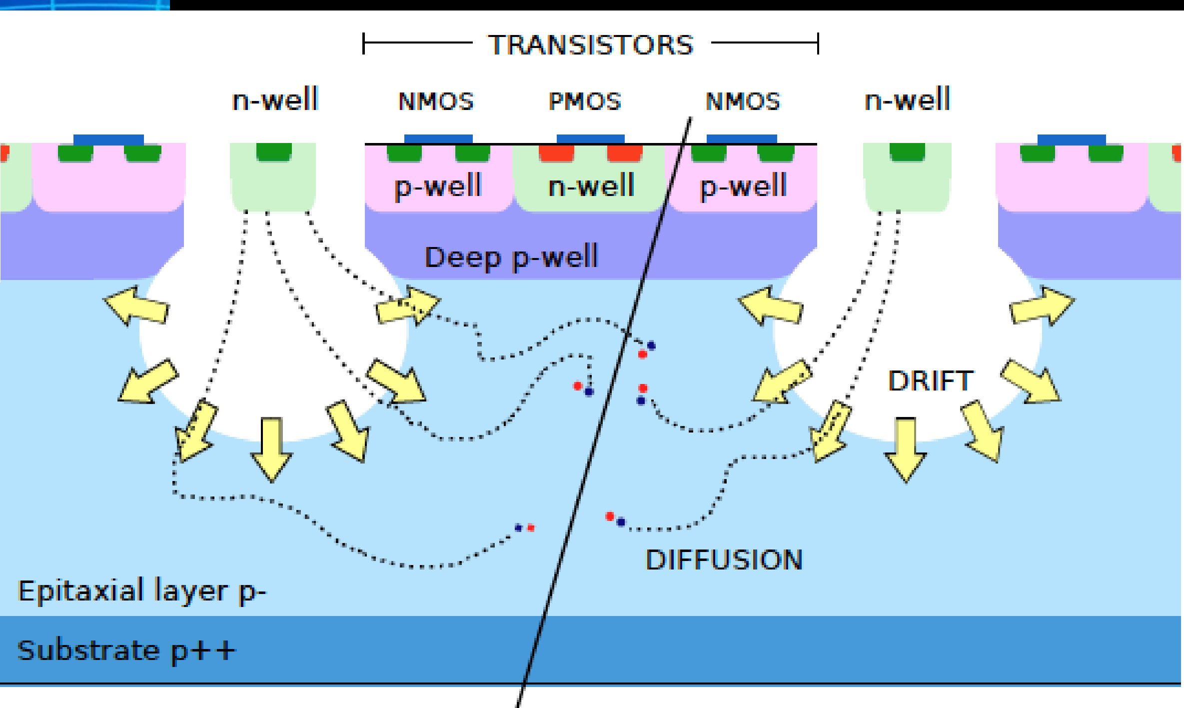


Hit efficiency is as high as 98.9% after the NIEL irradiation ($10^{15} n_{eq}/cm^2$)

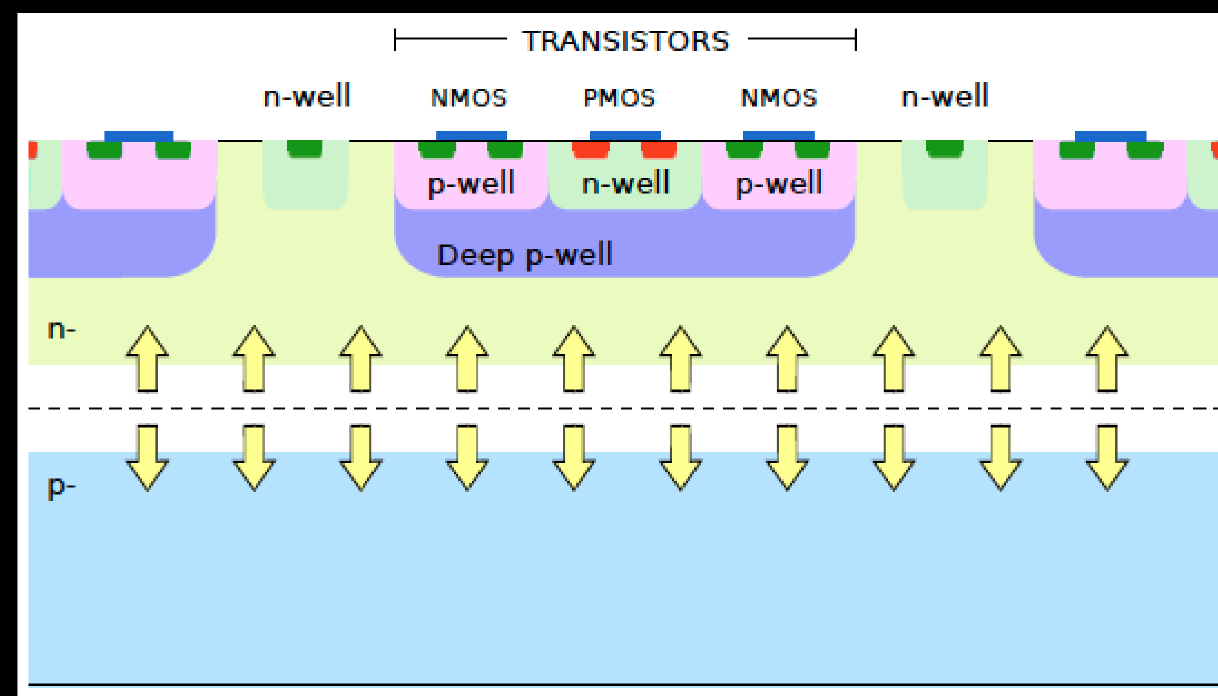
Overdrive = In-time threshold – Discriminator threshold (1500 e-)

TowerJazz 180nm MALTA sensor

- Small collection electrode (few um.)
- Small input capacitance (< 3 fF) allows for fast & low-power FE
- High S/N for a depletion depth of ~20um
- To ensure full lateral depletion, uniform n-implant in the epi layer (modified process)



Standard Process

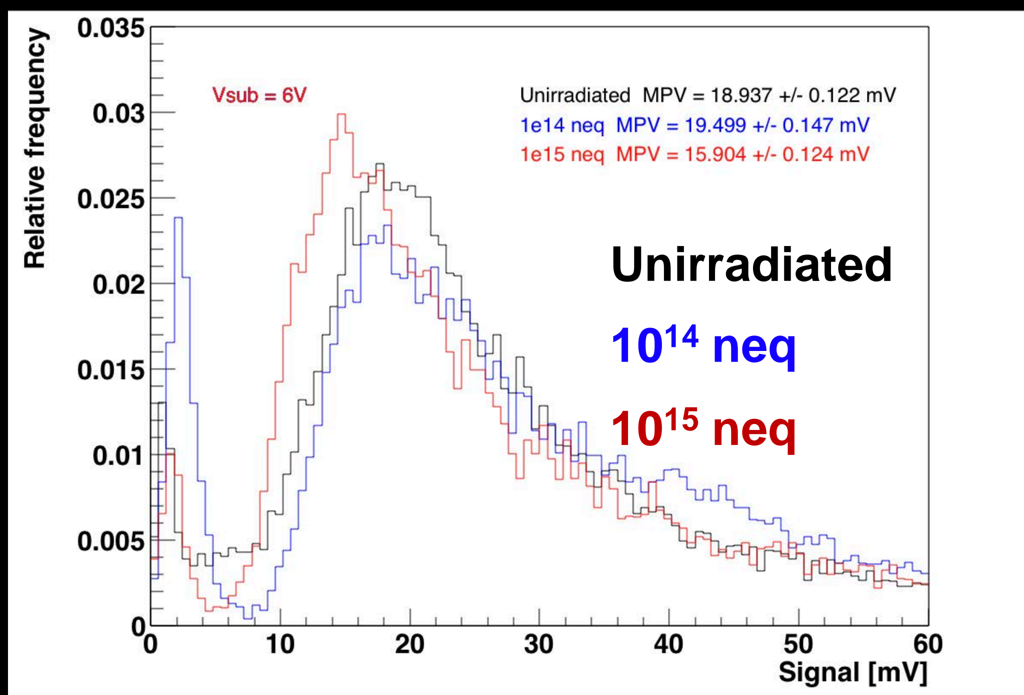


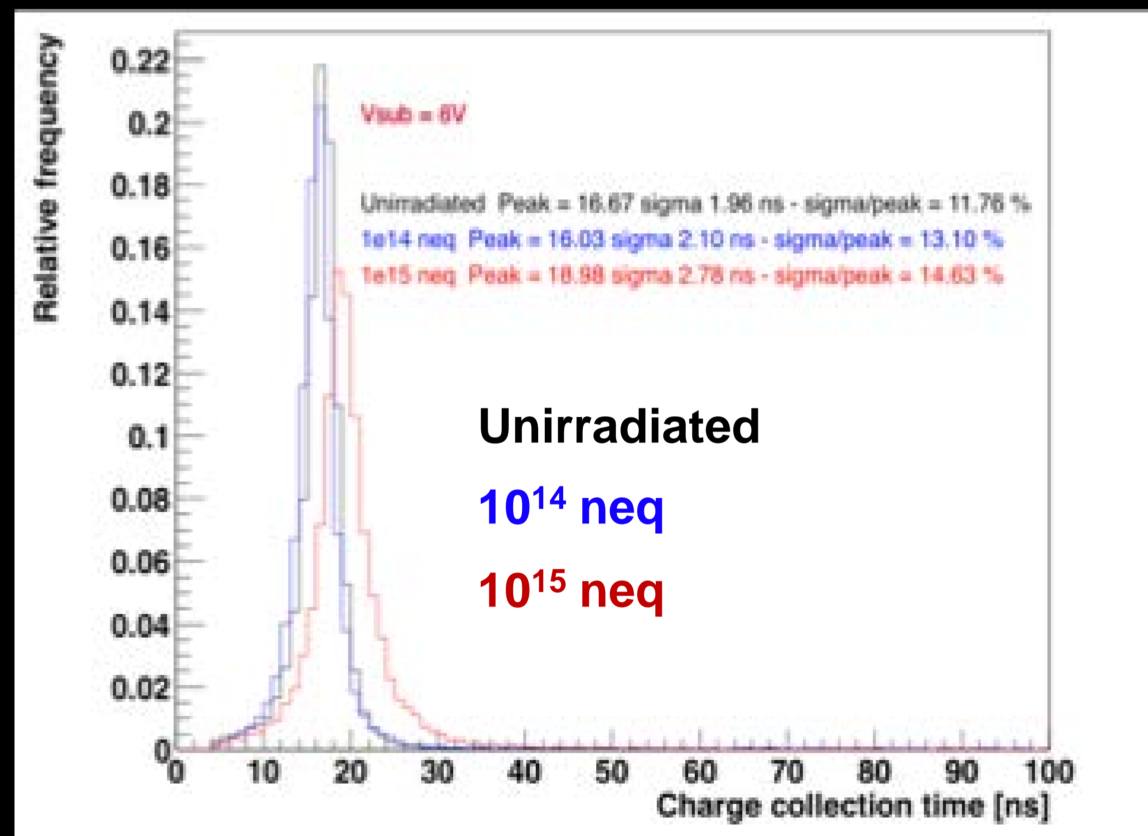
Modified Process: TowerJazz 180nm MALTA sensor
W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046

Initial results with small electrodes

- TJ180nm Investigator Sensor (*CE: 3 x 3 μm² centered in a 18 x 18 μm² opening, 25 μm epi)*
- Developed in context of ALICE ITS Studies of pixel pitch, electrode size & spacing
- Irradiation program for ATLAS outer pixels

^{90}Sr measurements on modified process samples

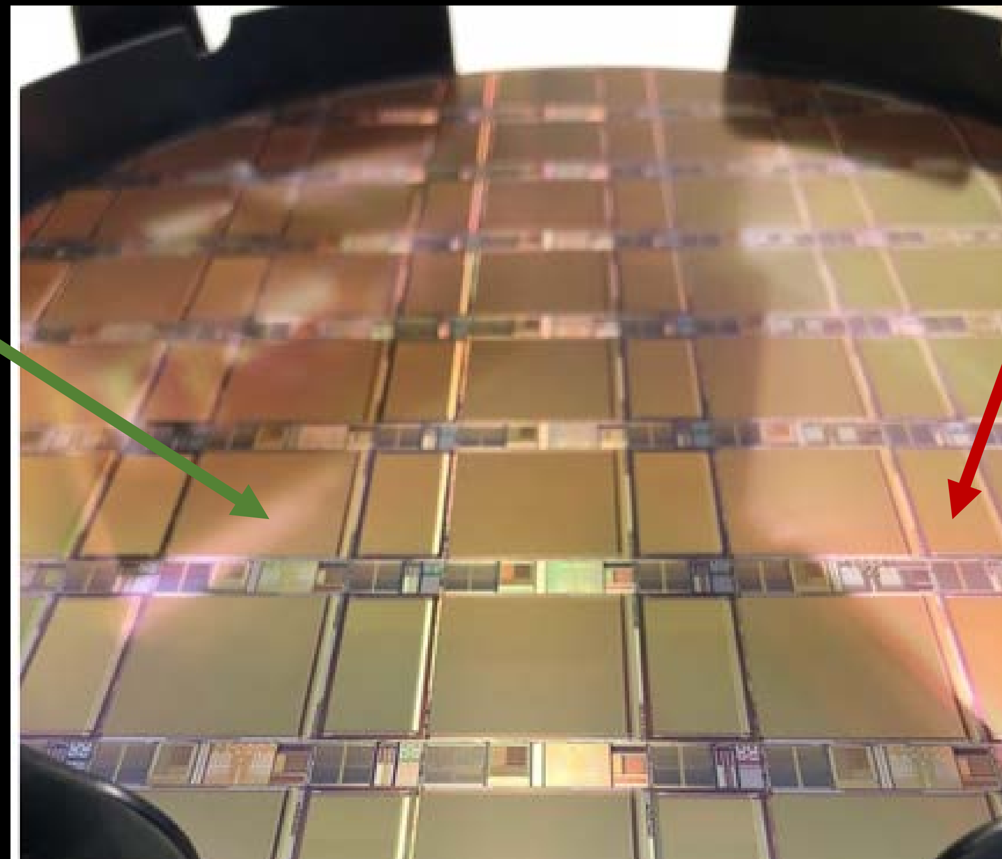




MALTA

- Two large scale demonstrators for ATLAS outer pixel layers

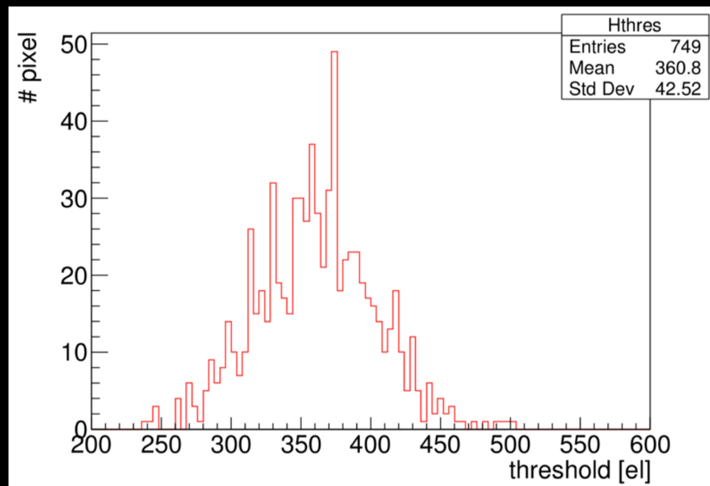
The “MALTA” chip
($2 \times 2.2\ cm^2$)
Asynchronous readout architecture
Pixel size $36.4 \times 36.4\ \mu m^2$



The “TJ-Monopix” chip
($2 \times 1\ cm^2$) Synchronous readout architecture
$36 \times 40\ \mu m^2$

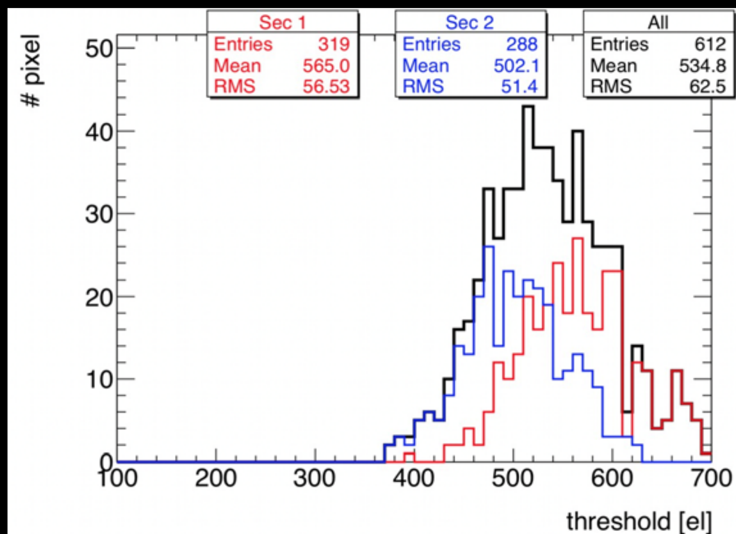
Malta performance

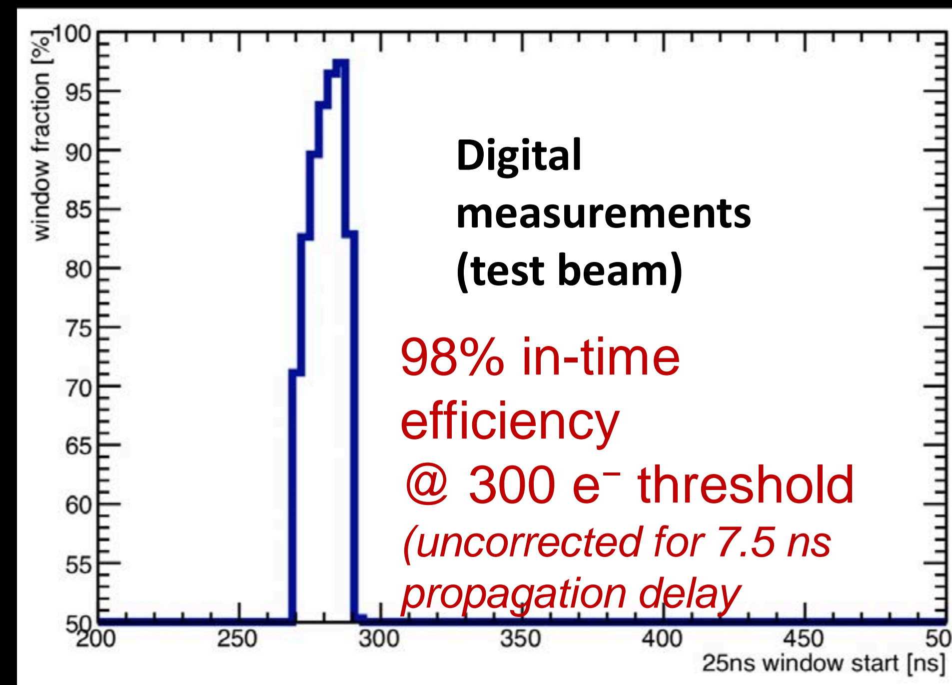
Before Irradiation

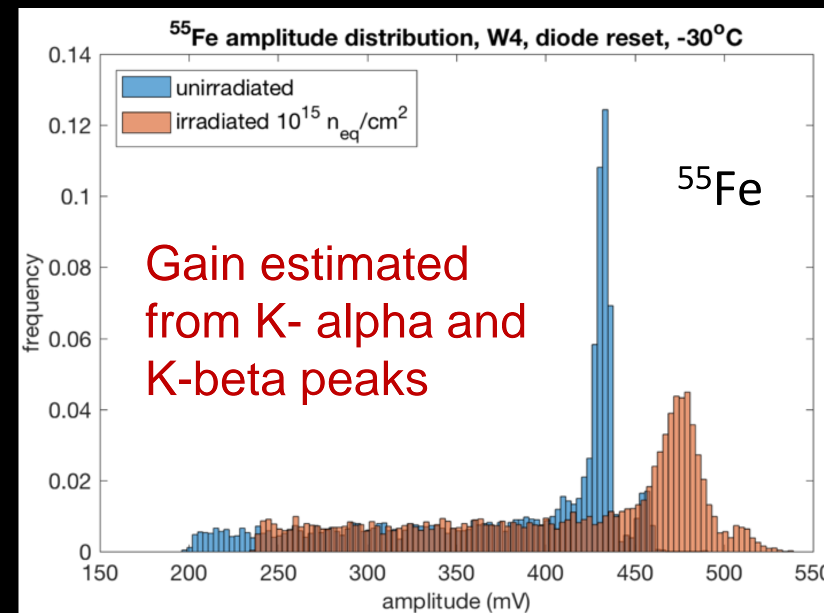


- Threshold dispersion ~x2 larger than design
- Improvements already made

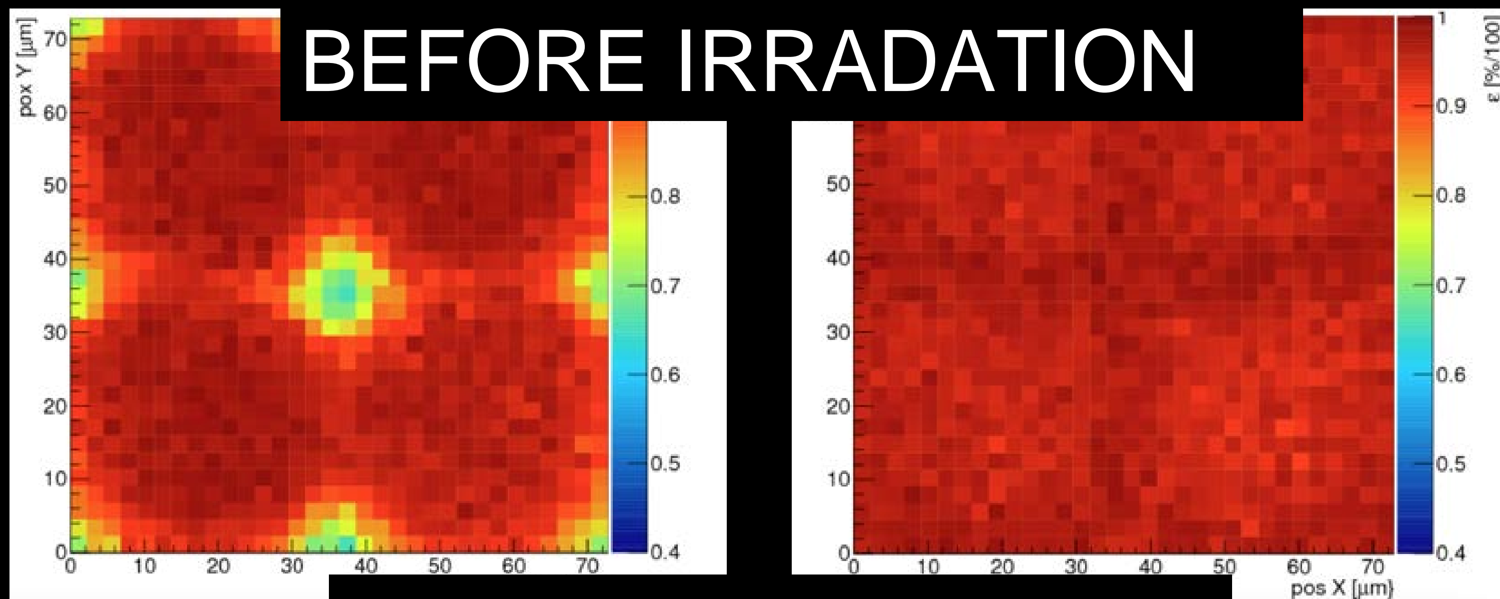
After Irradiation 70 MRad

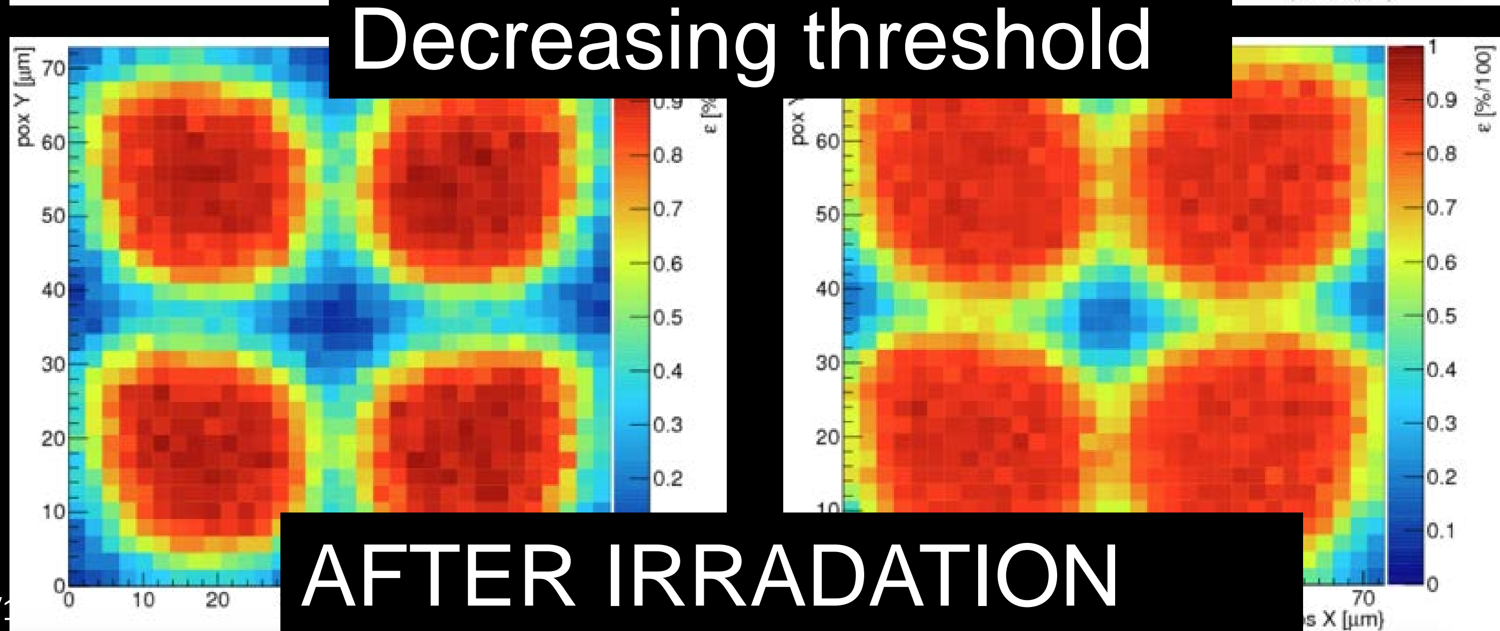






MALTA performance (Beam Tests)

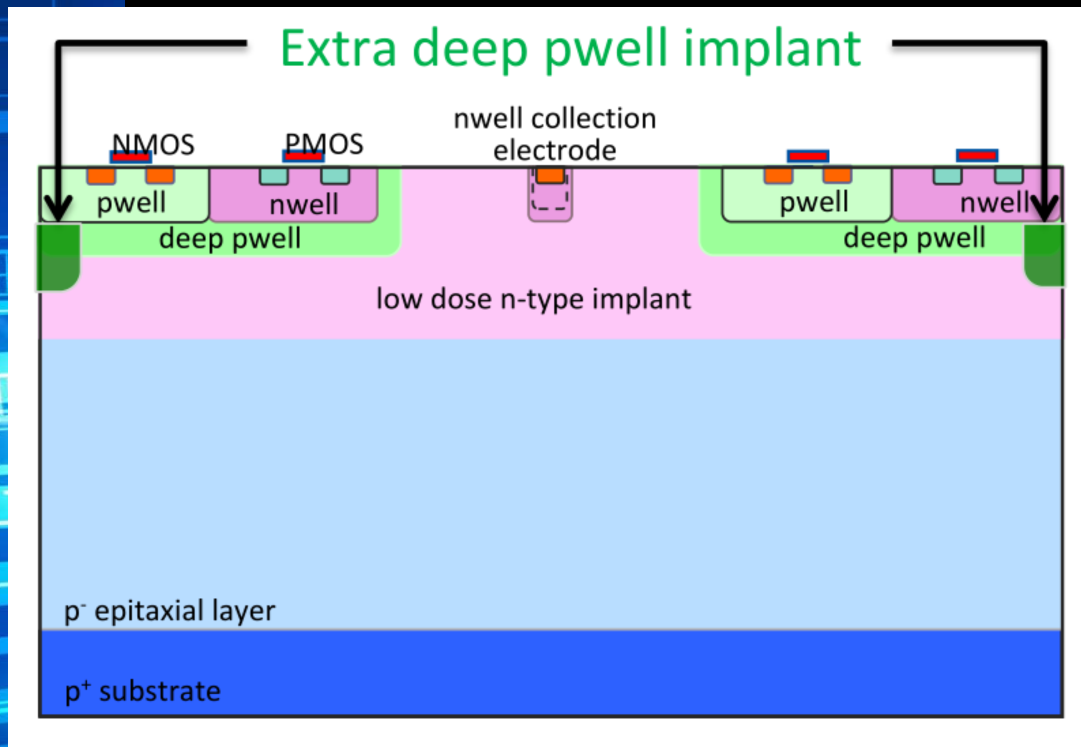




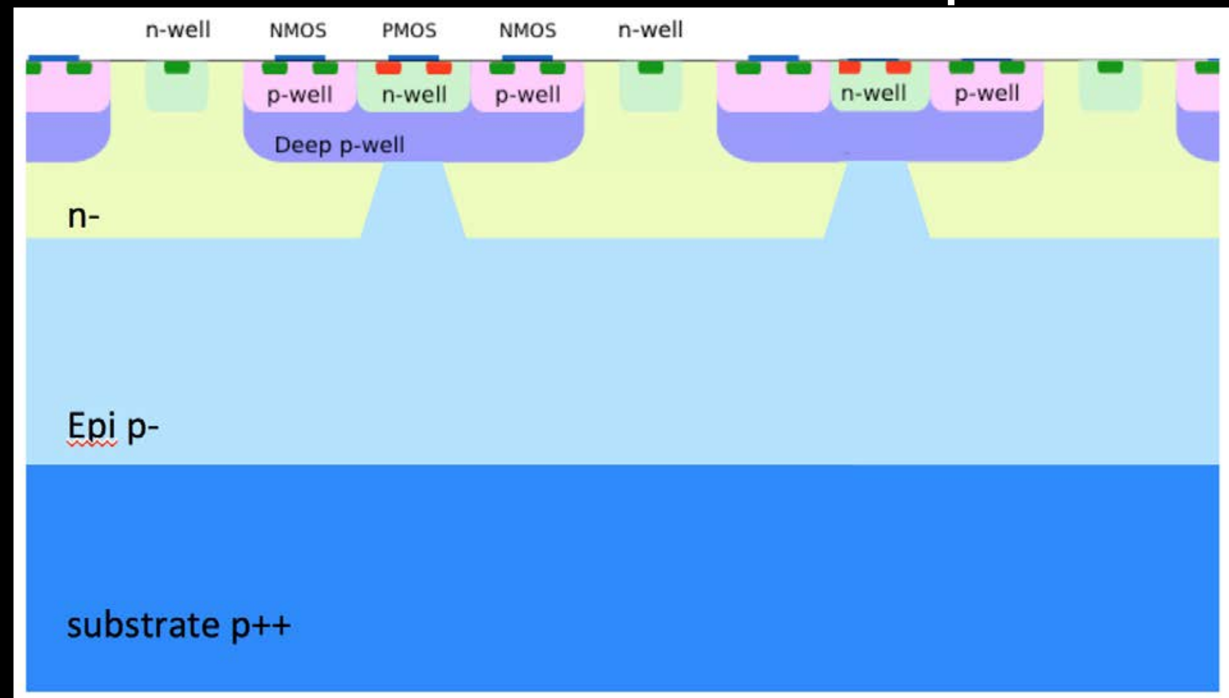
- In Pixel efficiency
  - High (600 e^-) to low (250 e^-) threshold before irradiation
- In Pixel efficiency
  - High (600 e^-) to low (350 e^-) after $5x10^{14}$ n_{eq}/cm^2

Pernegger, Sharma

Improvements to MALTA

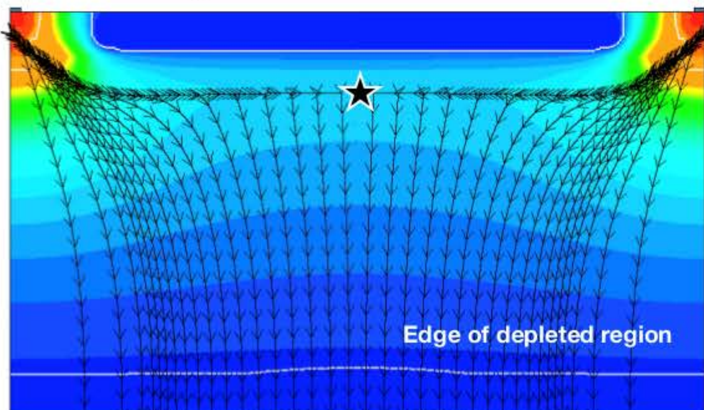


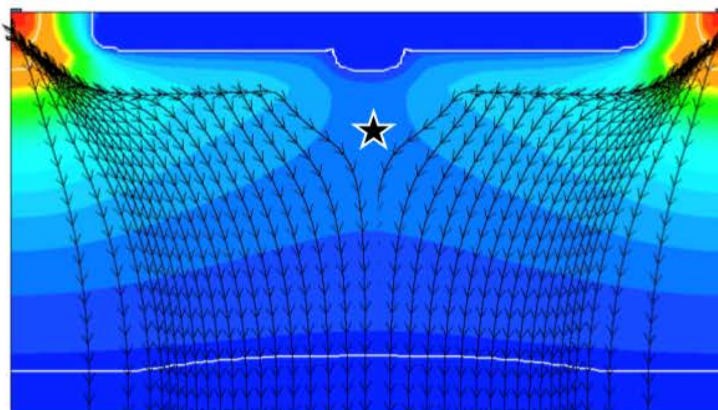
- Further modification of the process

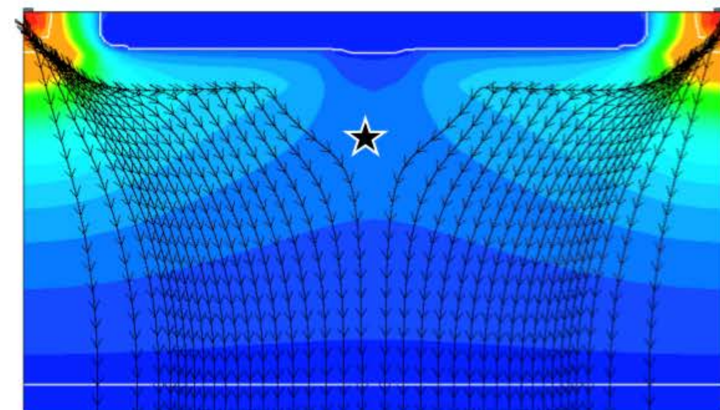


- Extra deep p-well implant
- Gap in the n-layer
- Tested with MiniMalta (Chip just arrived)

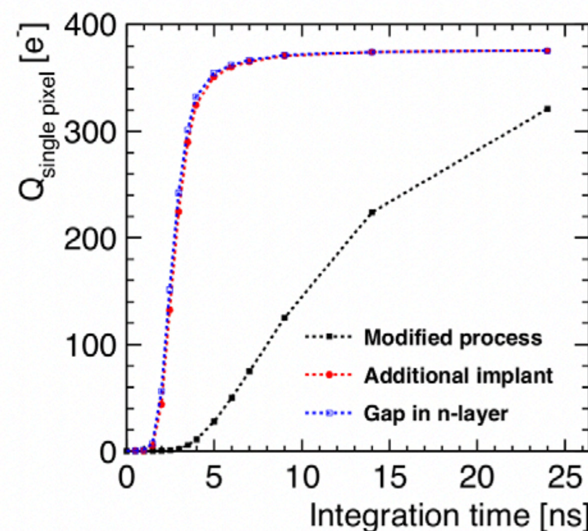
Improved pixel design

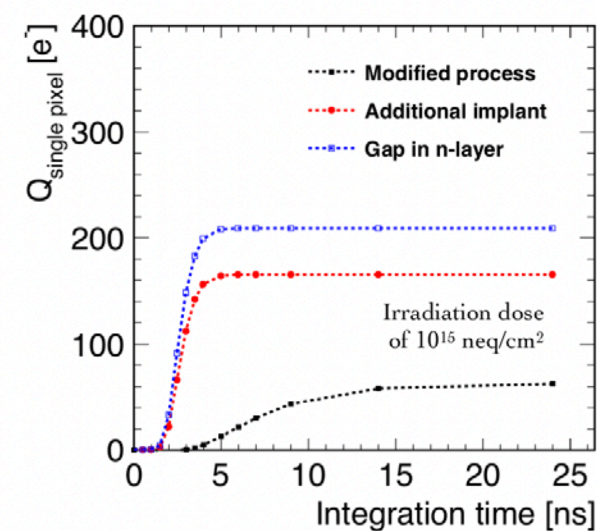






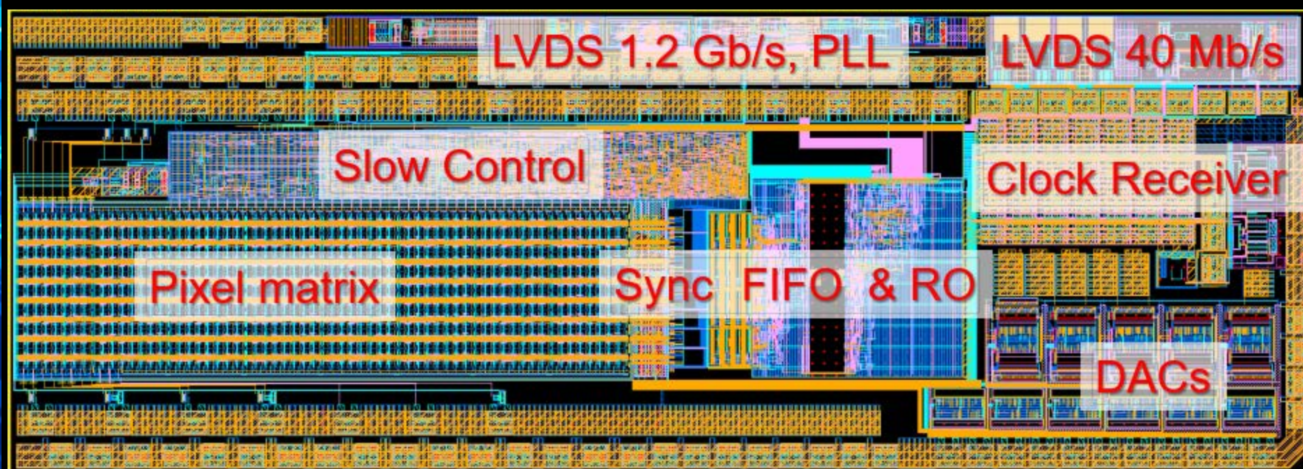
- **3D TCAD transient simulation**
- from M. Munker
  Constant potential at pixel border produces a field minimum (★)
  Additional implant and gap in n- layer provides a potential difference in the lateral direction





MiniMALTA

- Improved process design
- Matrix of 64x16 pixels
- 8 sector splits for analog FE design, reset mechanism and process
- Synchronization at the end of column
- Also, new version of MALTA available, with improved Slow Control



analogue monitoring pixels

S0 S4 — standard

S1 S5 — extra-deep p-well

S2 S6 — standard, PMOS reset

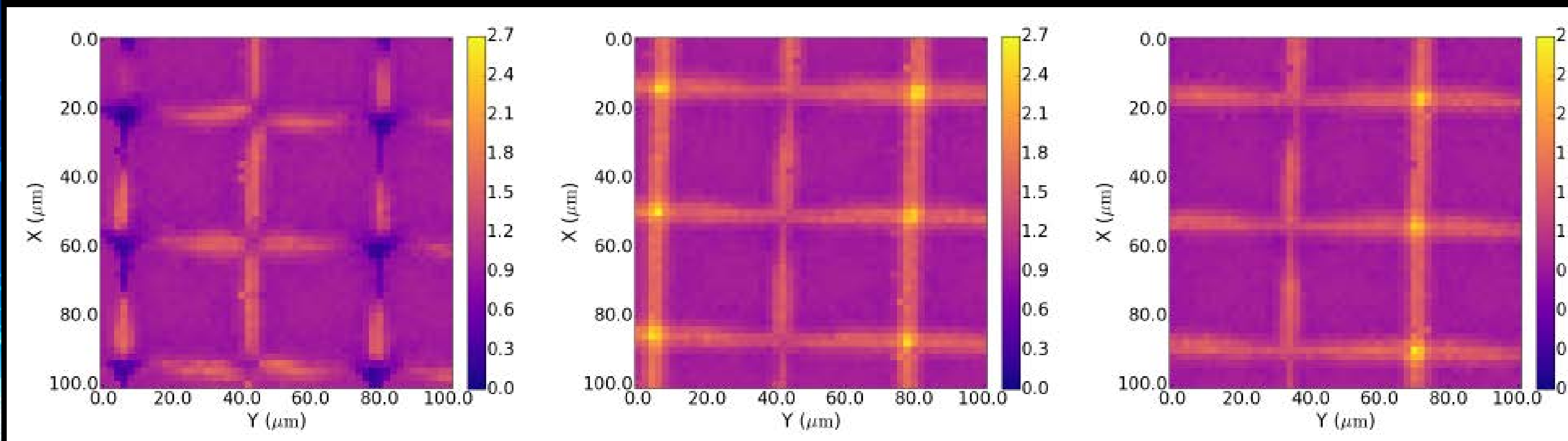
S3 S7 — n- gap

standard front-end

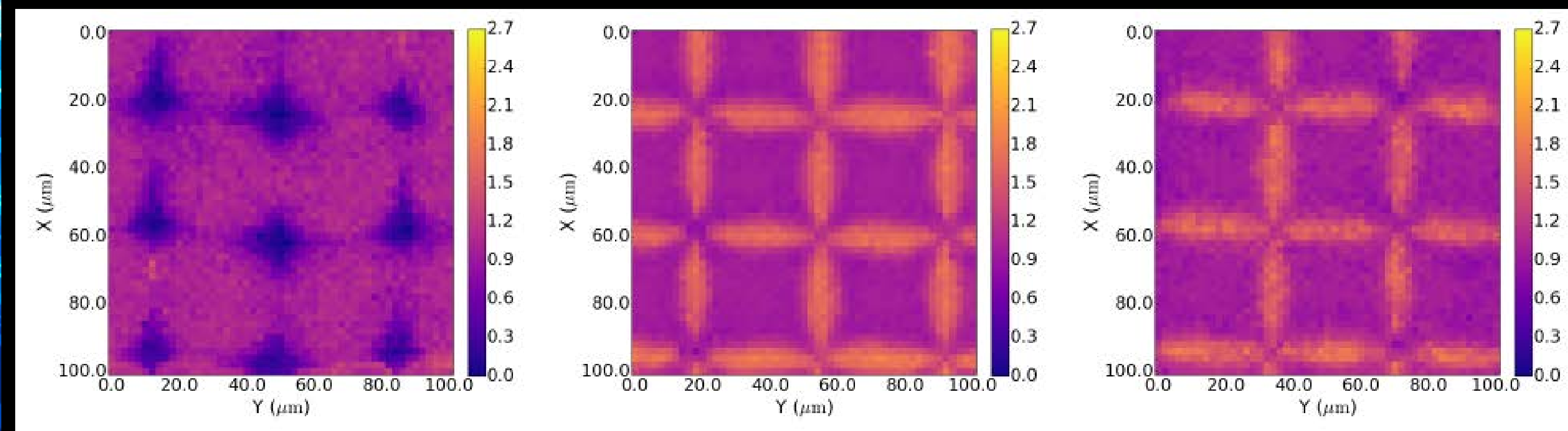
enlarged transistors

MiniMALTA

8 KeV microbeam at DIAMOND



Before Irradiation



After 10^{15} n_{eq}/cm^2

Malta | P-well | N-gap

Beyond ATLAS

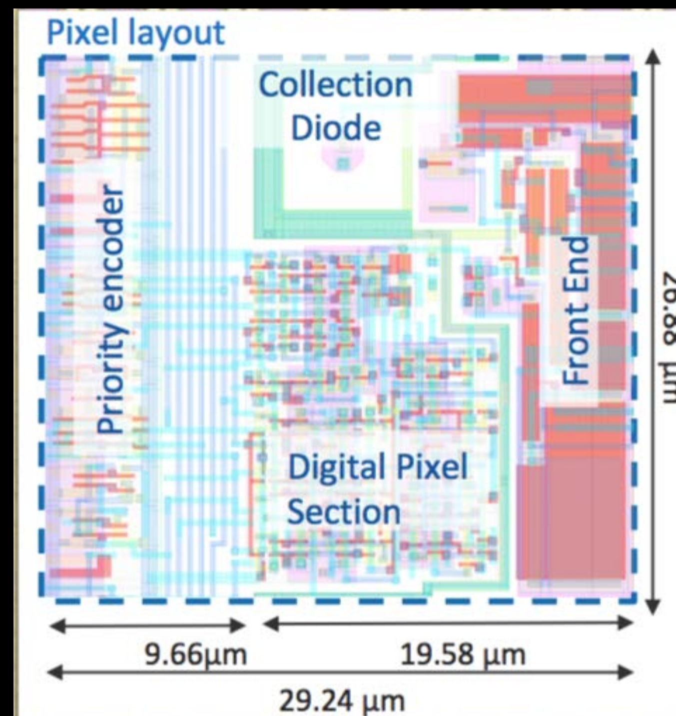
Pernegger

Now in 0.18 µm

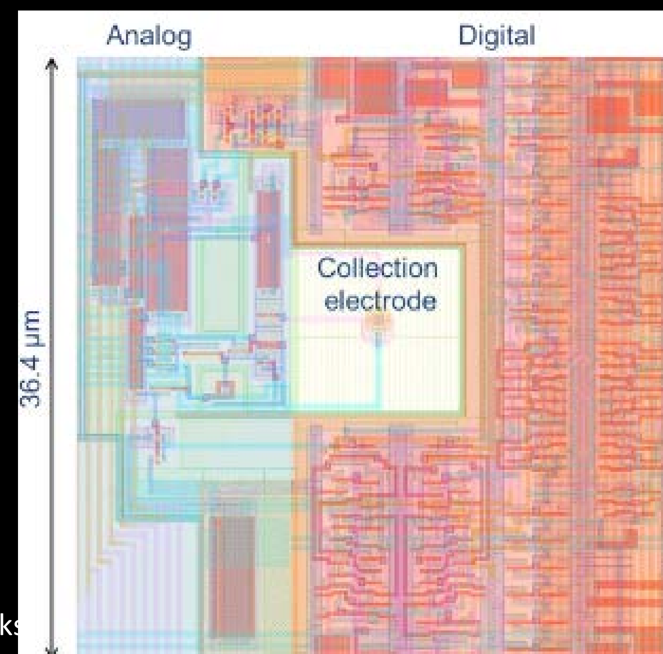
- Q/C > ~ 0.25 fC / 5 fF = 50 mV
  - ALPIDE: 40 nW/pixel (analog)
  - MALTA/Monopix: 1 µW /pixel (25ns)
  - Analog power in matrix dominant
- Pixel pitch ≈ sensitive layer thickness ≈ 30 µm
  - Position resolution ~ 5 µm
- Matrix hit rate capability:
  - MALTA matrix > 100 Mhit/mm²/s (but cannot cope at periphery)

Deeper submicron

- Q/C >>
  - Analog power will go close to zero
- Pixel pitch ≈ sensitive layer thickness ≈ 5-10 µm
  - Position resolution ~ 1-2 µm
- Matrix hit rate capability:
  - 10's of GHz/mm² (but need to cope at periphery)



ALPIDE

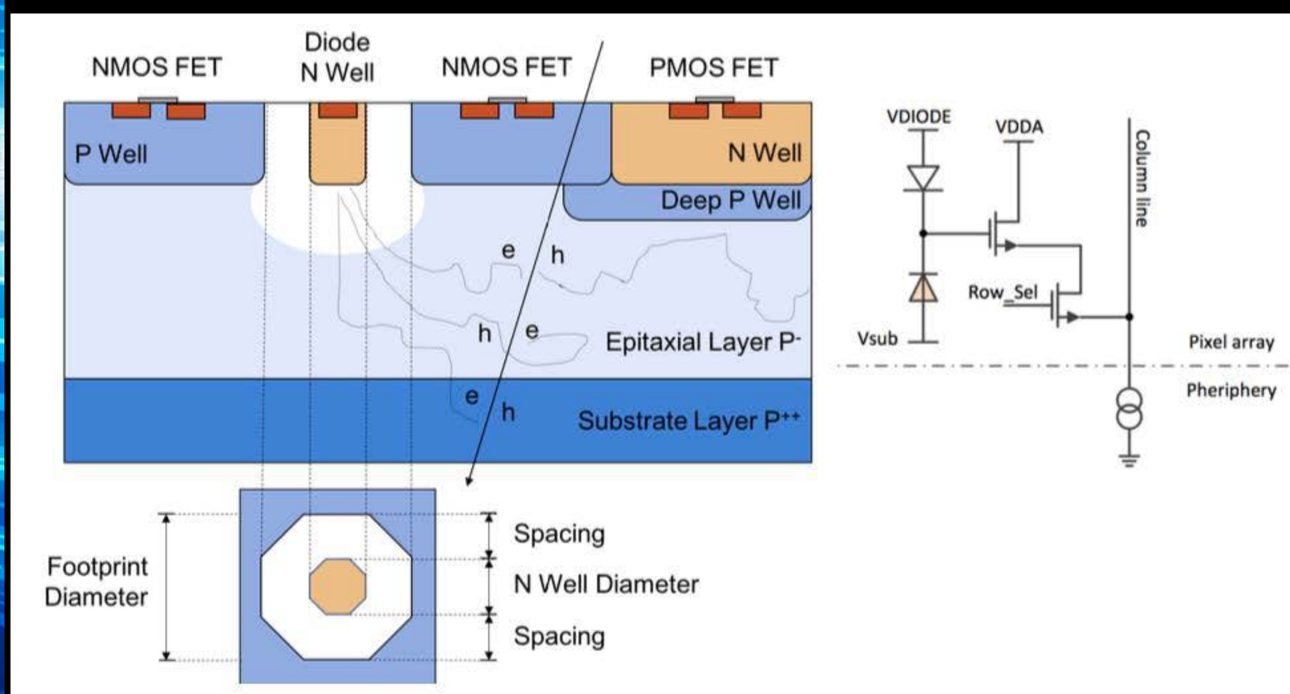


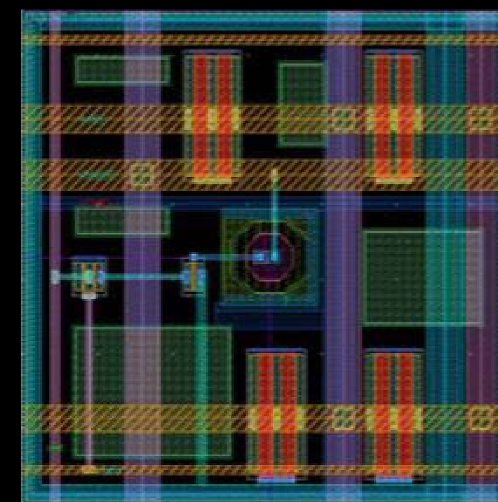
MALTA

JadePIX 1 for the CEPC

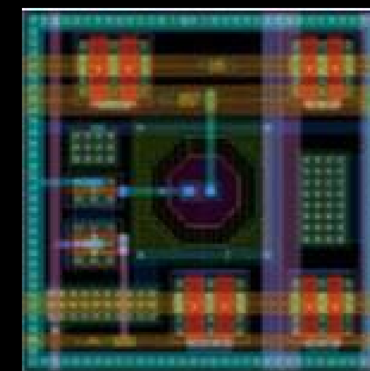
IHEP, USTC

- TJ 0.18 µm CMOS image process with high resistance epi-layer
- Goal: sensor diode geometry optimization





$33x33\mu m^2$



$16x16\mu m^2$

Submission end 2015, detailed characterization in 2018

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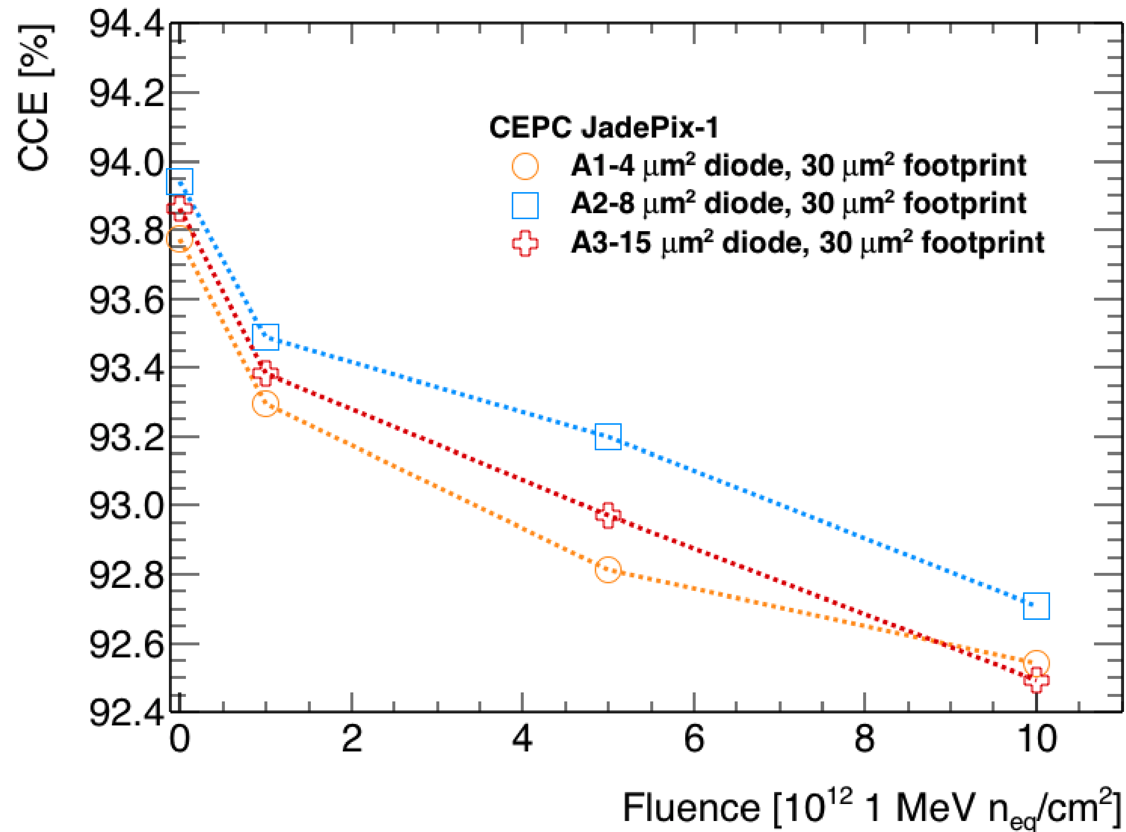
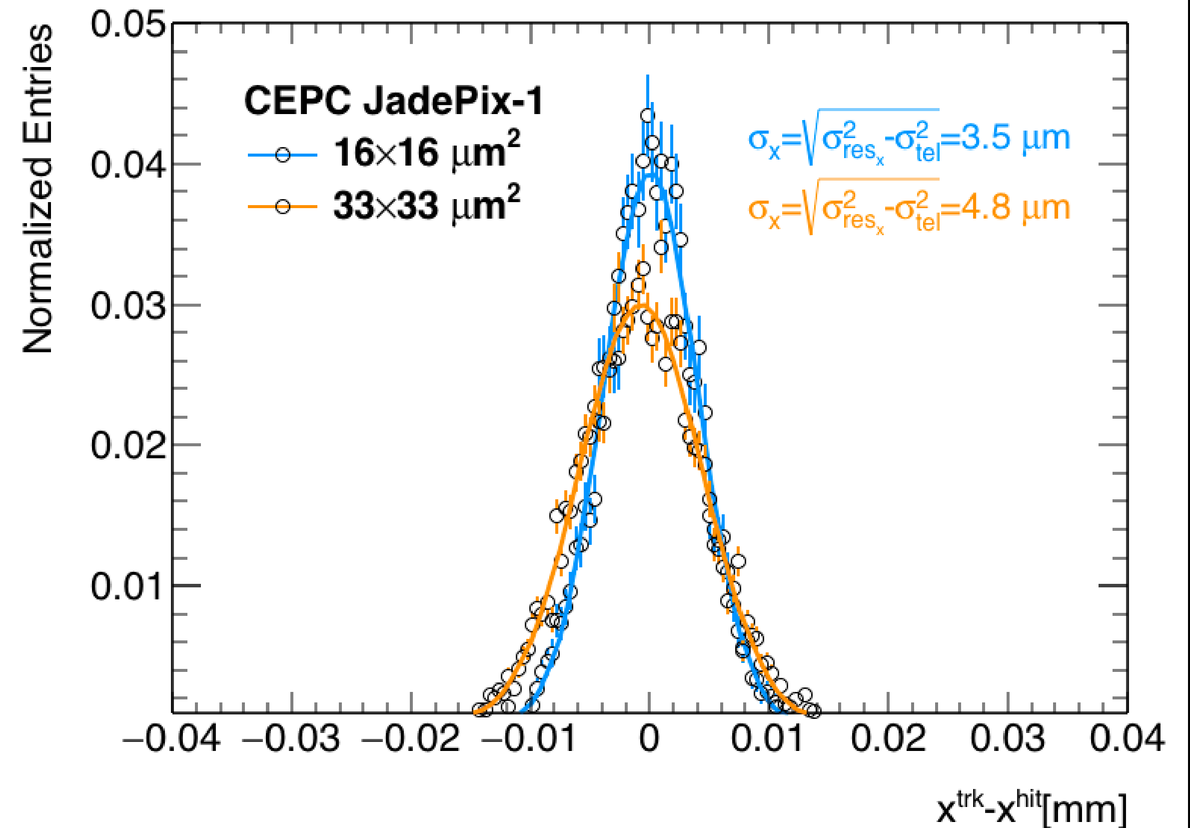
JadePIX 1 characterization

Charge collection efficiency (measures with Sr90) decreases as a function of dose

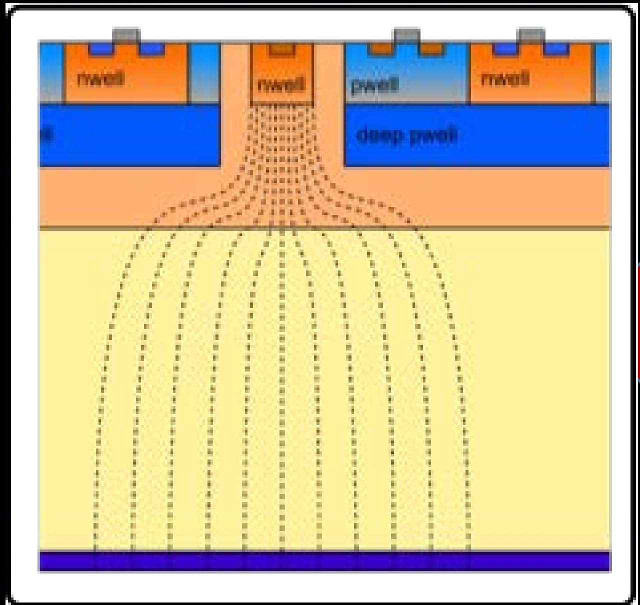


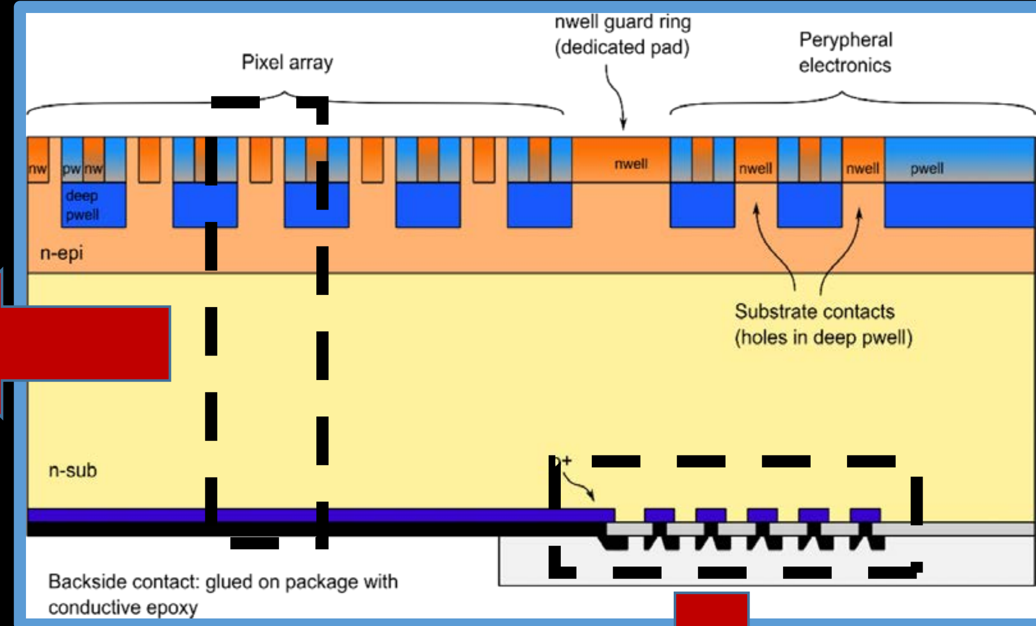
- Spatial resolutions better than 5 μm and 3.5 μm for pixel sizes of 33x33 μm^2 and 16x16 μm^2 achieved at DESY beam test

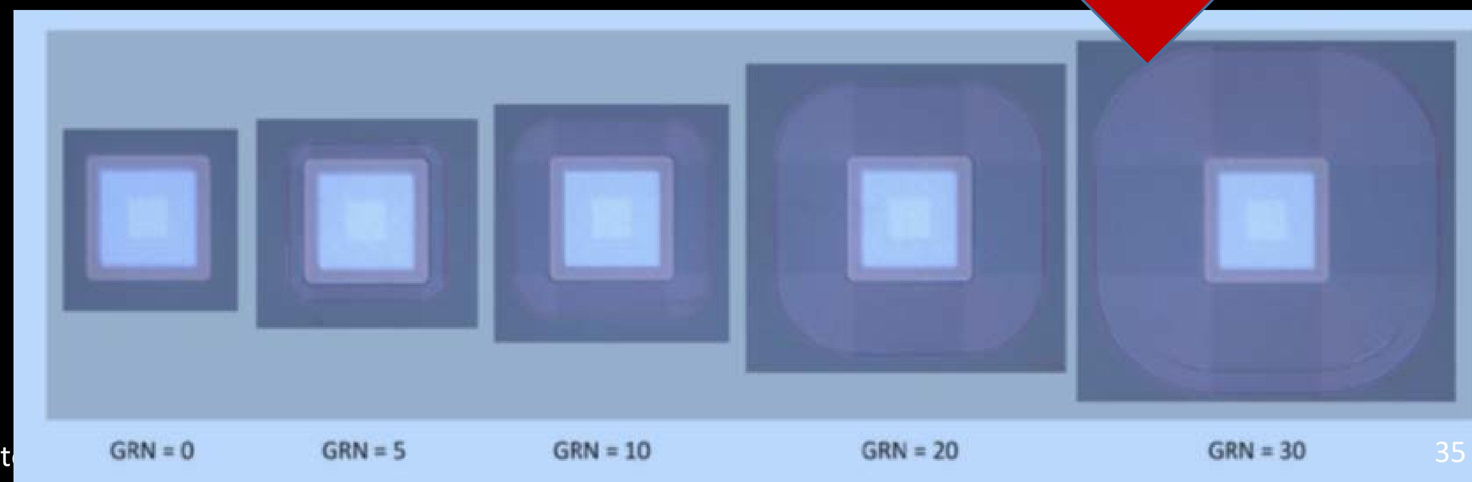


SEED Sensor with Embedded Electronics Development (INFN)

- 110 nm CMOS on high-resistivity bulk (LFOUNDRY)
- Small n-type collecting node ➟Low capacitance (20 fF) and fast O(ns)
- Deep p-well allows both NMOS and PMOS transistors
- Full depletion in 100-500 μm n-type substrate achieved by voltage at the p+ backside
- Double-sided lithography was used for the processing of the backside layers
- Backside p+ implantation after thinning
- Floating guard rings have been added to avoid early breakdown



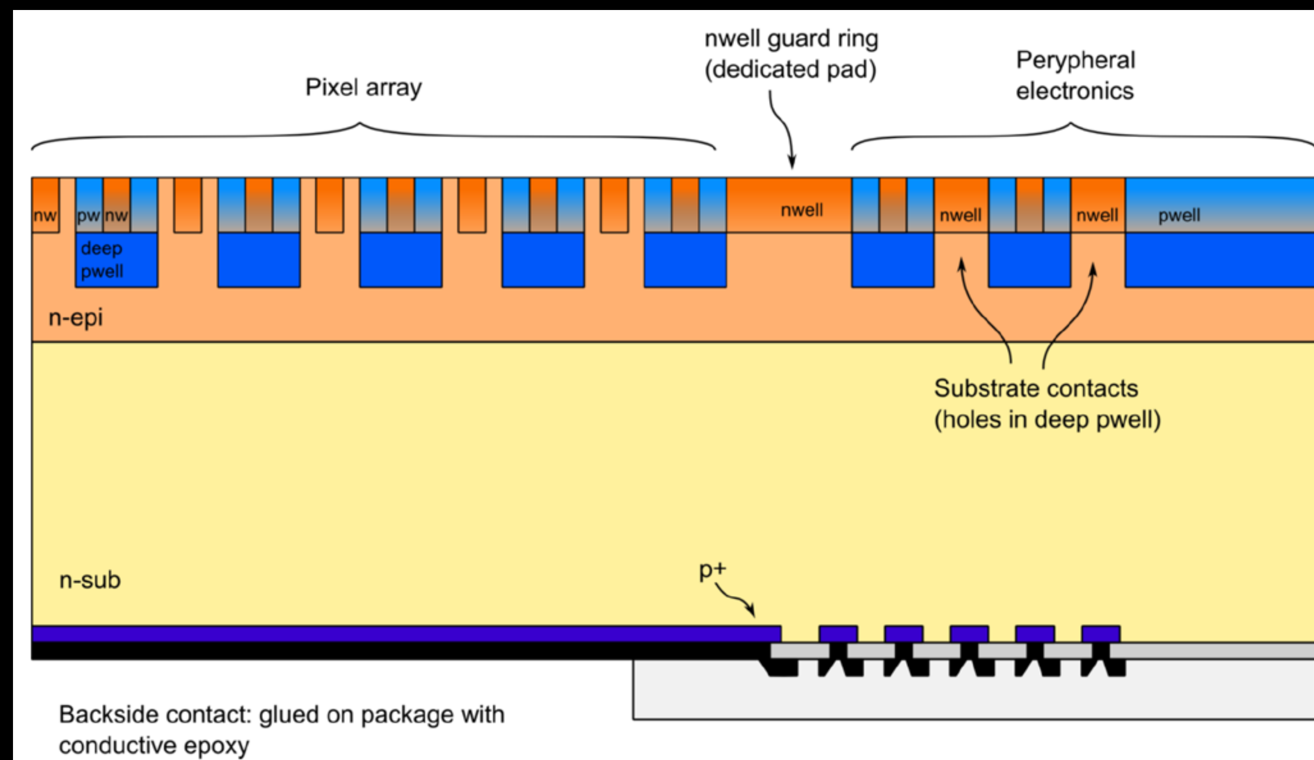




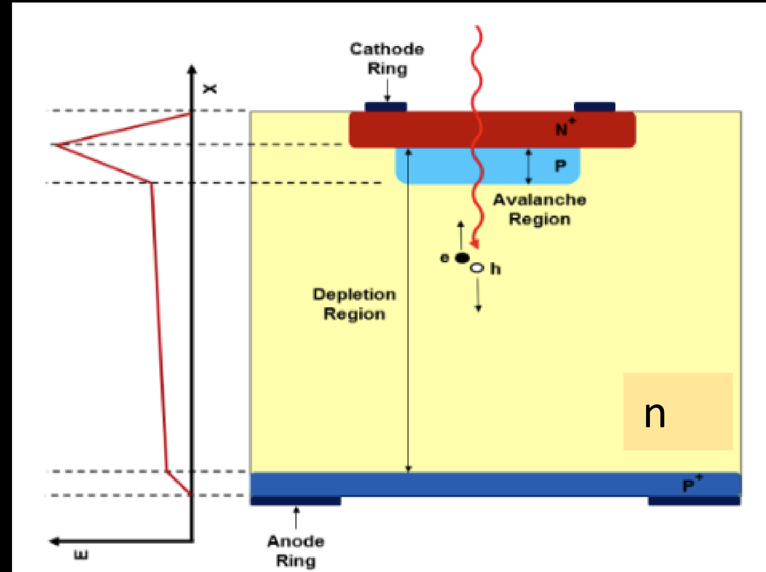
ARCADIA: System-grade Demonstrator

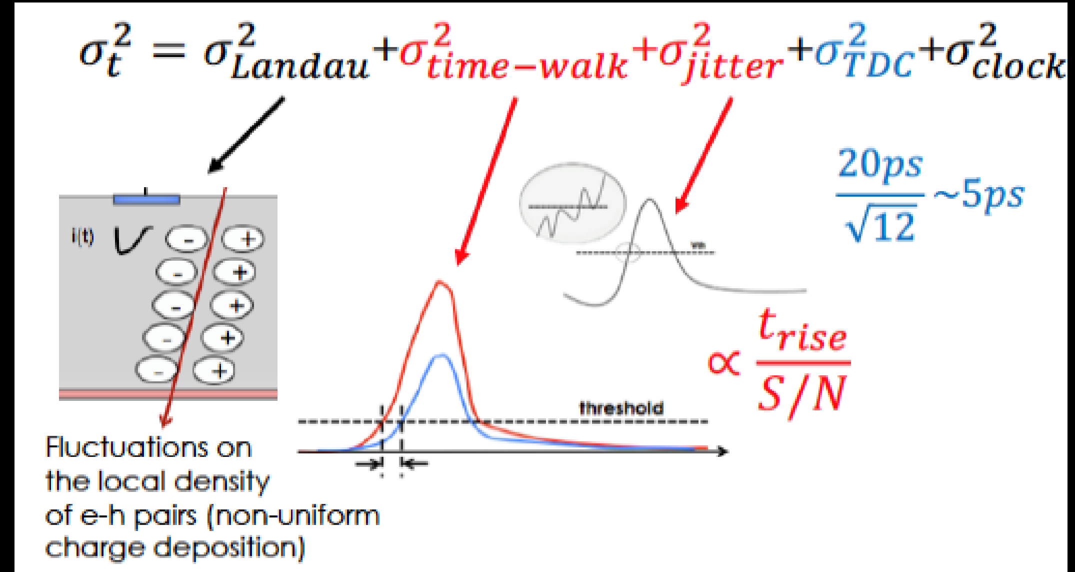
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

- INFN CSNV Call Project: budget 1MEur
- Active sensor thickness in the range 50 μm to 500 μm or more
- Operation in full depletion with fast charge collection by drift
- Small charge collecting electrode for optimal signal-to-noise ratio
- Scalable readout architecture with ultra-low power capability (O(10mW/cm^2))
- Easy compatibility with standard CMOS processes.
- Deliverable: full-size system-ready demonstrator of a low-power High-density pixel matrix CMOS monolithic sensor

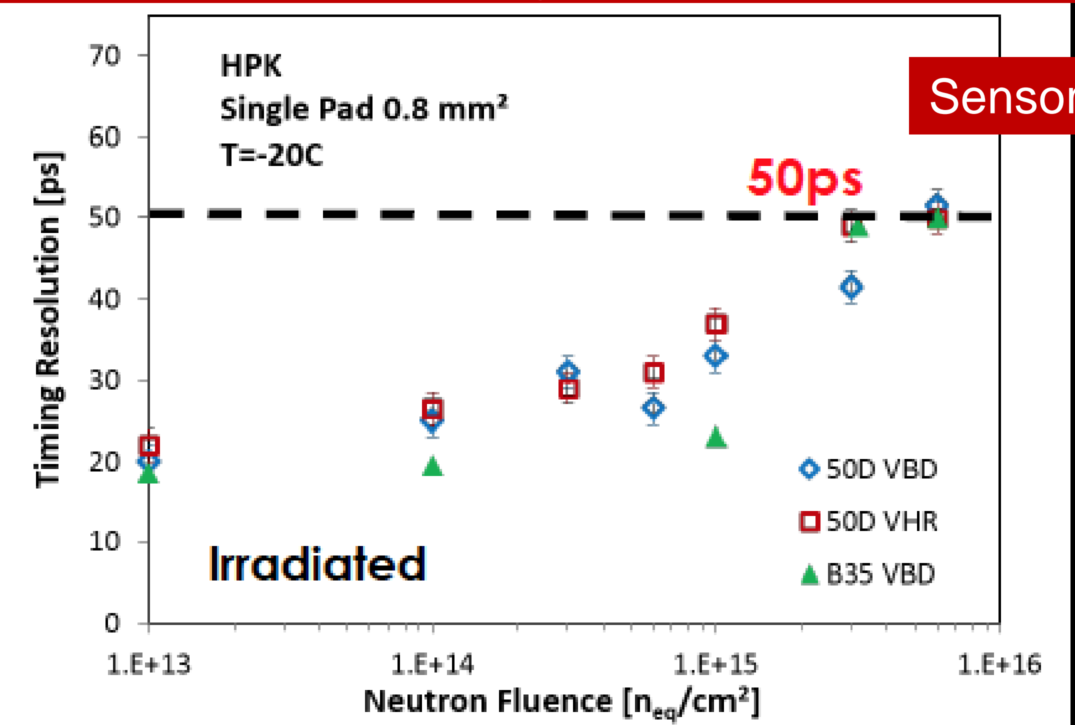


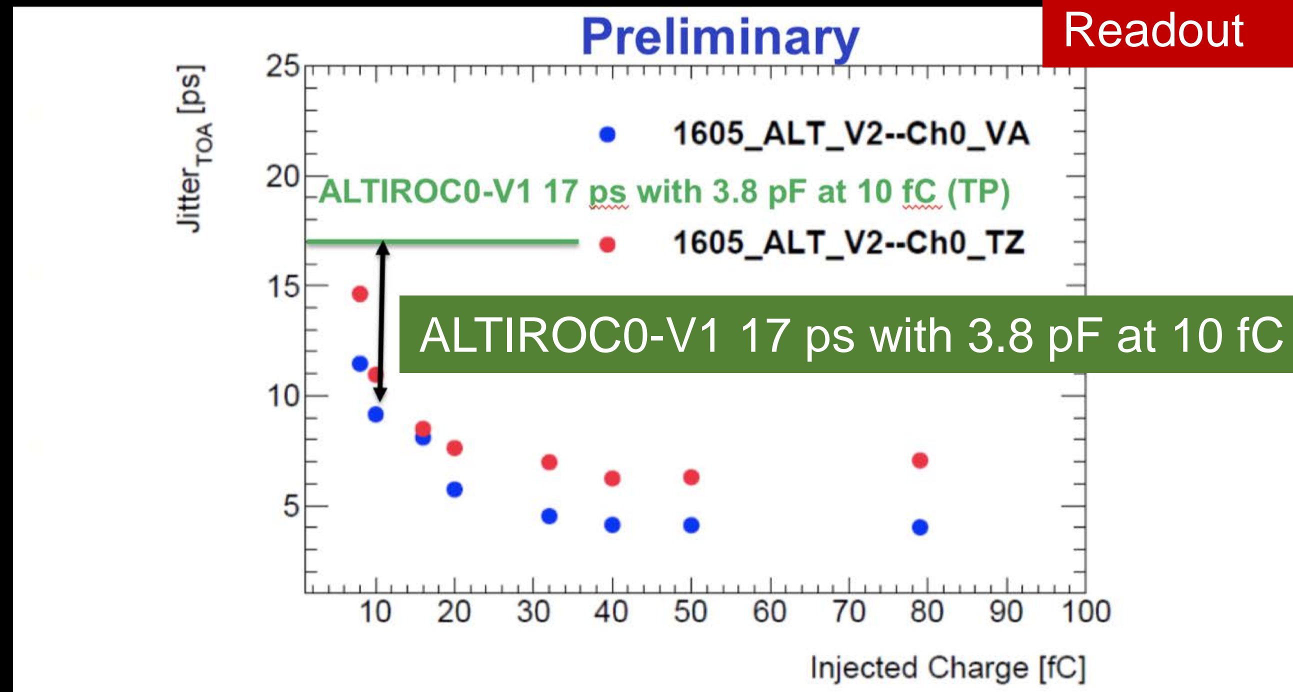
LGAD





$\sigma(t) < 50$ ps @ 5×10^{15} n_{eq}/cm^2 with V_{bias} 10% < V_{BD}



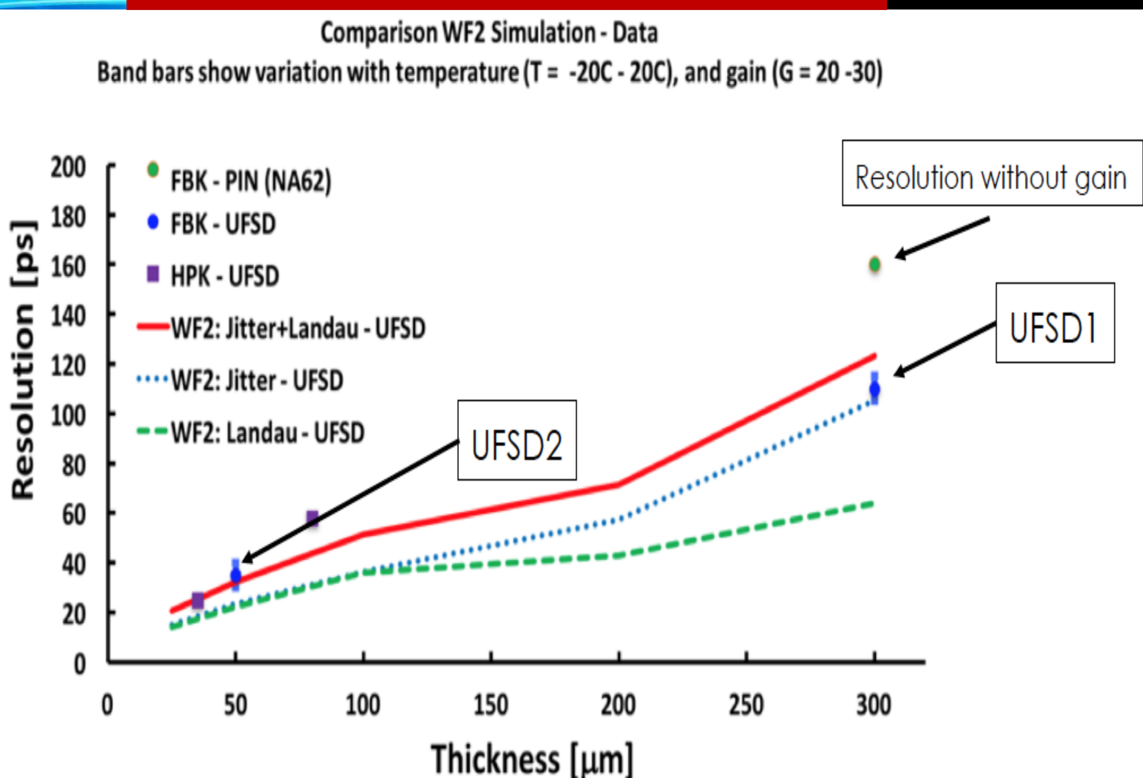


Still need to check that input parasitic capacitance on PCB is similar for V2 and V1

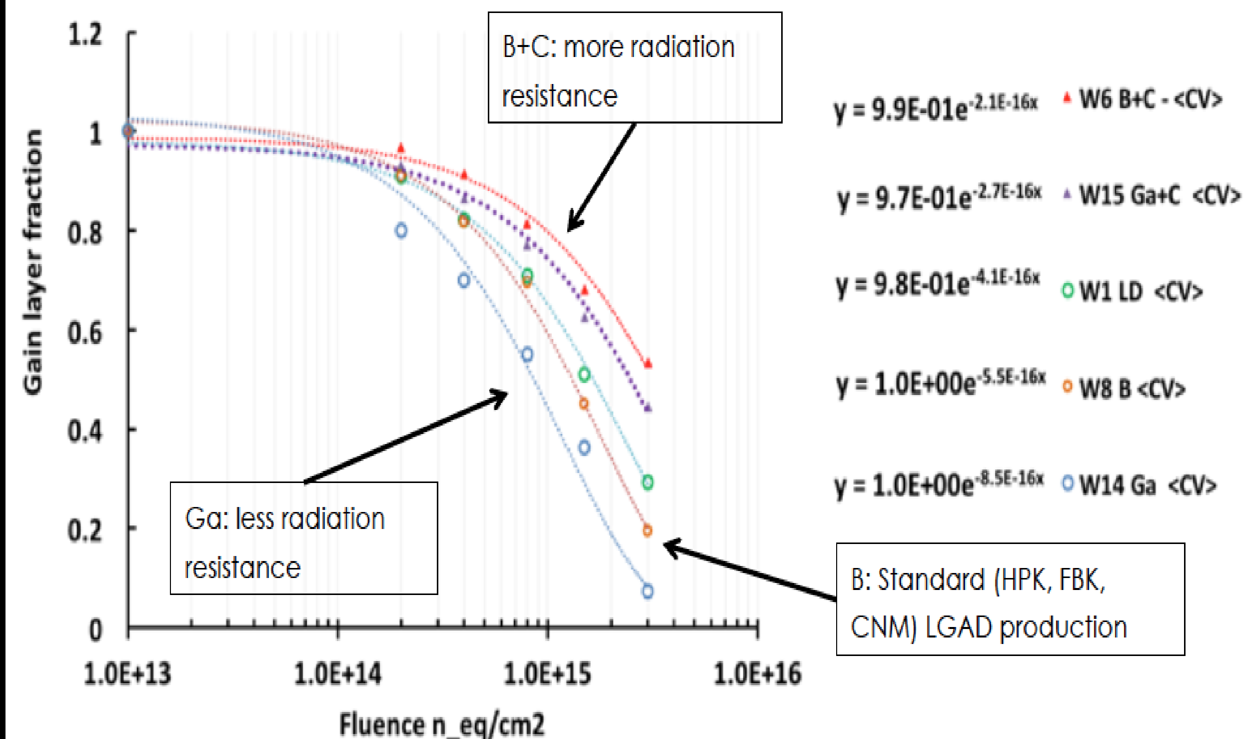
4D TRACKING – ULTRA FAST SILICON

- Timing at each point along the track→4D Tracking

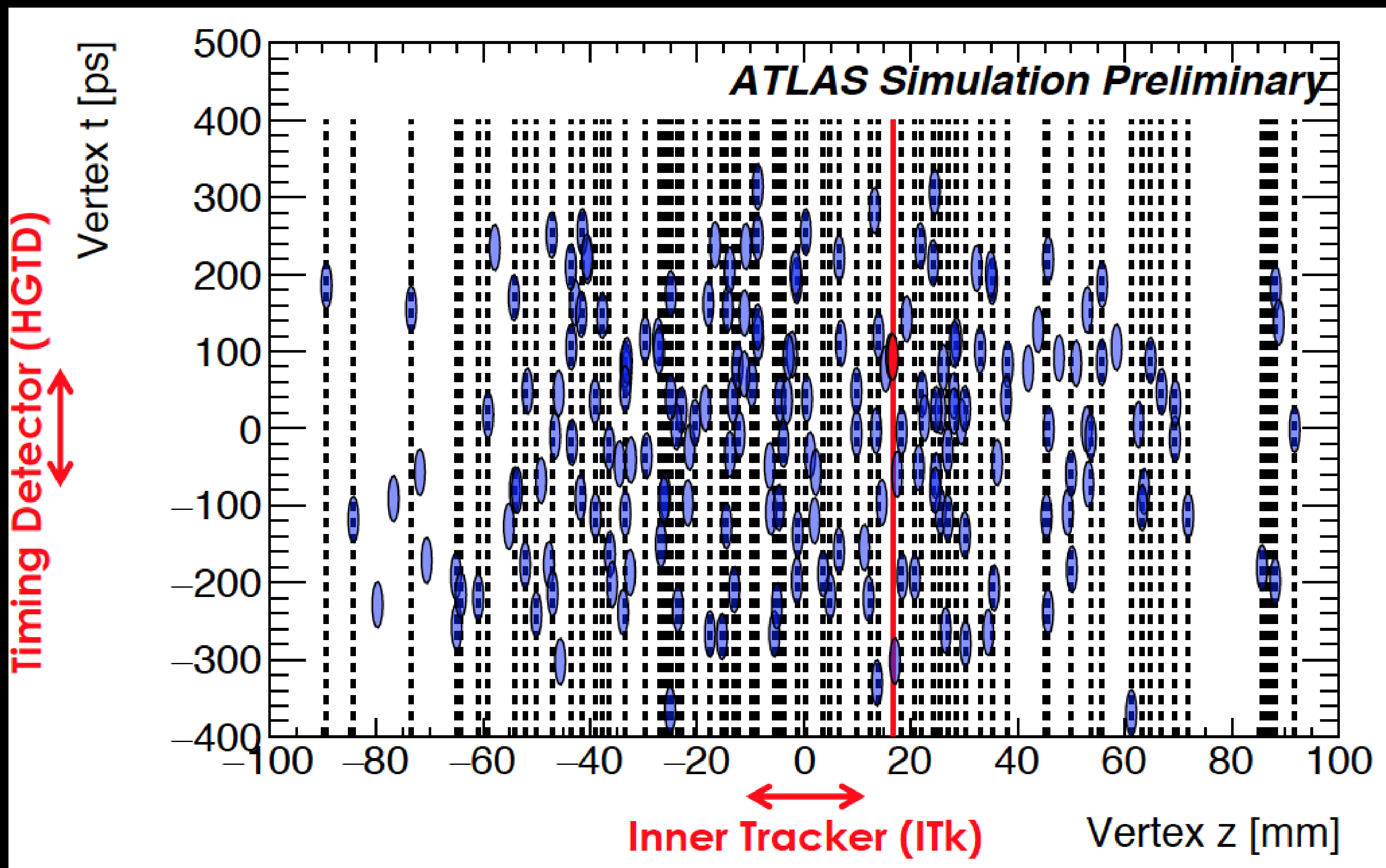
Thinner detectors



σ(t) ~ 30 ps achievable up to $1.5 \cdot 10^{15}$ n_{eq}/cm^2 using Boron+Carbon



TIMING



Exploit the time spread of collisions to reduce pileup contamination

MECHANICS & COOLING

Vital that module concepts, cooling and mechanics solutions come hand in hand with detector design!

New module concepts with TSV

- Comparison between WB and TSV on board integration

Sensor 200µm

Wirebonds for sensor HV bias

ASIC wirebonds

Chip 750µm

Area for chip periphery

WB extenders

Campbell et al, IWORID 2015

Sensor 500µm (edgeless)

Wirebond for sensor HV bias

Chip thinned to 120µm

BGA connections

0.8mm 1mm

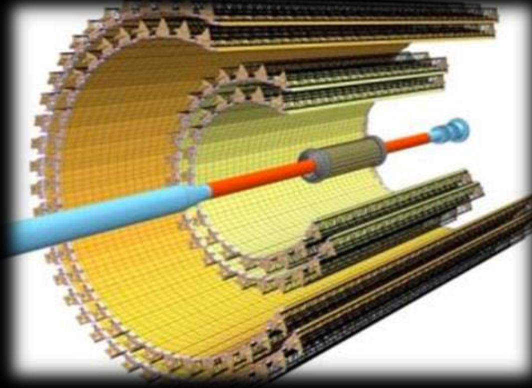
LETI

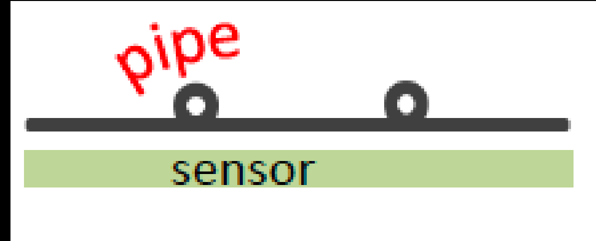
- In AIDA-2020 WP4, the Bonn group is driving an effort for processing Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips.
- AIDA2020 WP2 is also financing a Proof-of Concept project to develop a reliable TSV technology with Fraunhofer IZM

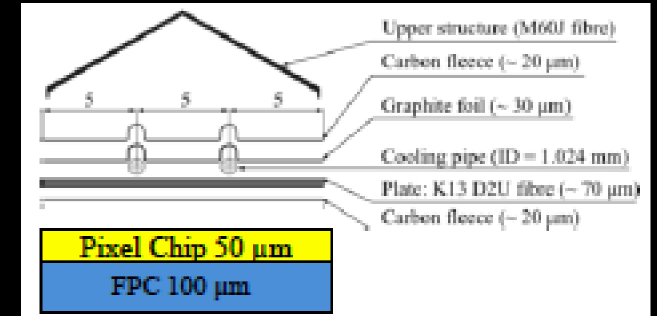
Fabian Hügging, N. Owtscharenko, D.-L. Pohl, N. Wermes - Physikalisches Institut - University of Bonn
T. Fritzsch, O. Ehrmann, H. Oppermann, M. Rothermund, Piotr Mackowiak, Kai Zoschke - Fraunhofer IZM Berlin

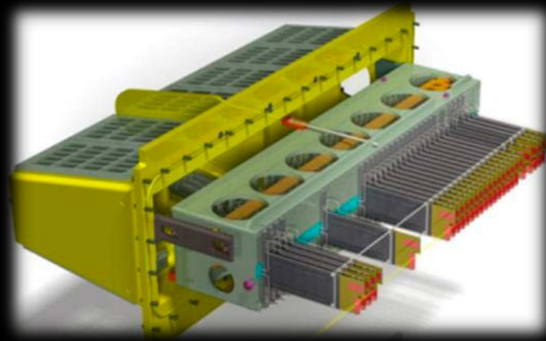
Gargiulo

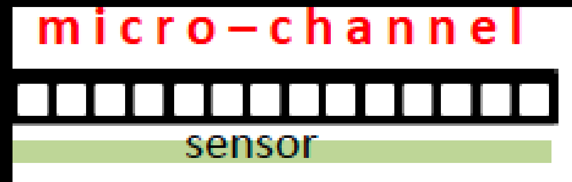
Light Support Structures

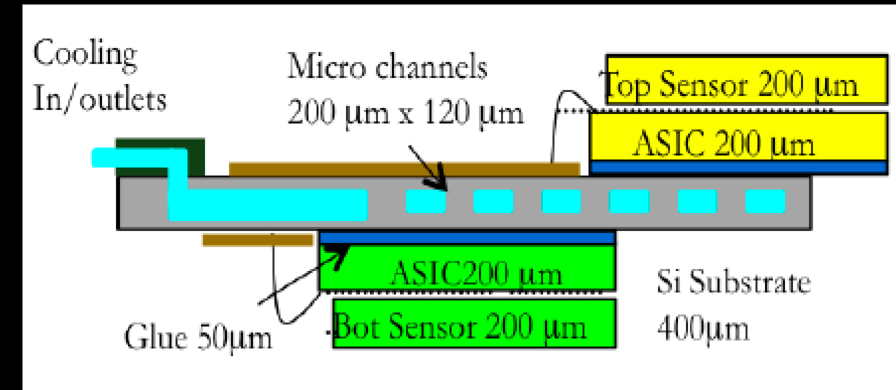


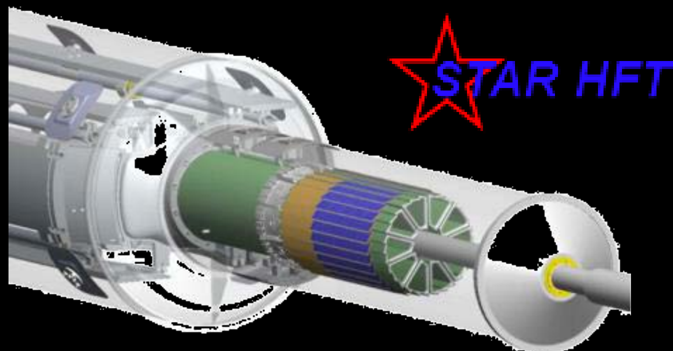


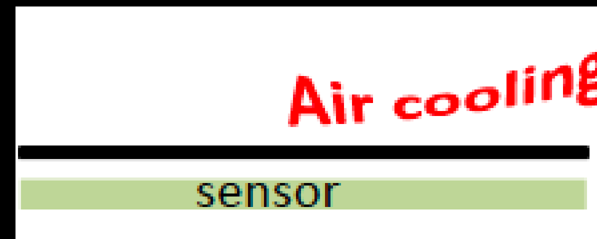


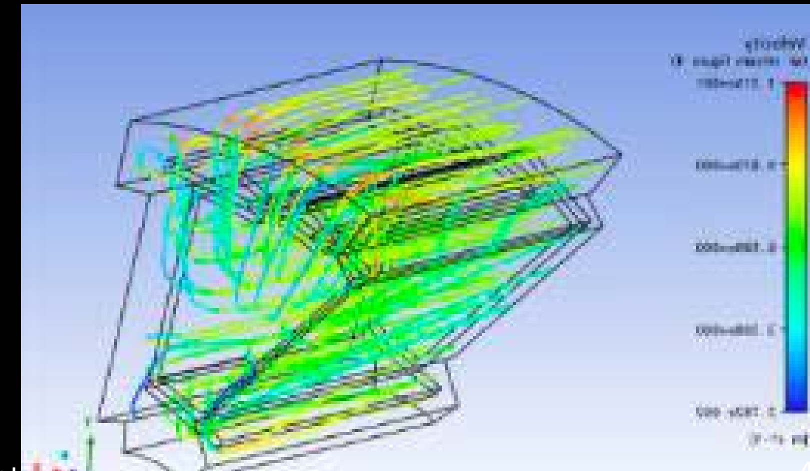






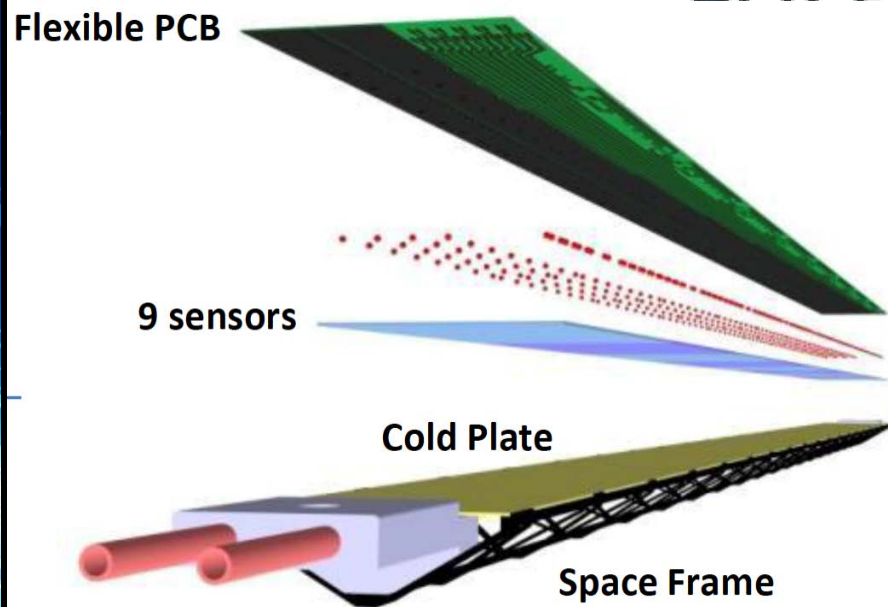


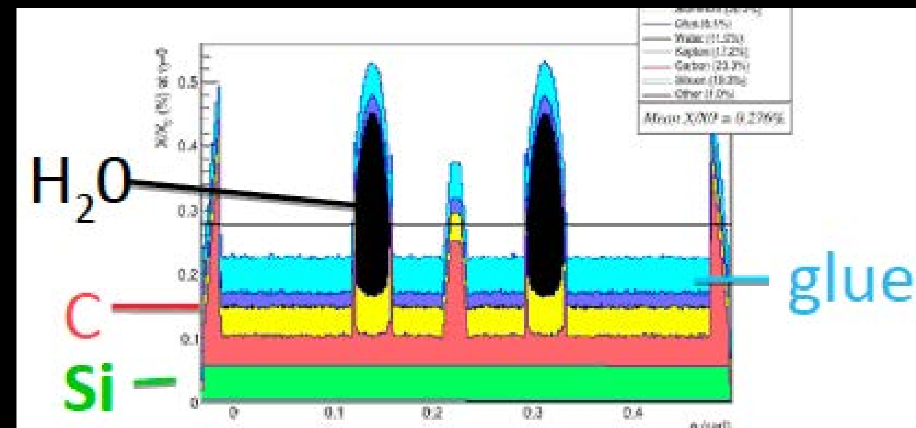


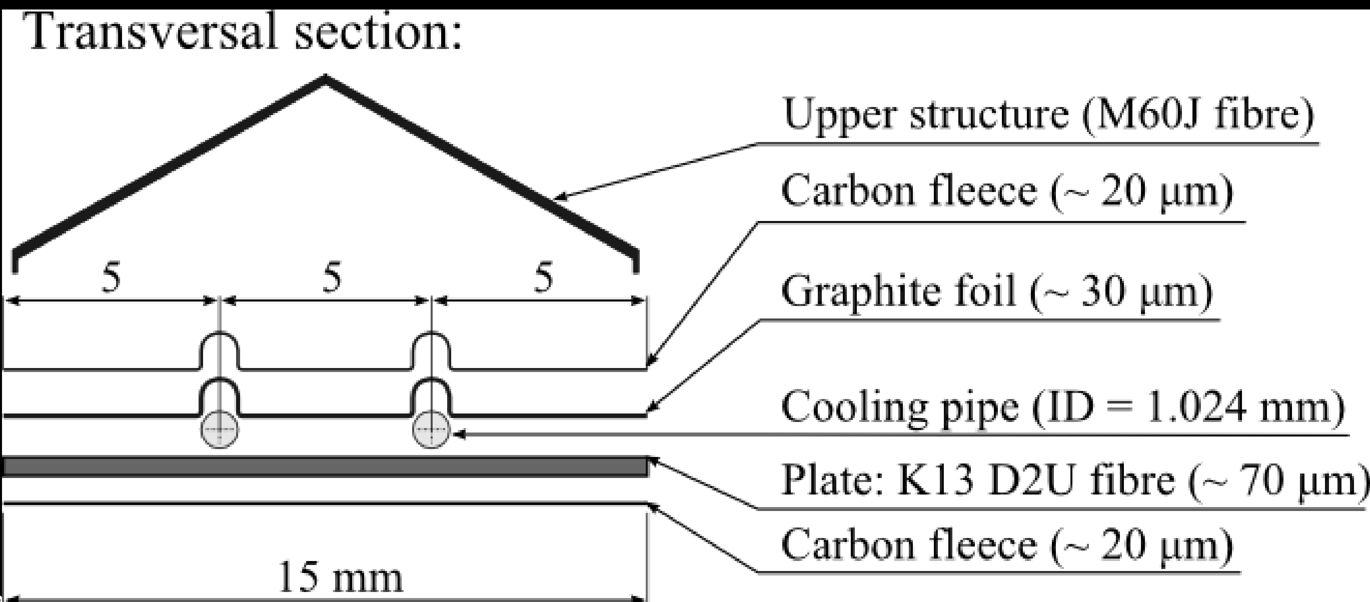


ALICE

Power density<100 mW/cm^2
Length 290 mm
Material 0.3 X_0
Throughput (@100KHz)< 80 Mb/s/cm^2

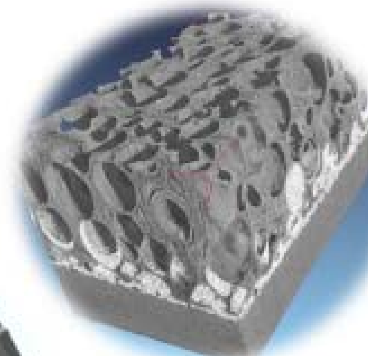






ATLAS IBL stave operated @ -20°C, CO_2 evaporative

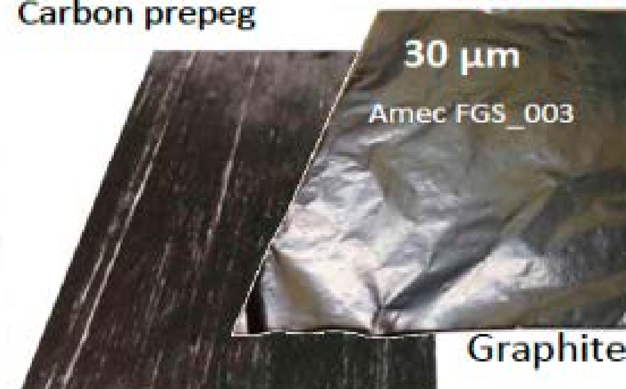
«pipe»
materials



- High Thermal Conductive (HTC) material carries the heat to a pipe with coolant.
- Pipe embedded in carbon foam or graphite foil
- Pipe can be either metallic or plastic

ALICE ITS stave upgrade, operated @ <30°C, water leakless

High thermal conductivity
1500 W/mK



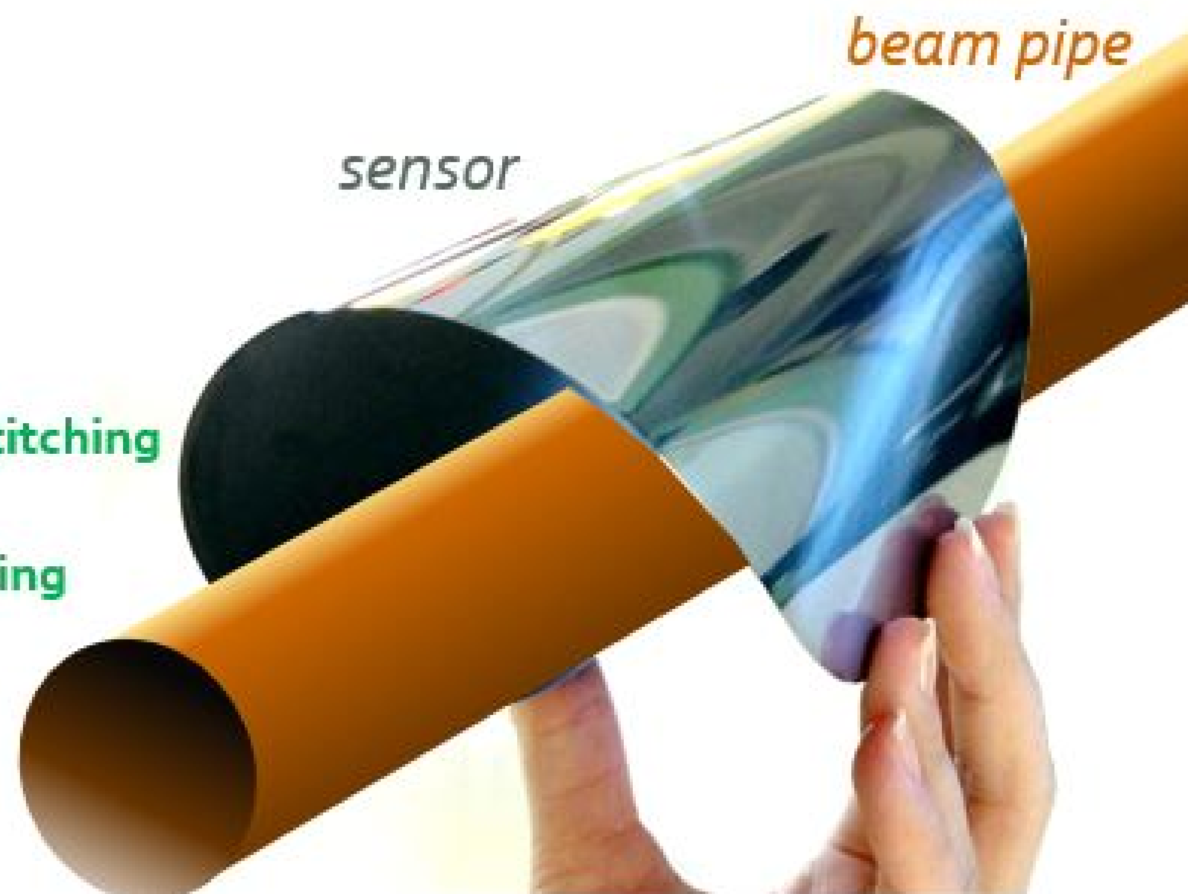
R&D

x/Xo~ 0.3% per layer

Present limit

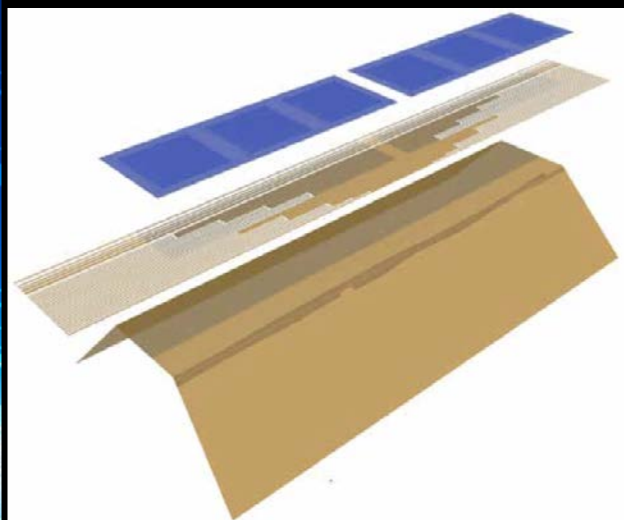
x/Xo< 0.1% per layer

New lepton collider requirements

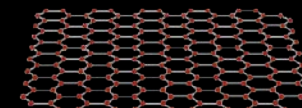


- ✓ **Eliminate liquid cooling**
  possible for power <20mW/cm2
- ✓ **Eliminate electrical substrate**
  possible if the sensor covers the full stave length: **Stitching**
- ✓ **Minimize mechanical support**
  exploit flexible nature of the silicon (<50μm): **Bending**

MATERIAL REDUCTION



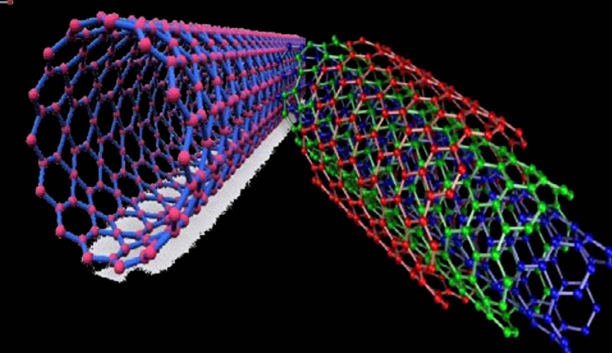
- 50 μm DMAPS
- 25 μm Kapton Flexprint
- 50 μm Kapton support frame
- < 1‰ Radiation length



Carbon Nanotubes

Allotrope of carbon with a cylindrical nanostructure

Very high Therma Conductivity (T_C=3500 W/mK)



Graphene

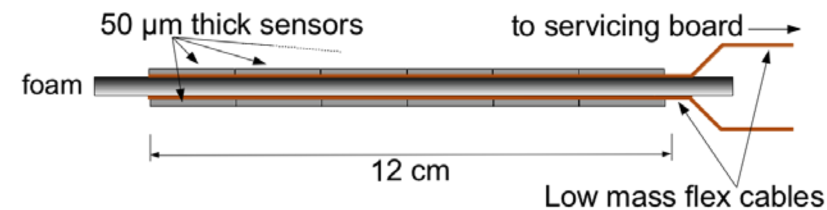
One atomic-layer thin film of carbon atoms in honeycomb lattice. Graphene shows outstanding thermal performance, the intrinsic T_C of a single layer is 3000-5000 W/mK

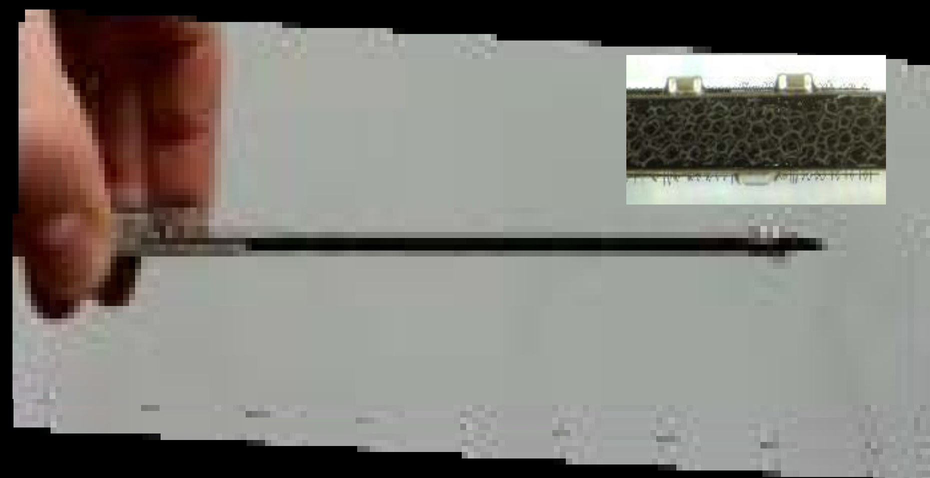
Conclusions

BEAST at BELLE

Bristol, DESY, IPHC

- Amazing progress on low-mass designs and improved radiation hardness
- Pixel sizes approaching linear and circular e^+e^- needs
- MAPS and DMAPS are the technological front runners but advances in 3D integration might blur the distinction between hybrid and monolithic pixels
- Interesting development on precision timing that should be watched

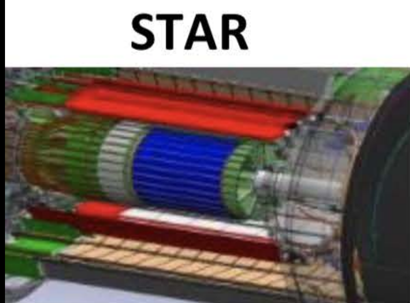




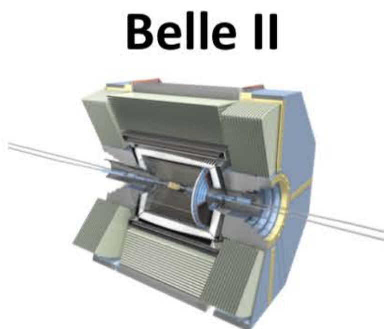
- PLUME-2
- 2x6 MIMOSA-26 sensors
- Pitch 18.4 μm, Thinned to 50 μm
- 8 Mpixels
- 2 μm thick Si-carbide foam
- Material budget 0.4% X_0)

Rate and Radiation Levels

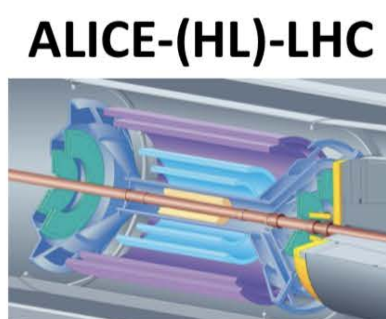
STAR



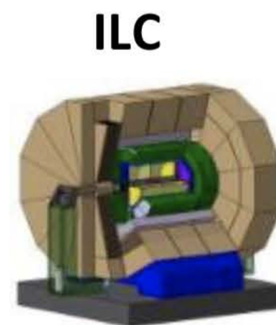
Belle II



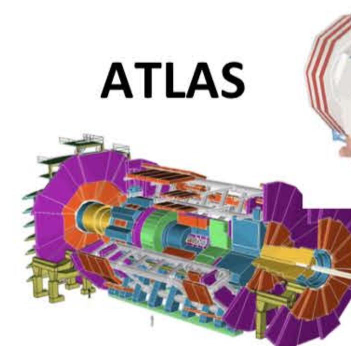
ALICE-(HL)-LHC

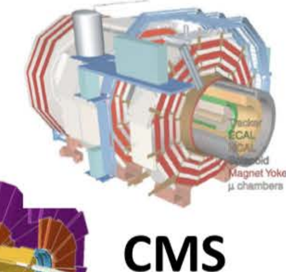


ILC



ATLAS





CMS

Numbers for innermost layers (r ≈ 5cm,) -> scale by 1/10 for typical strip layers (r > 25 cm)

	STAR	Belle II	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
						Outer	Inner
BX-time (ns)	110	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	10	250	1 000	1 000	10 000
Φ (n_{eq}/cm^2)	few 10^{12}	3 x 10^{12}	> 10^{13}	10^{12}	$2x10^{15}$	10^{15}	$2x10^{16}$
TID (Mrad)*	0.2	20	0.7	0.4	80	50	> 1000

*per (assumed) liftetime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

in need for
- much less material
- higher resolution
- thinner strips & monolithic pixels

state of the art
- large area strips
- hybrid pixels

- even larger area
- radhard sensors
- higher rates R/O
- R&D of new types

- EXTRA SLIDES 3D INTEGRATION

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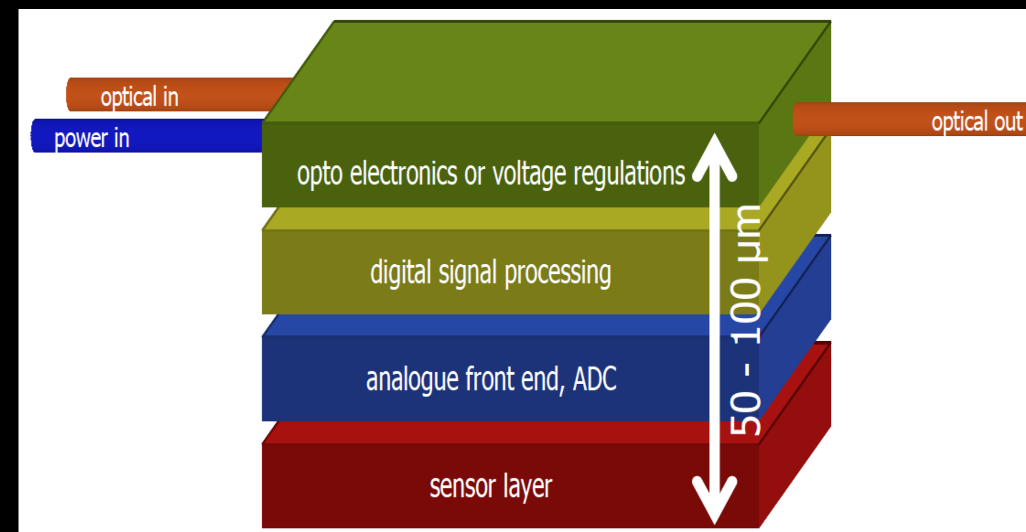
3D Integration

- " vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."
- 3D integration technologies (Through-Silicon Vias, low-mass bonding,…)

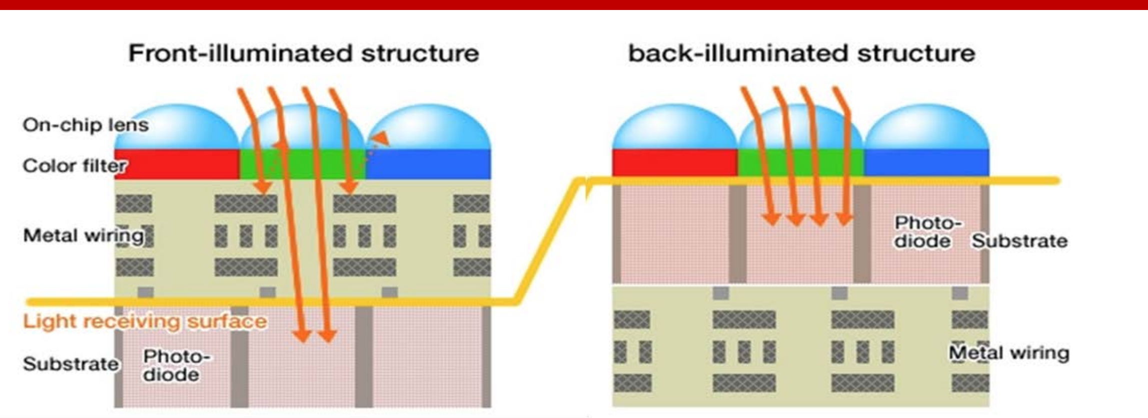


- Goals:
  - Improve resolution with smaller pixels and pitch to ≤ 20 µm
  - Preserve or even increase pixel-level electronic functions such as high data rates, large dynamic range, high resolution analog-to digital conversion and timing, sparsification, large memory capacity, and intelligent data processing which contributes to limiting the minimum size of pixel readout cells
  - Develop large area detector with minimum or no dead area
  - Decrease amount of material: thin sensor and electronics reduce errors in track reconstruction due to multiple scatterings of particles in the detector system (50 -100 µm total thickness)

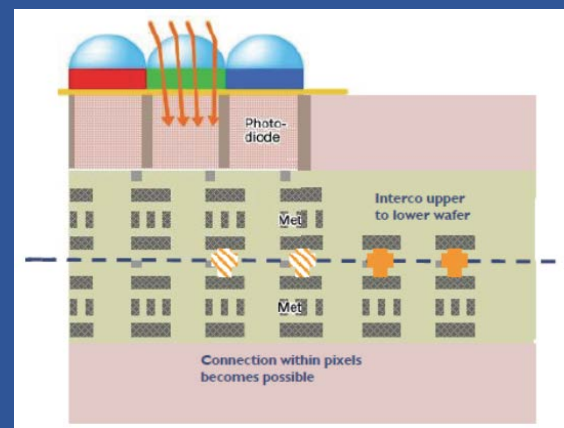
Industry trends

- Stacking CMOS image sensors with a CMOS mixed-signal readout chip, both in O(10) nanometer technologies
  - Use high density bonding for µm or sub-µm pixels, wafer thinning to a few µm
  - Limited use of TSVs
- Semiconductor companies (such as TSMC, LFoundry,…) are involved in these developments
- The resulting architectures may stimulate interesting ideas for particle tracking detectors

BSI (Backside Illumination) optical sensors were developed to improve light efficiency etc.

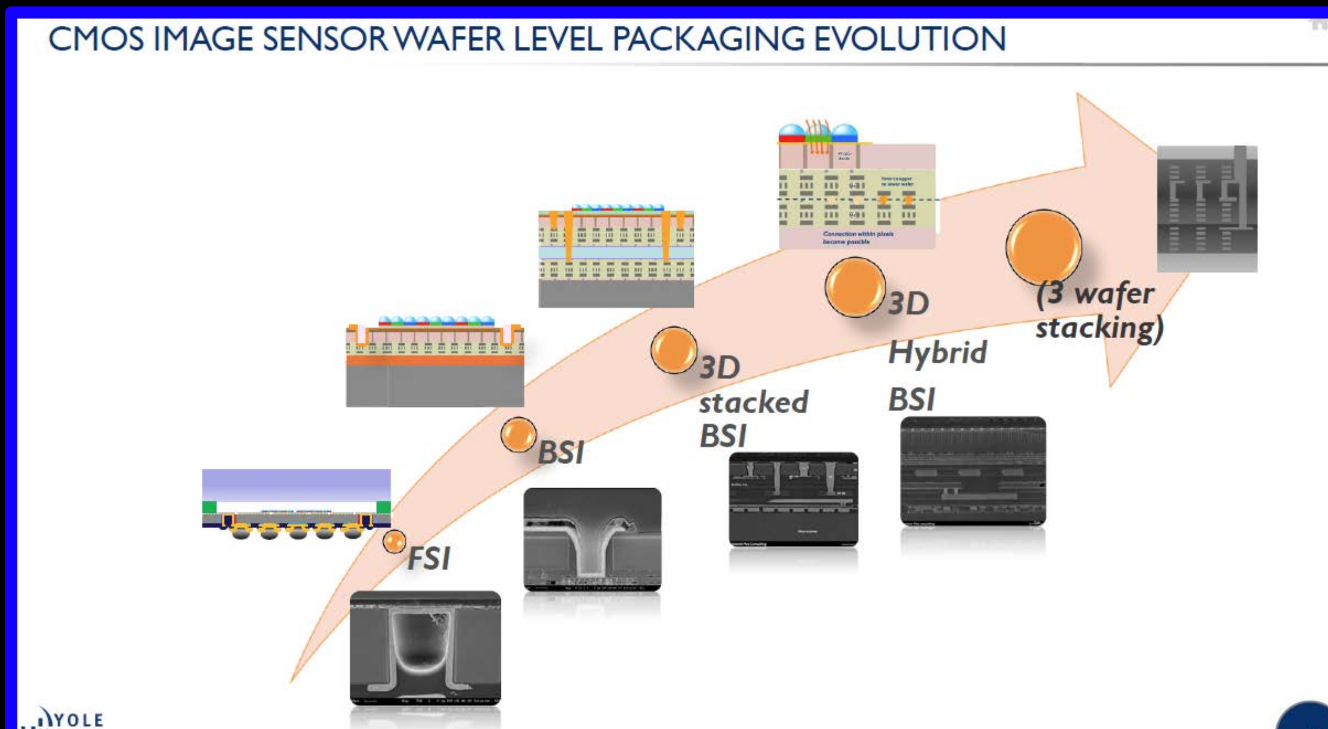


Hybrid/Stacking is developed to improve fill factor, speed, low power, …

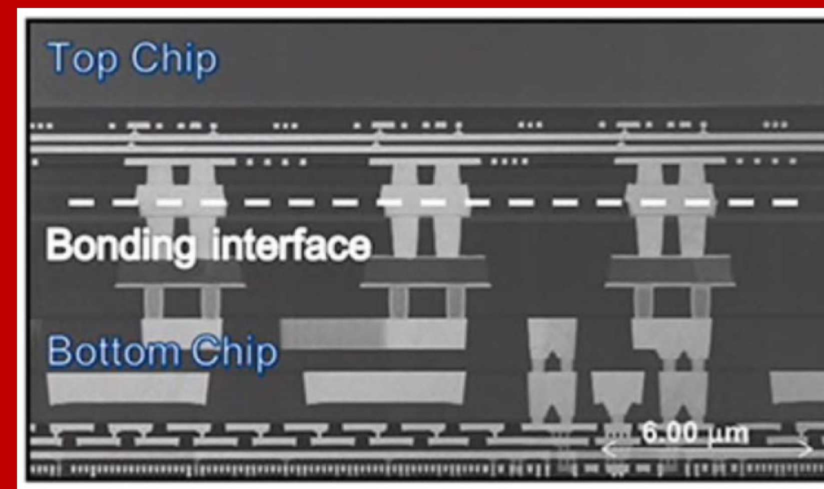


Industry trends

- At ISSCC 2018, six out of the ten papers on image sensors use a 3-D stacking process to preserve most of the top layer area for light sensing, while keeping the readout and image-signal-processing circuits on the bottom layer.

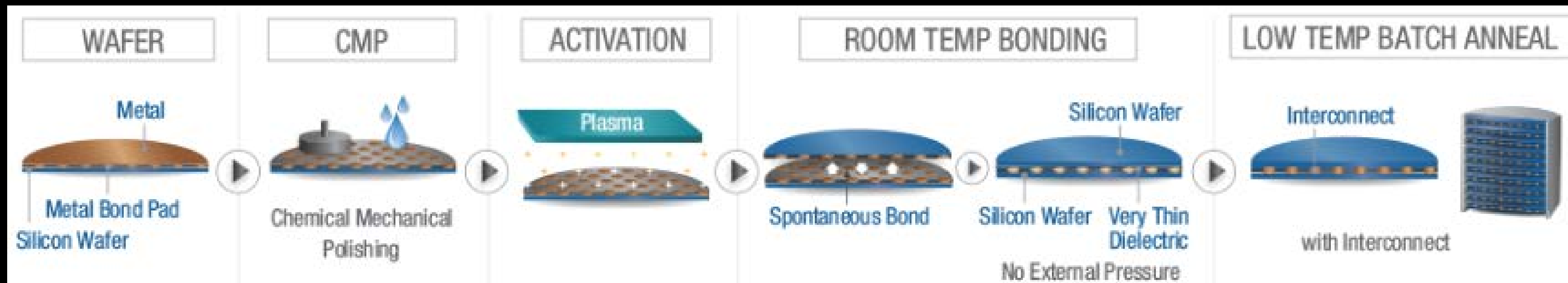


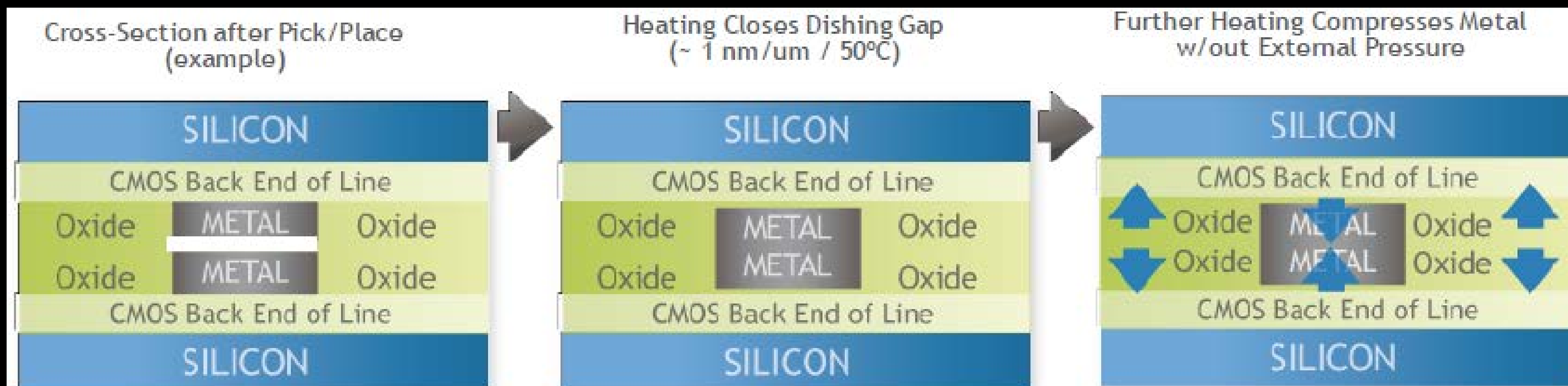
SONY M. Sakakibaraet al. ISSCC 2018,
A Back-Illuminated CMOS Image Sensor
Wafer level stacking: pixel size 6.9 µm x 6.9 µm,
14-bit pixel-level ADC logic



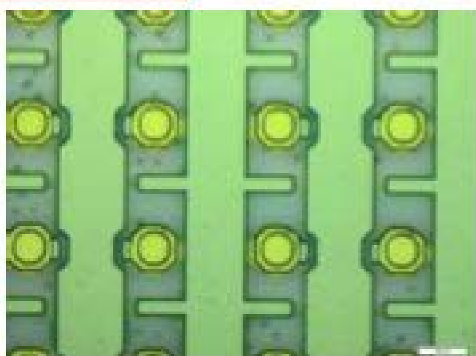
Industry trends

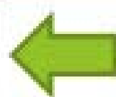
- Hybrid Stacking





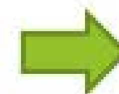
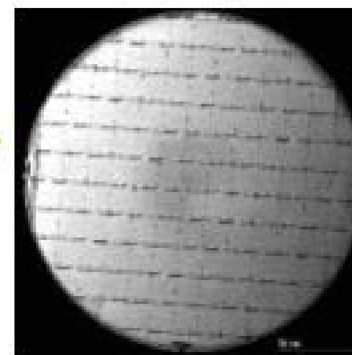
TIMEPIX3 (SI AT 50 MICRONS) WITH TSV-LAST FUNCTIONAL RESULTS (2015)

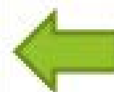




Under bump Metallurgy (TiNiAu) on pixel pads

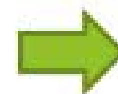
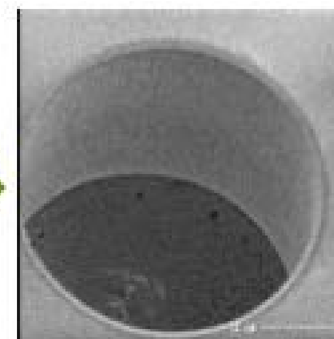
Wafer bonding on temporary carrier (SAM inspection showing good bonding)

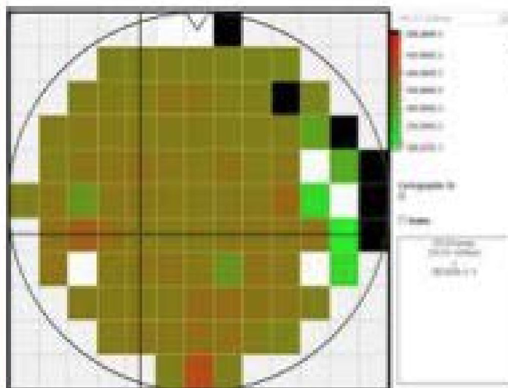





Wafer thickness profile after thinning to 50 µm (53 +/- 2 µm)

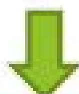
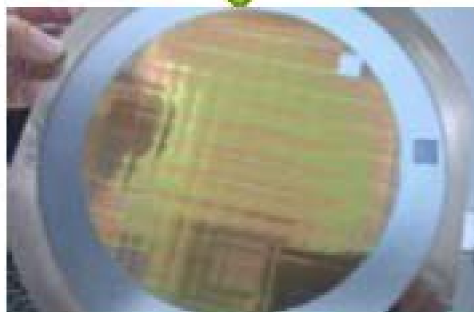
TSV etching to bottom oxide (diameter = 40 µm)

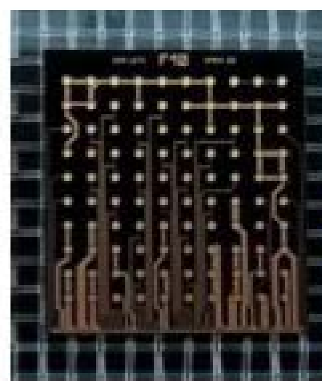
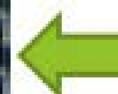





Daisy chain TSV resistance mapping
Yield = 88%

50 µm Thinned timepix wafer diced on tape

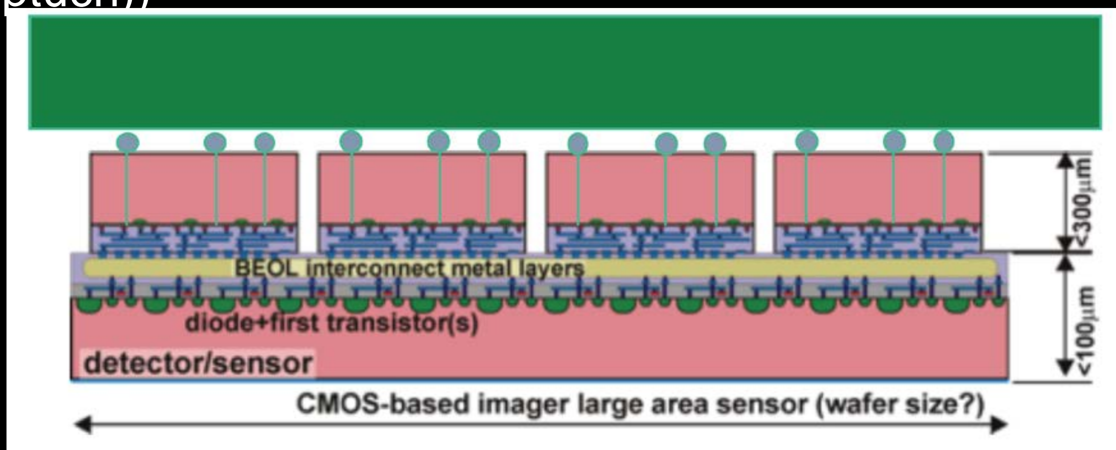



Timepix die from back side showing redistribution of I/O signal on BGA pads

3D integration and CMOS sensors

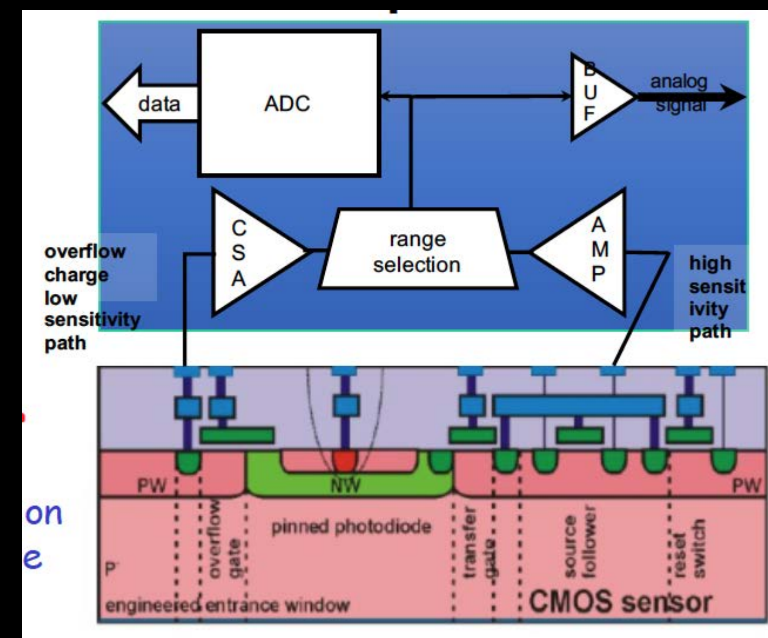
- A CMOS sensor for imaging or particle tracking can be augmented by an additional layer of dedicated high performance electronics, 3D integrated at the pixel level.

FLORA: Fermilab-LCLS CMOS 3D-integRated with Autogain
2M pixel, soft 0.2-2 keV X-rays, high speed 10kfps, high dynamic range 10^3 camera for LCSL II, (Fermilab-SLAC, P.I. G. Carini, G. Deptuch))



- exploiting good features of both technologies
- multiple metal layers on sensor/interposer for routing
- yield-optimized size of ROIC ASICs

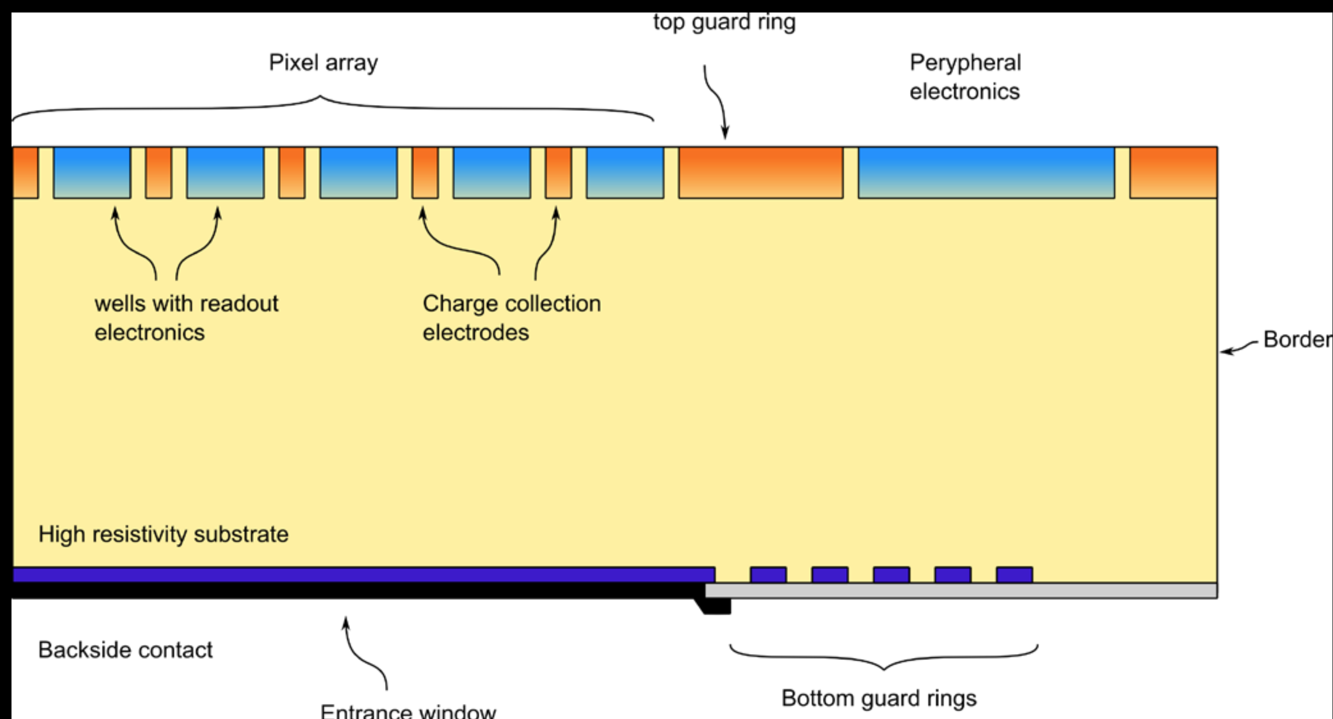
Mixed-signal Readout ASIC
advanced process node (65 nm)



Monolithic Active Pixel Sensor
OPTO-type process minimal circuitry for the conversion of the charge packet into voltage

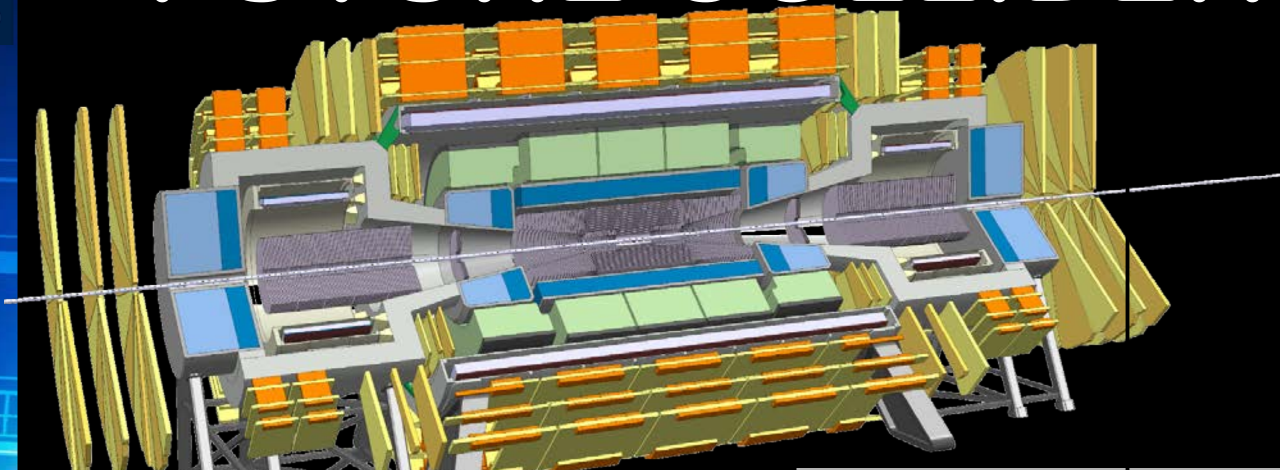
The XIMOS project

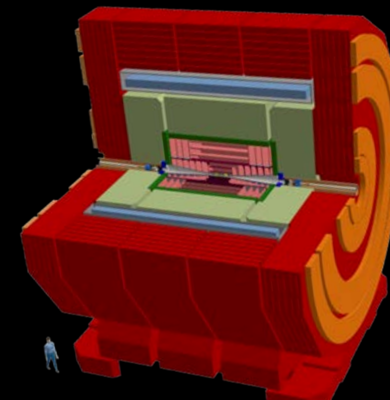
- High frame rate, high dynamic range X-ray and charged particle imager based on a large scale fully depleted CMOS pixel sensor for free electron lasers (FEL) and synchrotrons
- 110 nm CMOS sensor layer: CMOS sensor, preamplifier with dynamic signal compression, shaper
- 65 nm mixed-signal readout layer: pixel ADC, memory, data readout
- Relatively large pitch (100 μm x 100 μm)
- ≥ 9 bit amplitude resolution (in-pixel ADC)
- dynamic range 1 – 10^4 photons
- capability to store at least 500 events per pixel;
- capability to operate both in a direct readout mode (for FELs with constant pulse rate) and in a store-locally/read-out-later mode (for FELs operated in a burst mode, as the Eu-XFEL
- Tolerance to about 1GGy of total ionizing dose for 5 Kev X-rays



- CMOS pixel sensor with a thick fully depleted substrate (500 μm)
- Thin entrance window with shallow junction and minimum amount of dead material in the passivation stack (for low-energy X-rays)
- Multiple guard-ring termination structure on the back-side, minimizing the dead area at the sensor edge (device buttability to cover large detection areas in practical applications)

FUTURE COLLIDER DETECTORS





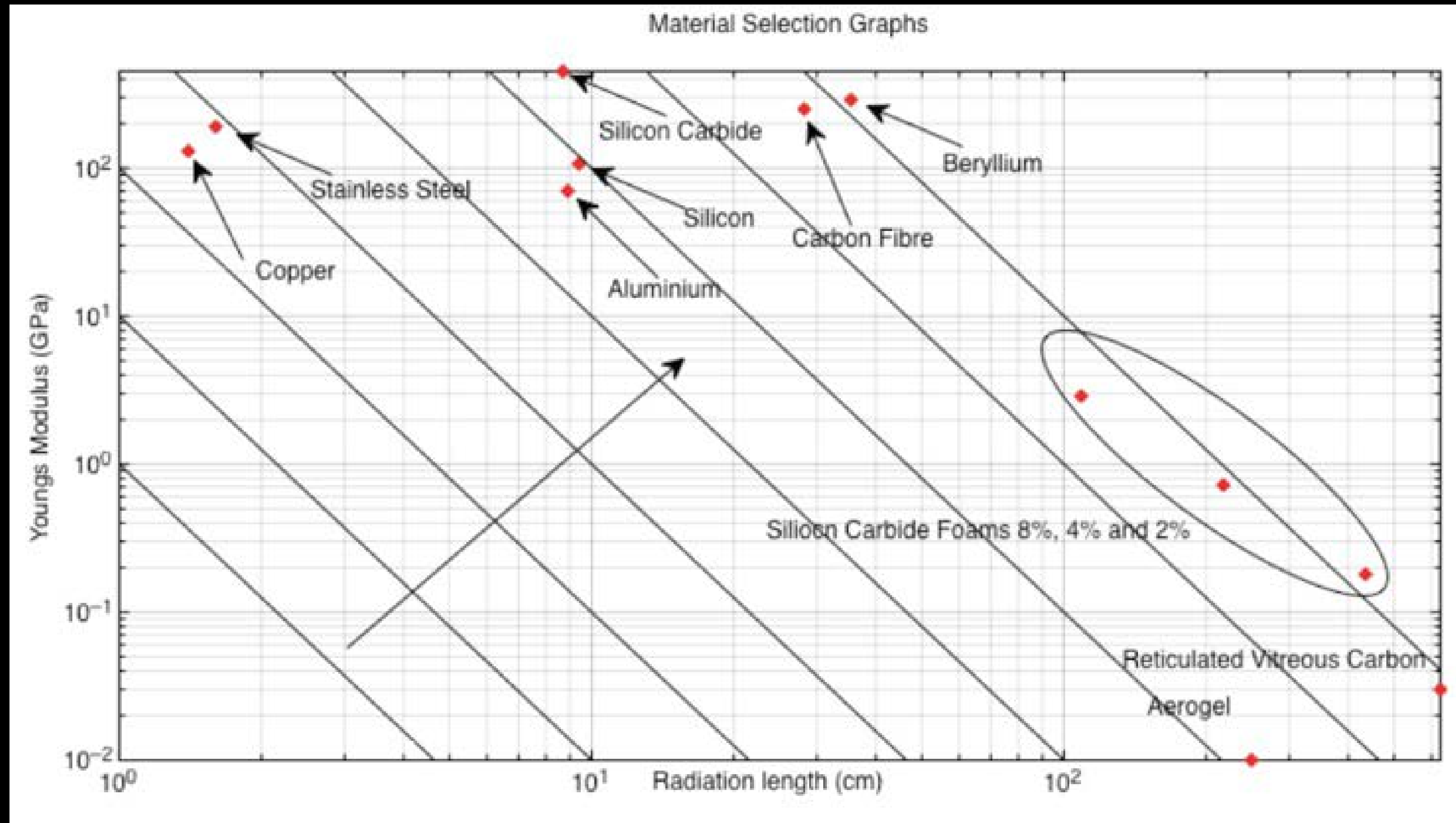
FCChh, HE-LHC | **hh collisions** | **e^+e^- collisions** | *CLIC, FCCee, ILC, CEPC,…*

- Large dimensions (50m)
- High radiation Level (up to 90MGy)
- 4T 10m solenoid
- Forward solenoids 4T
- Silicon tracker Radius 1.6m, Length 32m radiation damage is a concern
- Barrel ECAL LAr/ Barrel HCAL Fe/Sci
- Endcap HCAL/ECAL LAr
- Forward HCAL/ECAL LAr 2-4x better granularity than e.g. ATLAS Silicon ECAL and ideas for digital ECAL with MAPS
- Muon system

- Standard dimensions
- Low radiation Level
- 4T, 2T
- Silicon tracker unprecedented spatial resolution (1-5 μm point resolution)
- very low material budget (0.1X%)
- Dissipated power (vertex) (<50mW/cm²)
- Radiation level NIEL ($<4\times10^{10}$ neq cm^{-2}/yr)
- Radiation level TID (<200 Gy/yr)
- Barrel fine grained calorimeter
- Compact Forward calorimeter

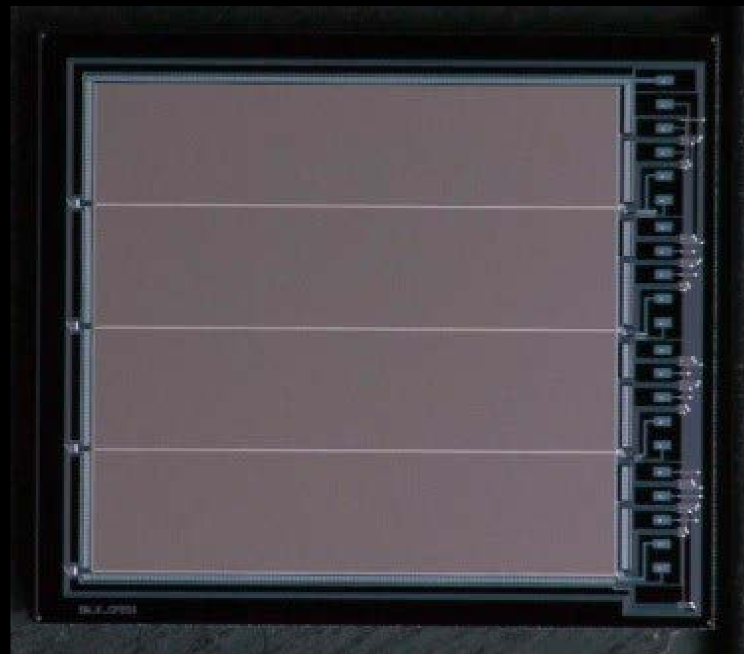
R&D

Light Support Structures

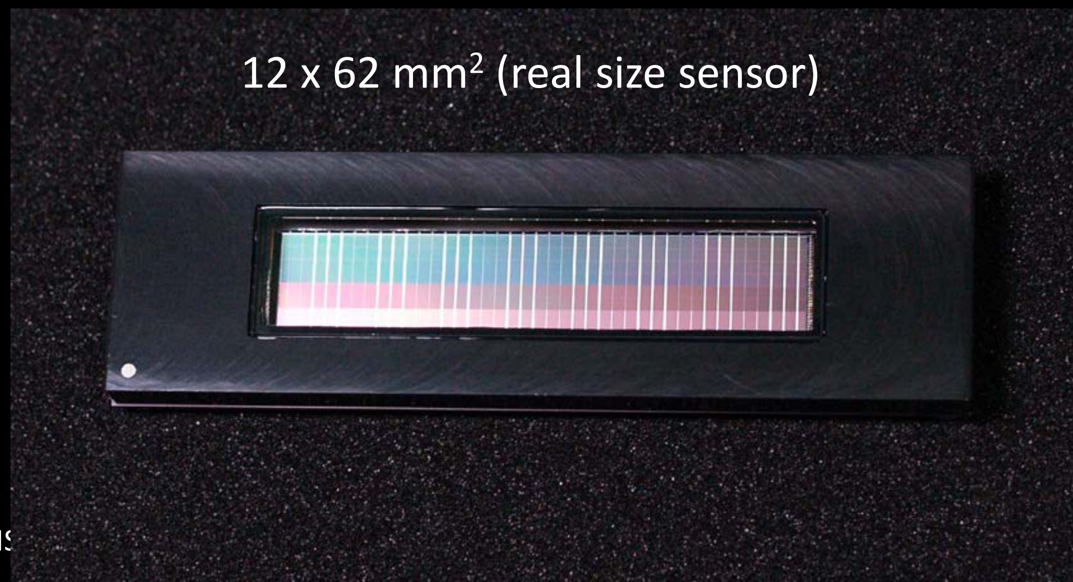


Semi-integrated technology: FPCCD

- Fine Pixel Charge-Coupled Devices (FPCCP) studied for ILD vertex detector
- Semi-integrated technology (separate r/o ASICs)
- Thickness of 50 μm, but material pushed to endcaps
- Trade-off:
  - Pixel pitch down to 5 μm ➠ 1.4 μm resolution for single pixel hits
  - Integrate over full ILC bunch trains ➠ no time stamps
  - Background rejection by pattern recognition
  - Operation at -40 C in cryostat using CO_2 cooling



FPCCD prototypes
(6 X 6 mm^2)
Pixel pitch 6, 12, 18, 24 μm



12 x 62 mm^2 (real size sensor)