Status of LHCb upgrade

With emphasis on electronics aspects

Upgrade Plan
Electronics Architecture
Sub-detector Status
Common Developments
Conclusions and Timescales

Ken Wyllie, CERN,
on behalf of the LHCb collaboration

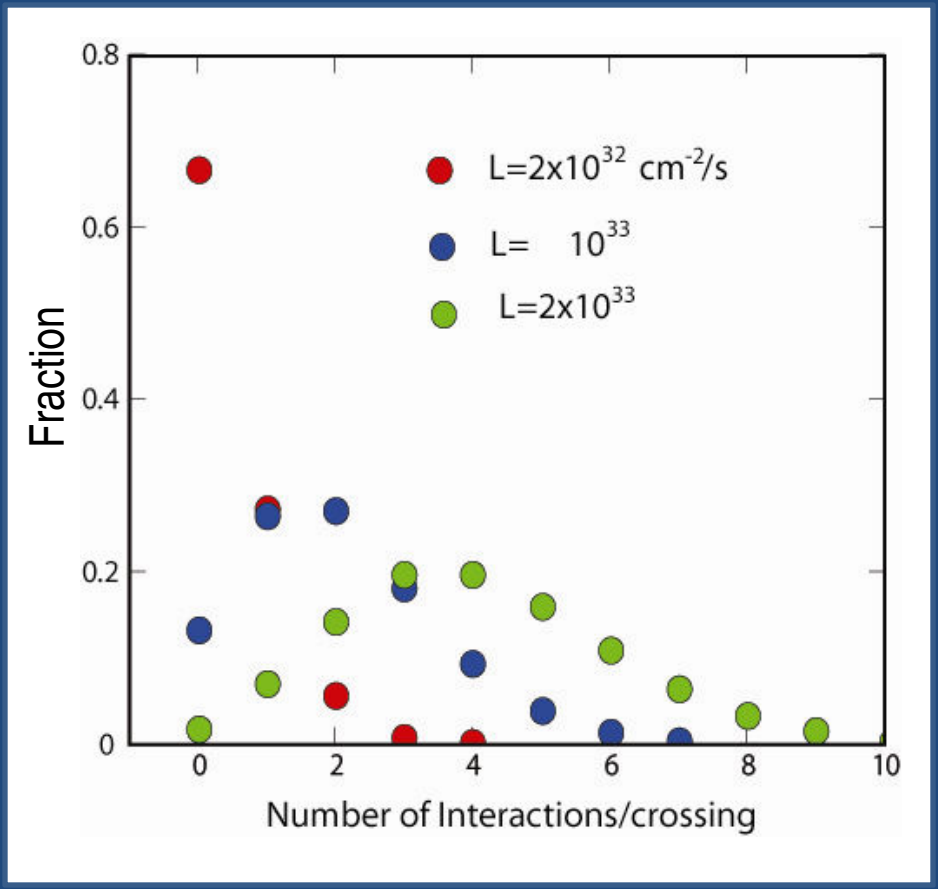
Reminder of upgrade plan

Run existing LHCb and collect 10 fb^{-1} in 5 years at $L = 2 \times 10^{32}\ cm^{-2}s^{-1}$

UPGRADE

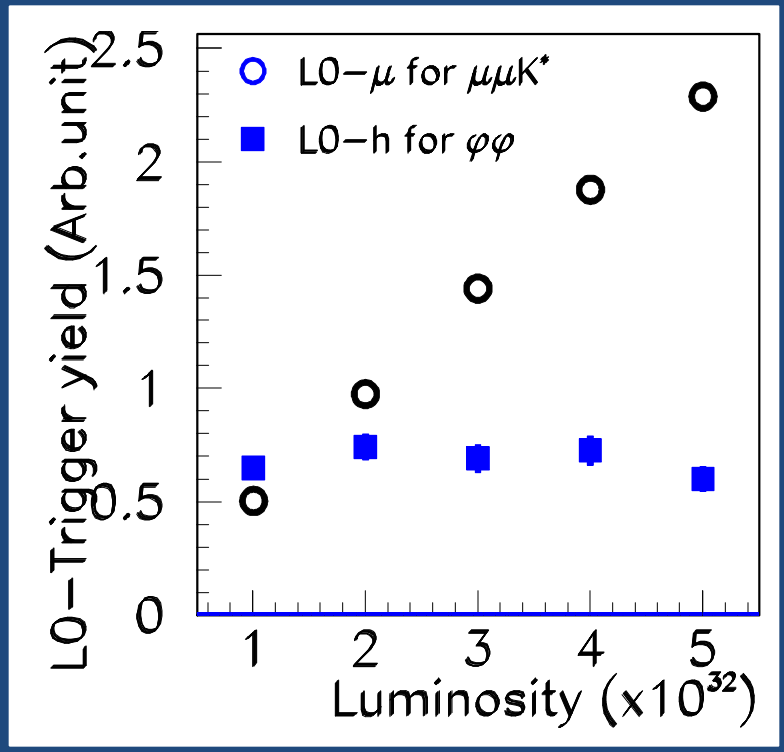
Collect 100 fb^{-1} in 5 years at $L = 2 \times 10^{33}\ cm^{-2}s^{-1}$

This is independent of SLHC



Requirements for upgrade

- Remove limits imposed by current L0 trigger
- Ship all data from every bunch-crossing to PC farm
- Efficient triggering in farm



- Work with LHC to define best scheme for 2 x 10^{33}

Electronics upgrade philosophy

Try to optimise:

- Cost
- Manpower
- Time (development, production, installation)

1. Re-use existing electronics & infrastructure as much as possible

2. Develop common solutions for use by all sub-detectors

Estimate of number of links

	No Zero-Suppression	Zero-Suppression	Existing LHCb
# links (3.2 Gbit/s)	55,000	10,000	6,000

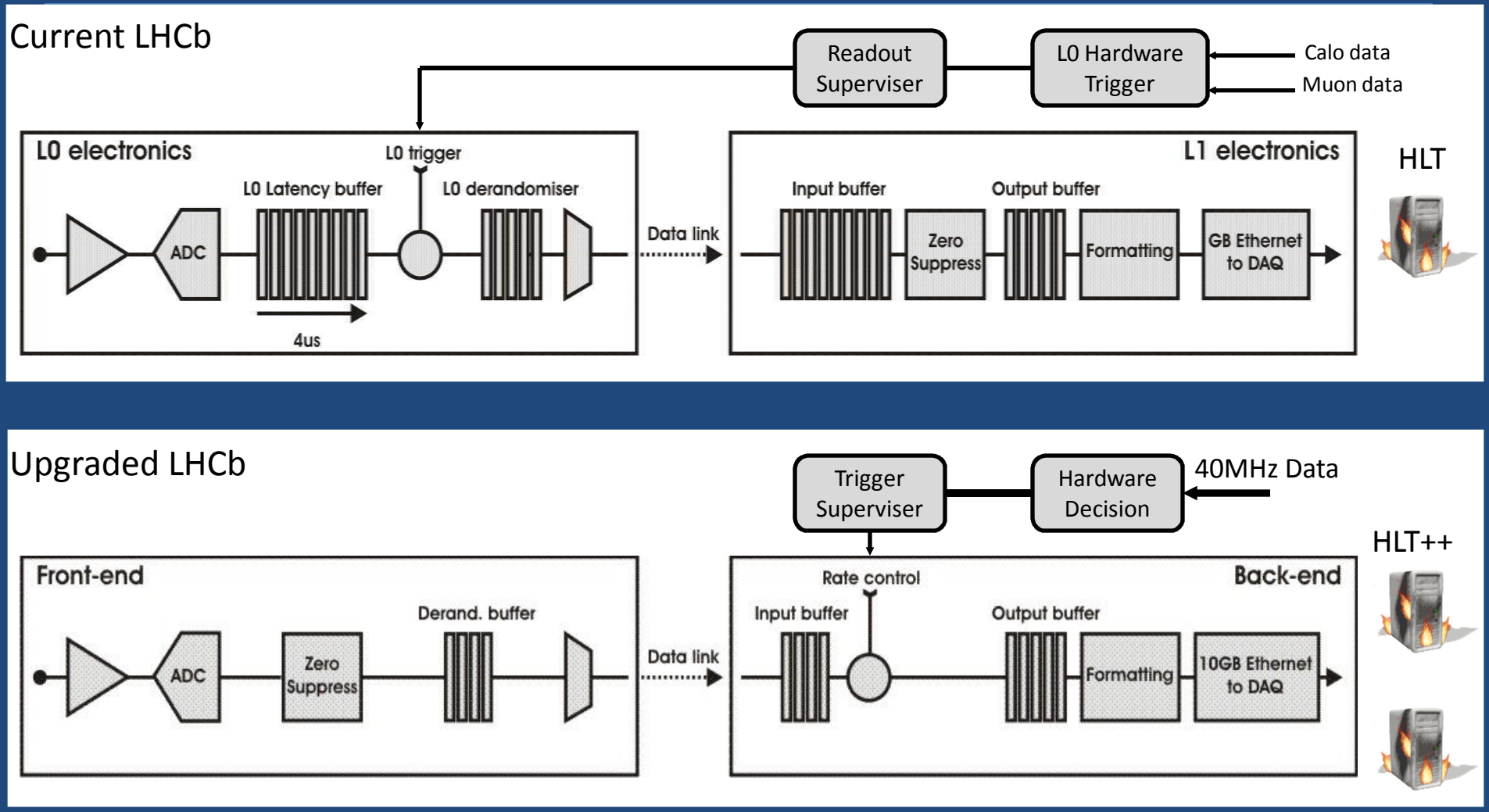
Clear cost saving in links by zero-suppressing in the front-end

But:

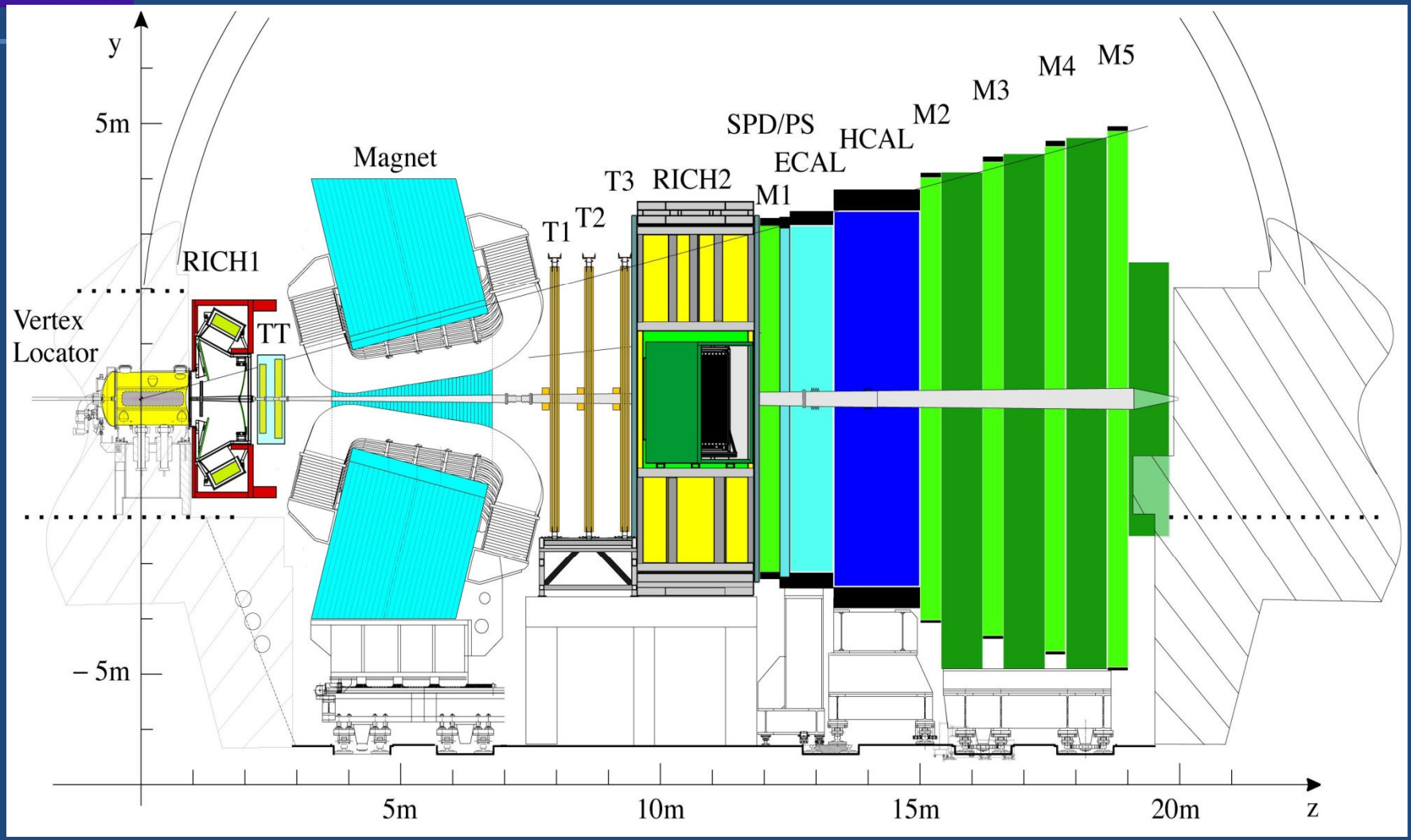
- Complex algorithms in front-end & careful monitoring required
- Event-sizes & statistical fluctuations have to be well understood

Use of programmable logic encouraged (see later)

Electronics system architecture



Sub-detectors & their electronics



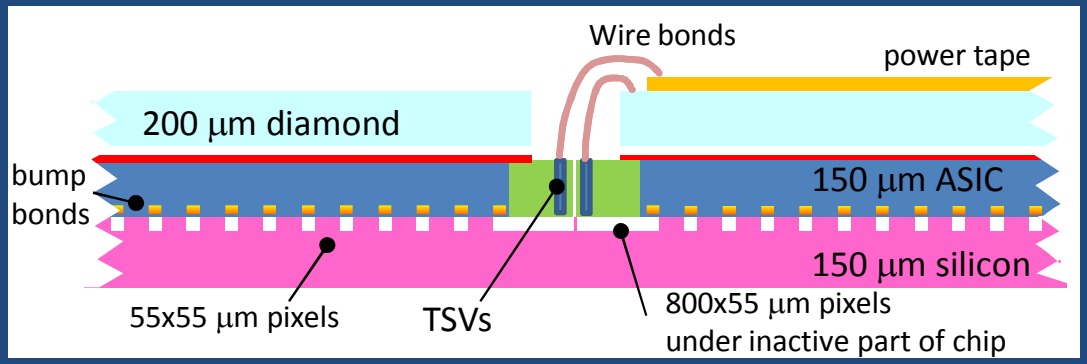
For more details on detector technologies,
see talk from Paula Collins at previous LHCC upgrade session

VELO electronics

Two detector options (& electronics) pursued:

Pixel solution - baseline (50 x 50 μm pixels)

- Big progress on front-end chip architecture VeloPix
- Strong overlap with Timepix2 project
  Chip design now starting (130nm CMOS) with common features
- Technology proven up to 500 Mrad TID (Medipix3)
- Work on electronics in parallel with module/mechanics



Silicon strip solution - backup

See Tracker slides

Tracker electronics

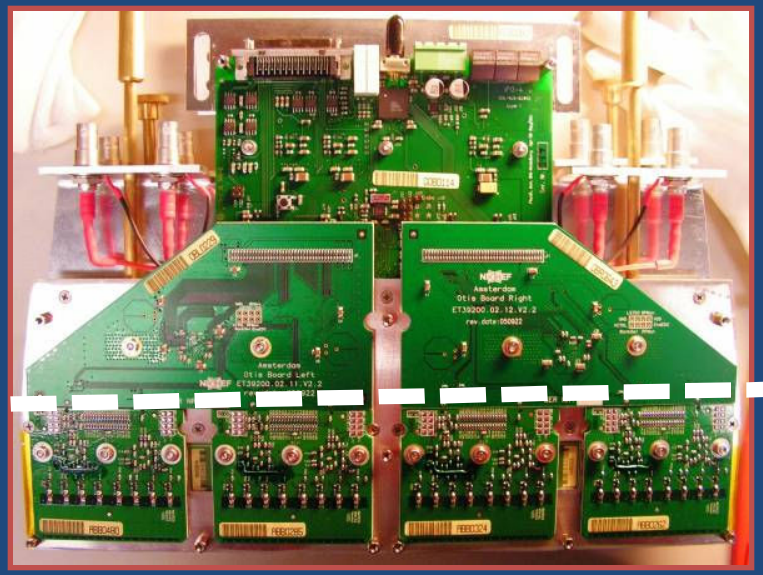
New front-end electronics required for Inner Tracker

Silicon strip solution

- Design now starting based on specs of current detector
- Big overlap with other developments (eg ABCnext, VFAT…….)

Re-use analog front-end of Outer Tracker
couple to new digitising card:

TDC ASIC replaced with ACTEL FPGA
Prototype working well



RICH electronics

MAPMT (probable photon-detector)

Two options being investigated:

1. Dedicated front-end development
2. Common development with Tracker

PMT characteristics under study to determine:

- Analog electronics specs (gain variation, cross-talk)
- Readout architecture (binary or ADC)

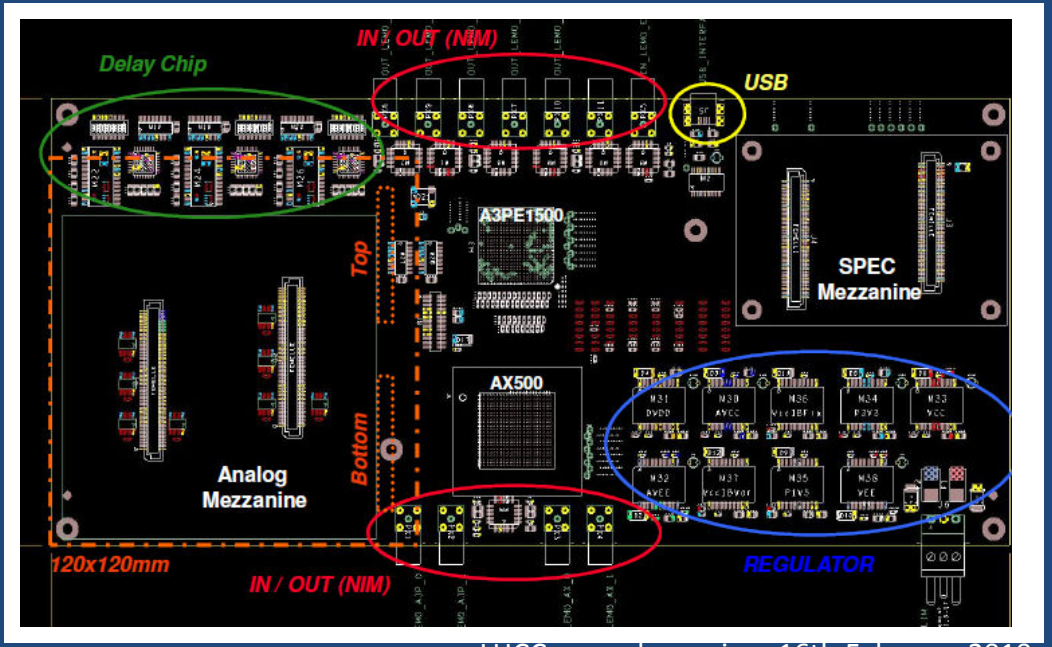
Calorimeter electronics

Two main developments:

1. New front-end amplifiers designed to compensate for reduced gain of PMTs
2. Digital processing + data packing designed for ACTEL FPGA

Incorporated in test board

Testing planned for March - April



Muon electronics

Re-use analog front-end

(to be verified for high occupancy regions)

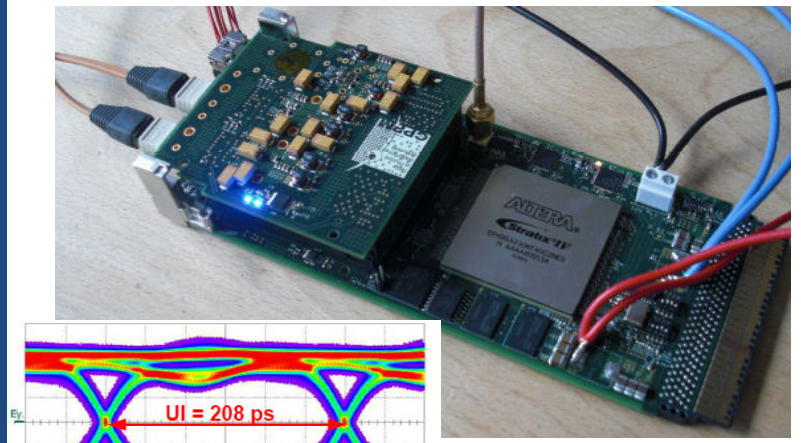
Digital processing + data packing to be re-designed:

implementation under study (ACTEL FPGA could be possible)

Common developments

TELL40: Common back-end readout board

- Tests of high-speed links on proto-board
- Parallel optical I/Os (12 x > 4.8 Gb/s), GBT compatible
- Proto-board under test



ACTEL FPGAs (Flash-based) for front-end modules

- Advantages over ASICs: re-programmable!!!
- Can they survive the radiation?
- Irradiation programme started on selected devices

Other developments

We will benefit from the 'White Paper' common R&D projects:

WP1: "Rad-hard technology & common building blocks"
support for ASIC designs, IP blocks

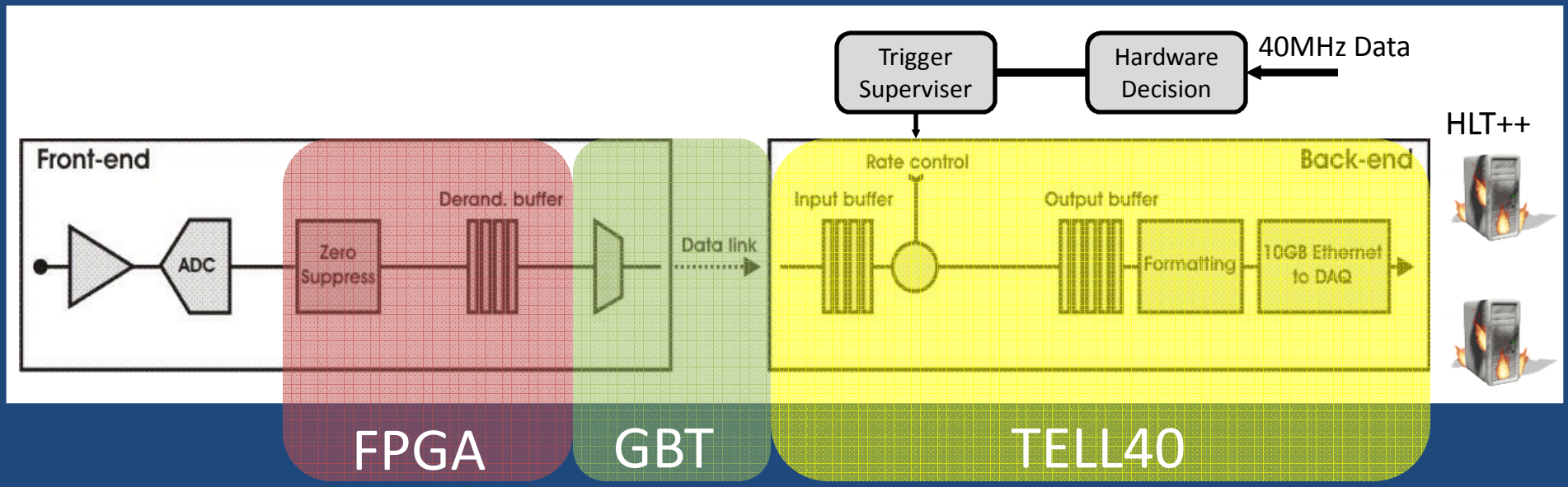
WP2: "On-detector power management"
DC-DC convertors, on-chip regulators …..


WP3: "Radiation-hard optical link"
GBT + Versatile link


WP6: "Interconnect Technology and Quality Assurance"
bump-bonding & through-silicon-vias for VELO

A large part of the existing infrastructure can be re-used (eg power supplies, cables)

Electronics system implementation



Timescales

Submission of Letter-of-Intent in 2010
with TDRs to follow later

LHC shutdown in 2012:
pre-preparation of infrastructure could be possible
(eg optical fibres, copper cables)

Upgrade ready for installation in 2016

Conclusions

All sub-detectors actively developing systems

Minimise work by re-using parts of existing systems but some detectors require completely new systems

Common developments progressing well

Upgrade ready for installation in 2016

Spare slides