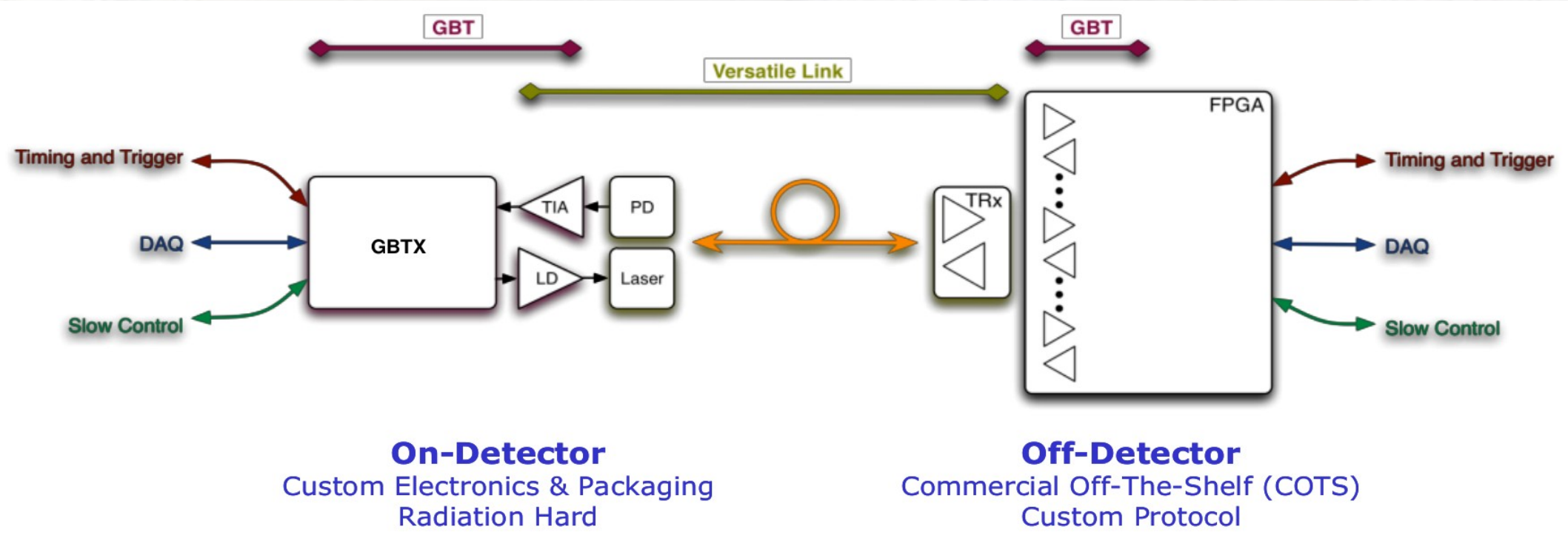
GBTx emulation for BM@N/MPD data acquisition systems

Presenter:
Wojciech M. Zabołotny
Institute of Electronic Systems
Warsaw University of Technology

The material presented is the result of the work of the teams from WUT (W.M. Zabołotny, A.P. Byszuk, M. Gumiński, G. Kasprowicz, K. Poźniak, R.Romaniuk) and GSI/FAIR (D. Emschermann, C.J. Schmidt)

What is GBTX?

- GBTX is a radiation tolerant ASIC, able to provide multiple high-speed links for high-energy physics experiments



GBTX in DAQ

- For DAQ applications the GBTX provides so called E-Links
  - The user data frame with length of 80 bits (with FEC) or 112 bits (without FEC) is delivered every 25 ns
  - This data may be used to implement so-called E-Links – SPI-like synchronous links, working at clock frequency between 40 and 320 MHz and with data rate between 80 and 320 Mb/s (DDR operation is possible)
- Additional slow control is possible via a dedicated SCA chip connected to simple synchronous serial interface

GBTX with SMX2 in DAQ

- In CBM experiment, in STS and MUCH detectors the GBTX works with STS-MUCH-XYTER2 (SMX2) ASICs (developed at AGH) to as front-end electronics.
- A dedicated protocol has been designed (AGH, WUT, GSI/FAIR) for:
  - Control of FEE (including link synchronization and transmission of synchronous commands)
  - Transmission of acquired hit data
- The protocol may be also adapted/reused by other systems in other FEE ASICs (e.g. SPADIC for TRD detector in CBM)

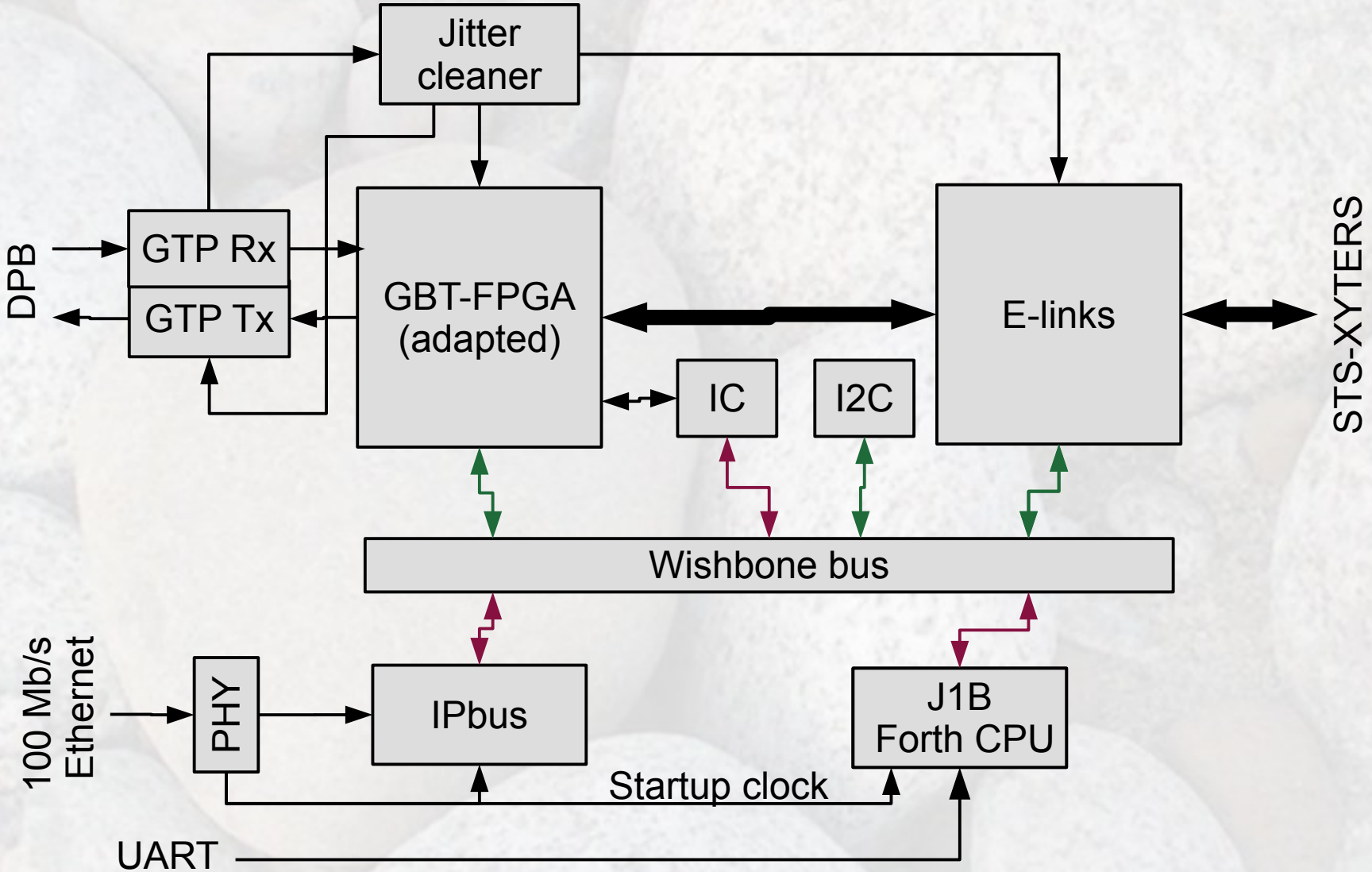
Problems with GBTX

- The original GBTX ASIC is manufactured in a special radiation-hard technology, therefore it is subject to export restrictions
  - The original chip can’t be used in many countries outside EU, including China, India and Russia
  - That affects collaboration at development of detectors and DAQ chains for CBM
  - That also impairs the synergy between CBM and NICA related to usage of SMX2 front-end ASICs

Possible solution - GBTxEMU

- A viable solution is to recreate the most important functionalities of the GBTX in the FPGA
  - The initial plans assumed no standard FEC in downlink direction
- The most important functionality is a possibility to transfer the data via E-Link to and from the FEE.
  - The initial plans assumed no phase adjustment in E-Links
- Additional slow control functionalities may be implemented using free pins of FPGA

Block diagram of the GBTxEMU



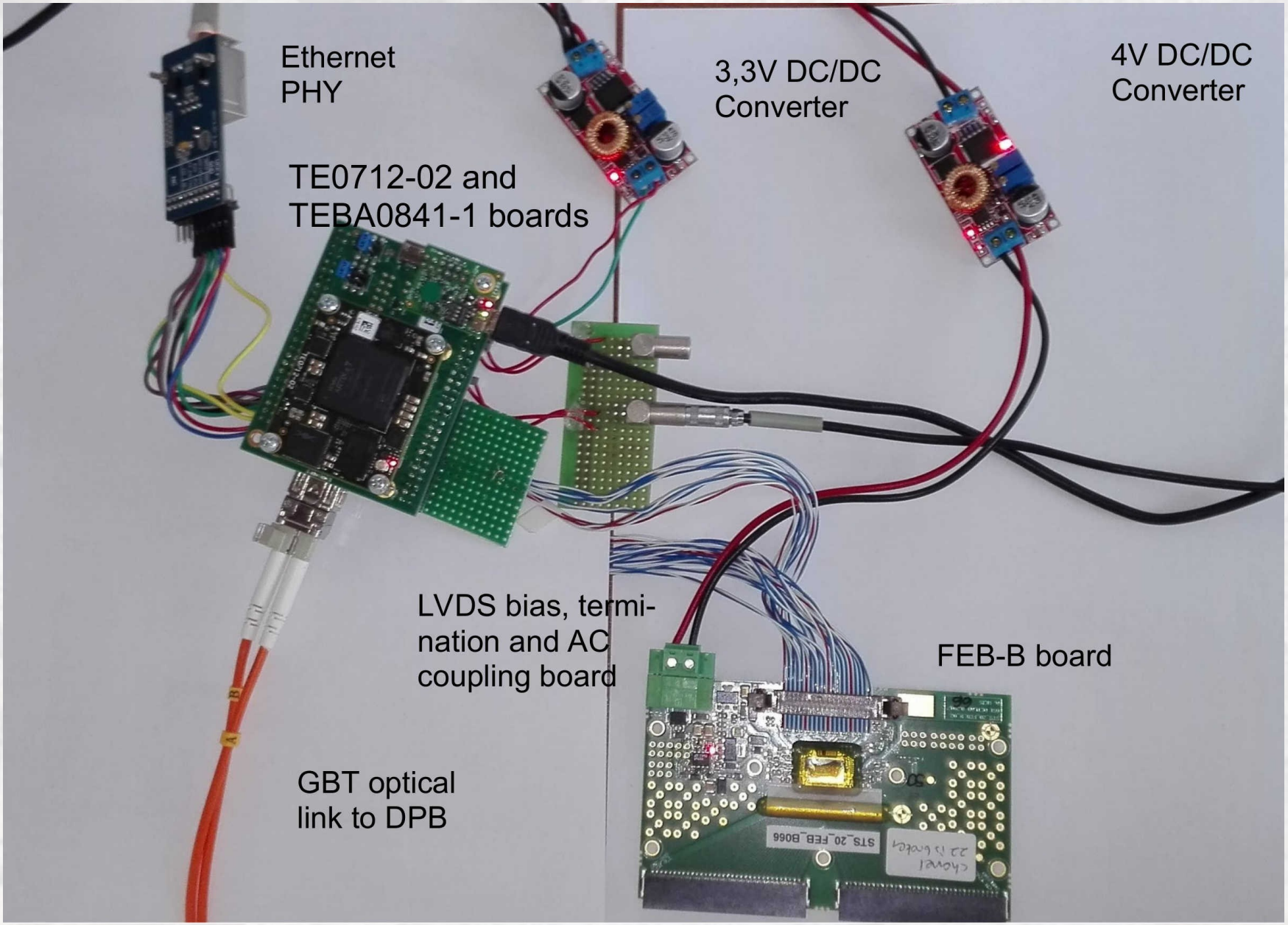
GBTxEMU – basic components

- GBT-FPGA – slightly adapted from the original core provided by the CERN team
- IC core – slightly adapted from original core provided by the CERN team
- J1B – Forth Soft CPU, developed by James Bowman, reused after some modifications
- Wishbone used as an internal bus with possibility to work with multiple masters (IPbus, J1B, IC)
- IPbus – adapted for operation with 100Mb/s link
- E-Links – dedicated core developed for GBTxEMU

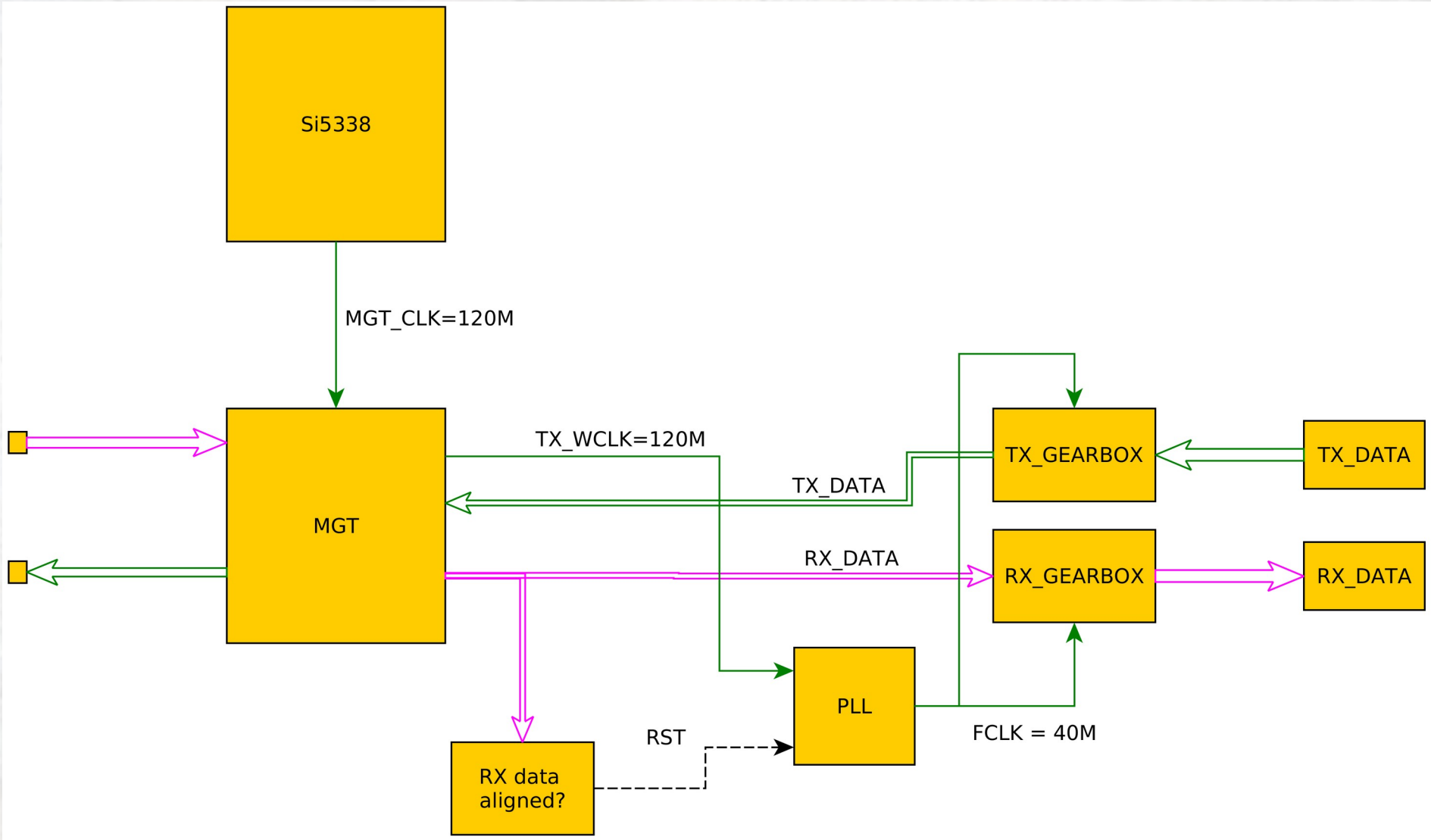
Selection of the hardware platform

- The heart of the GBTxEMU is an Artix 7-based board TE0712-2-200 from Trenz Electronic GmbH
  - Xilinx Artix-7 XC7A200T-1FBG484I FPGA
  - 4 GTP transceivers up to 6.4Gb/s
  - 100 Mb/s Ethernet
  - Programmable Low Jitter PLL (Silicon Labs Si5338)
  - 158 I/Os (78 differential pairs) available for user
- For initial experiments, the TEBA0841 board has been used

Test setup for first prototype



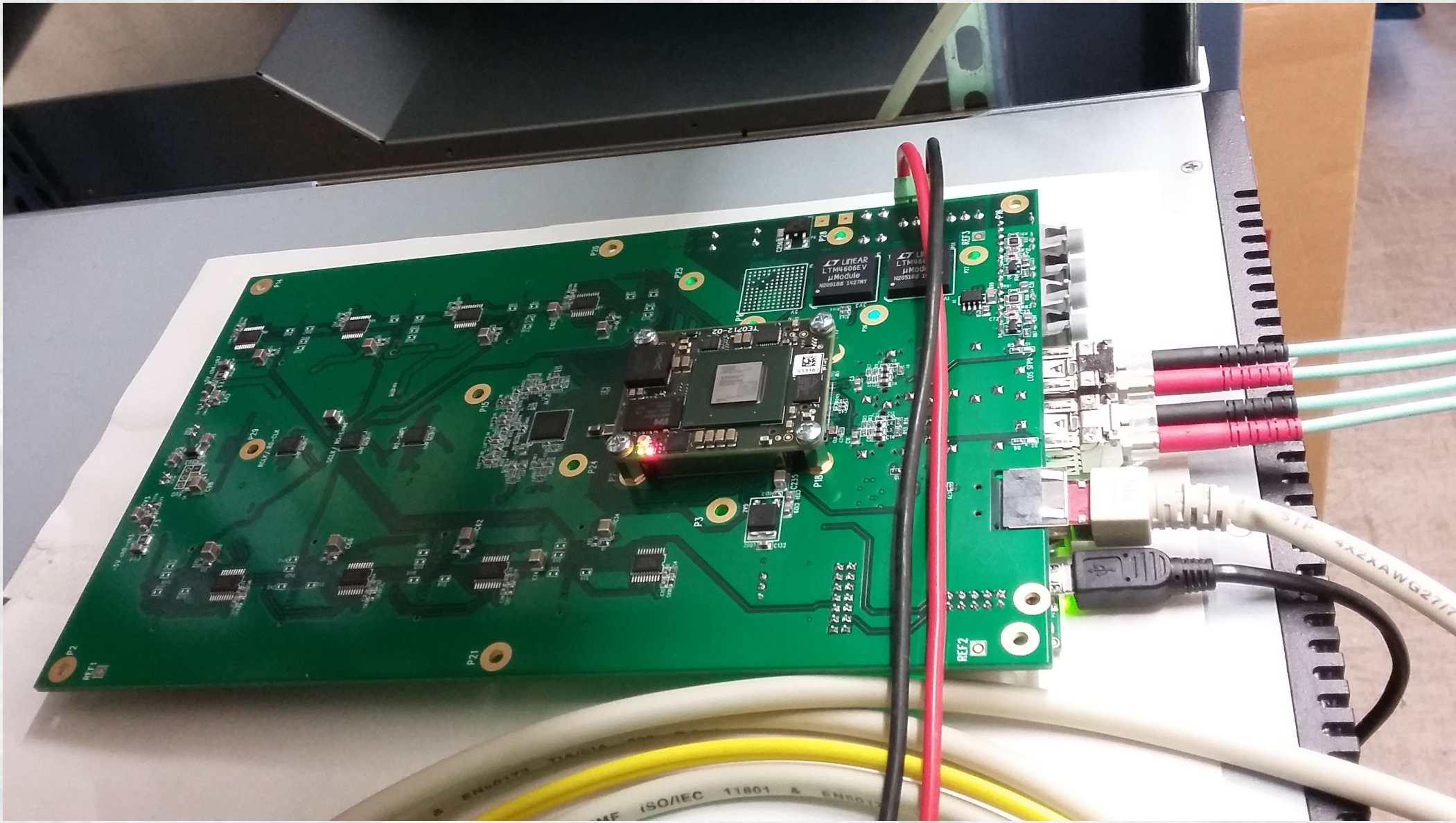
Clock structure with software JC



Dedicated GBTxEMU baseboard

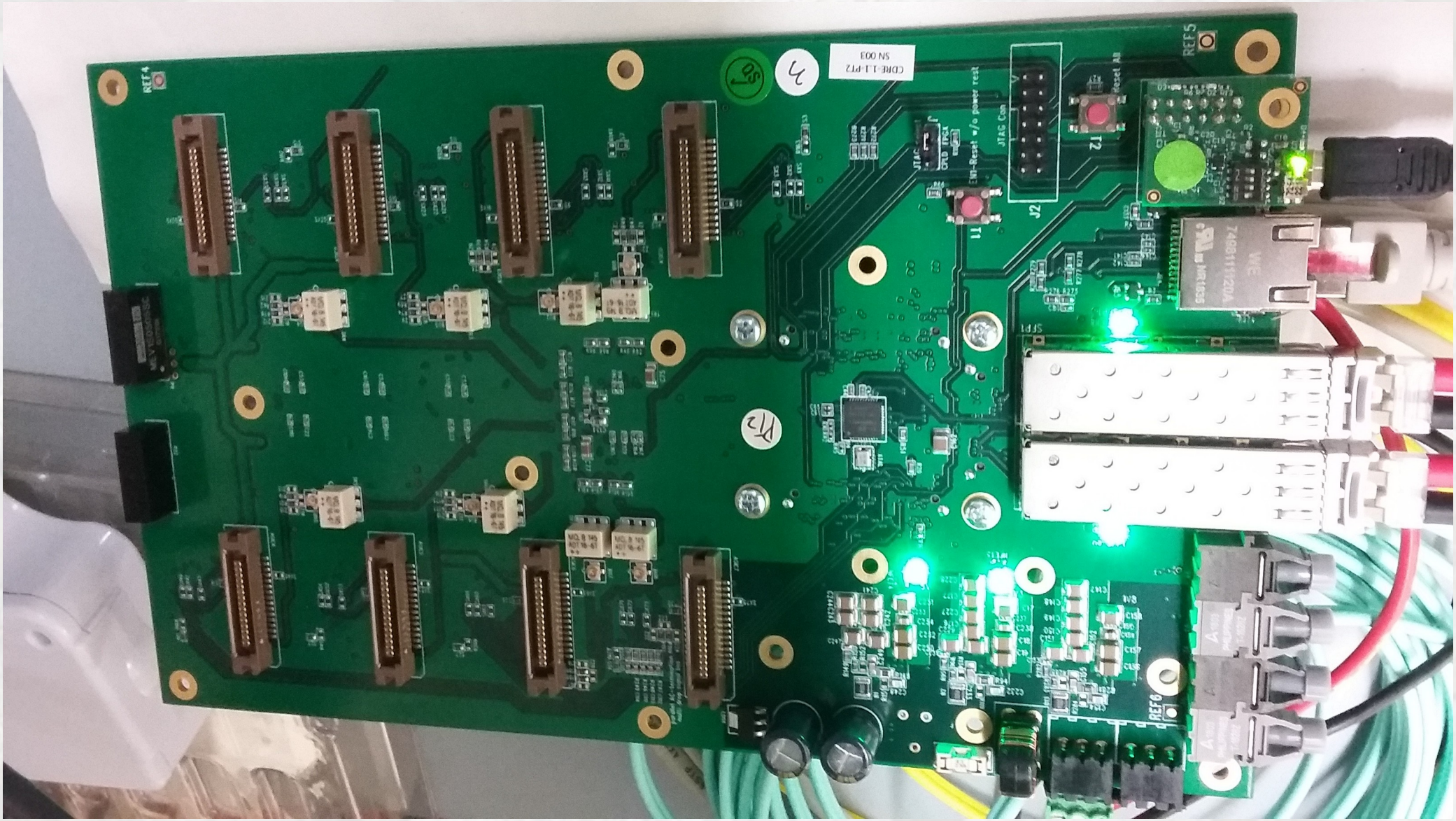
- The dedicated baseboard for TE0712-2 has been developed at GSI
  - It offers hardware jitter cleaner based on Si5344 chip
  - It is equipped with two SFP+ cages
  - It provides 8 ZIF connectors for FEE connections

GBTxEMU board – component side



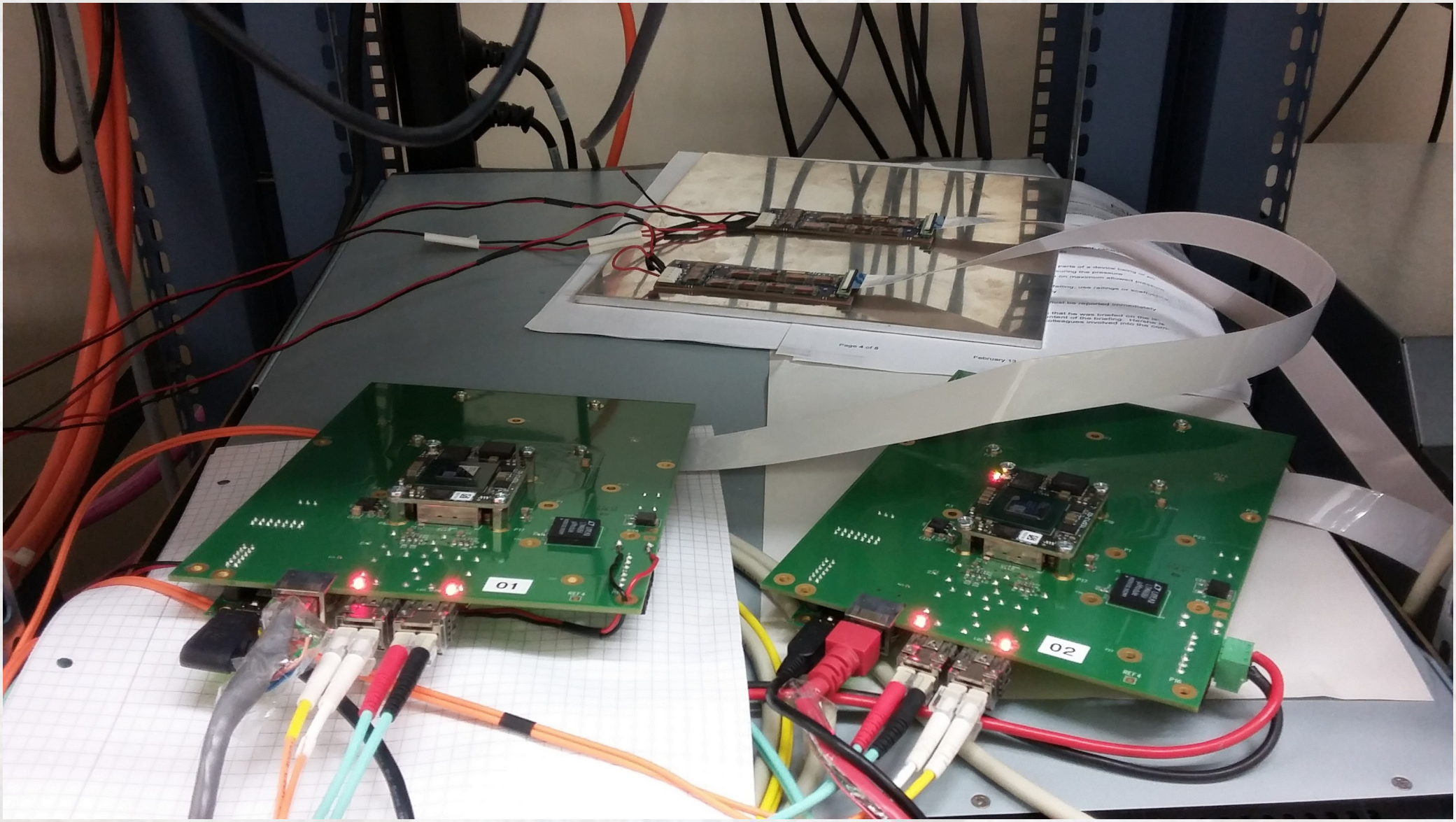
Board developed at GSI

GBTxEMU board – connectors side



Board developed at GSI

2 GBTxEMU with 2 FEB-8

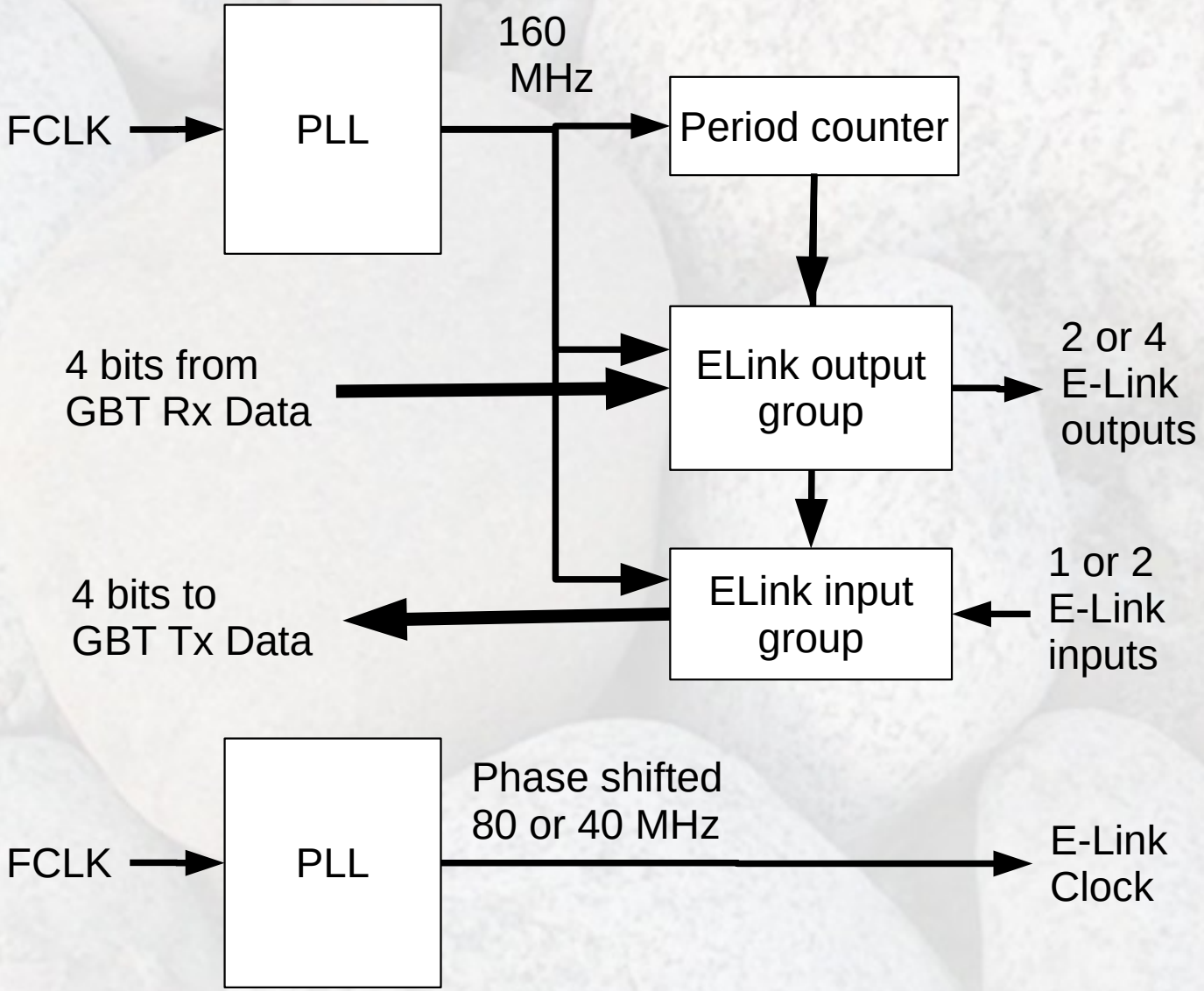


Test stand in GSI

The dedicated E-Link IP core

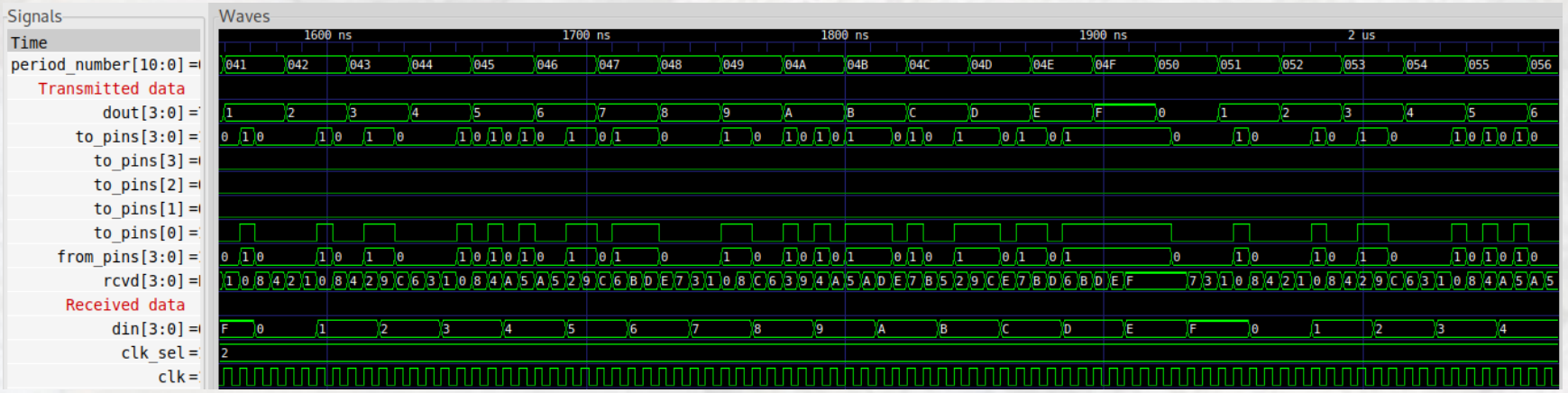
- GBTxEMU supports communication at two possible E-Link clock frequencies – 40 MHz or 80 MHz.
  - @ 40 MHz, the downlink bitrate is 40Mb/s, and uplink bitrate is 80 Mb/s (with 56 possible input channels)
  - @ 80 MHz, the downlink bitrate is 80Mb/s, and uplink bitrate is 160 Mb/s (with 28 possible input channels)
- Limited control of E-Link clock phase and delay of input data is possible

Block diagram of E-Link implementation

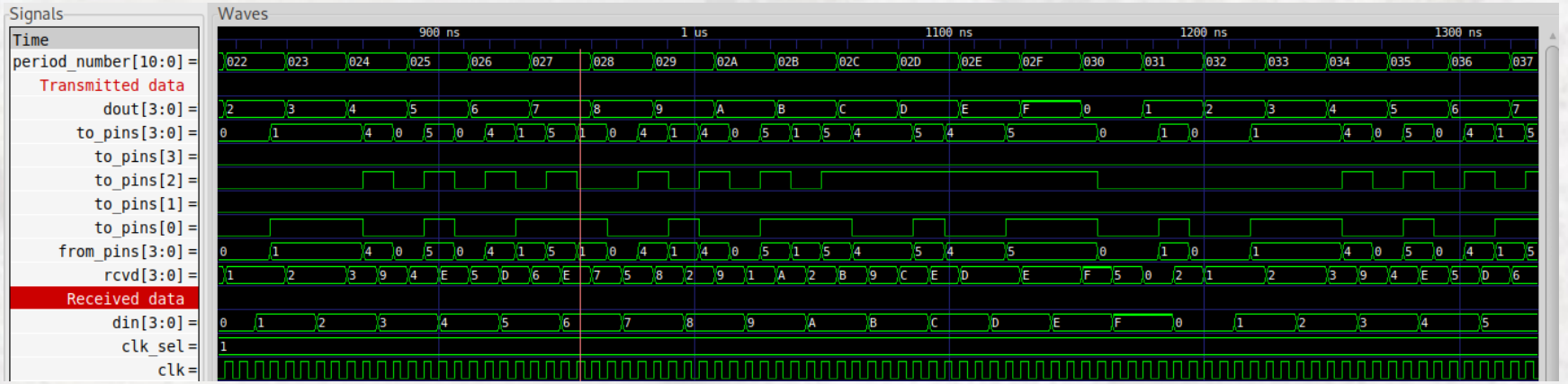


Operation of E-Links at different speed

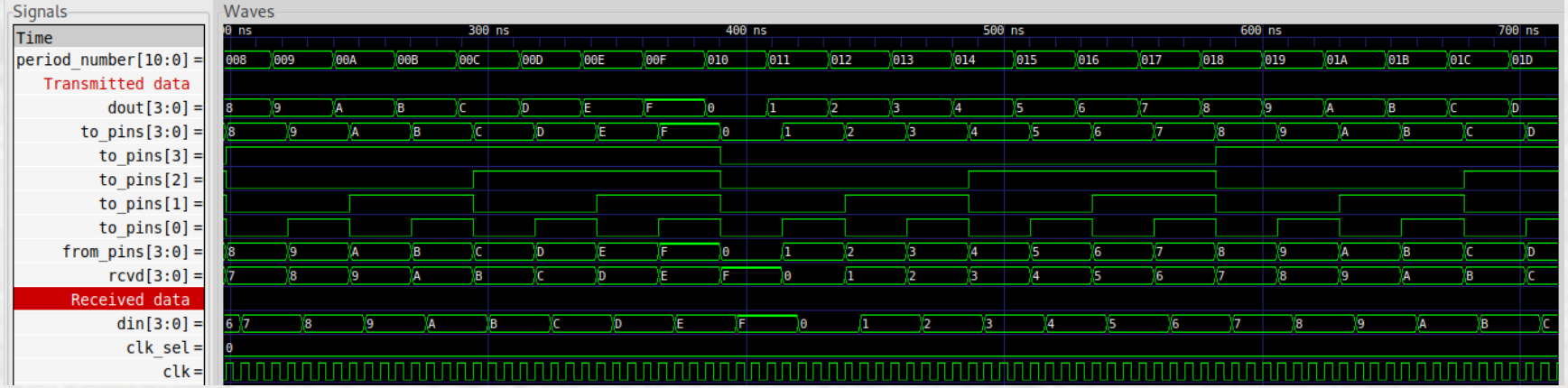
160 Mb/s



80 Mb/s



40 Mb/s

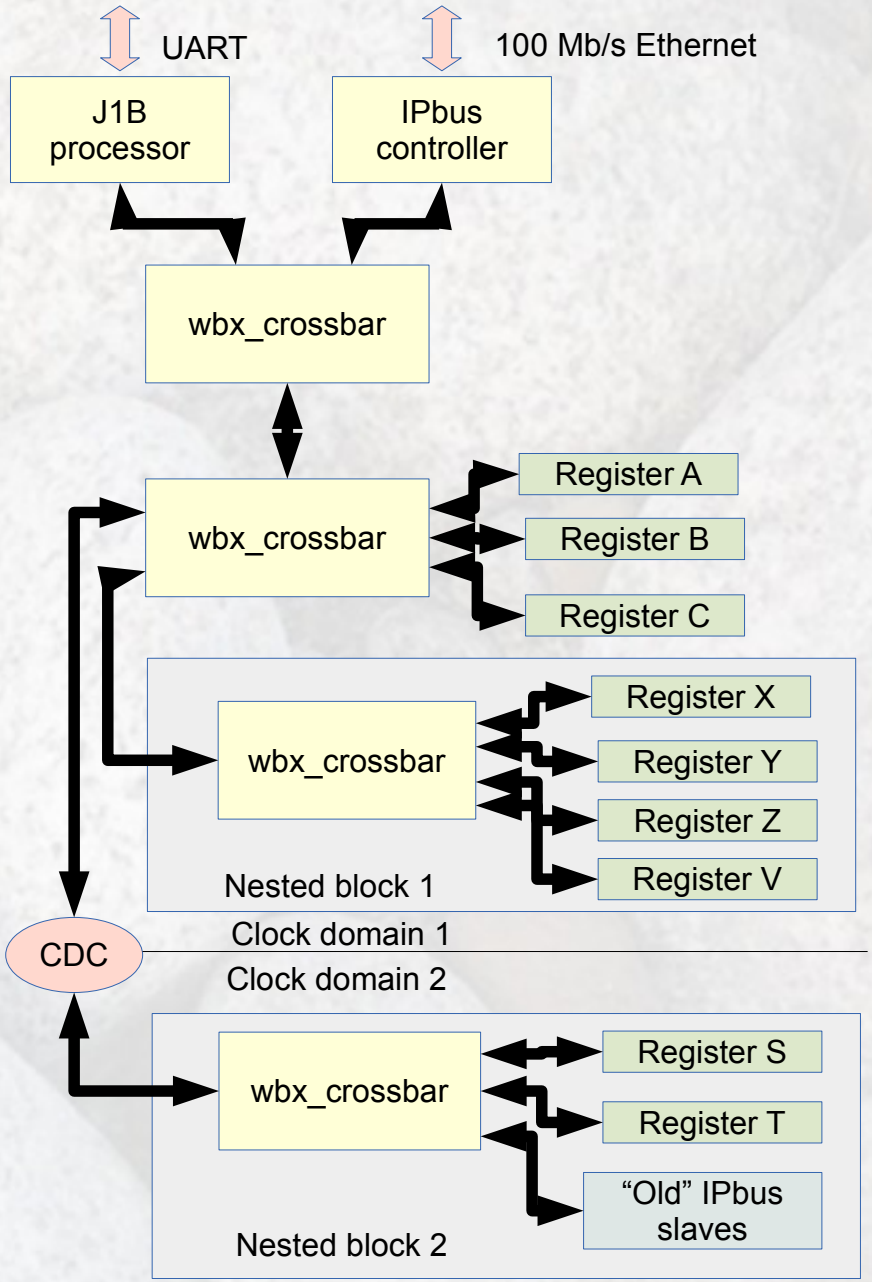


Control of GBTxEMU

- The GBTxEMU may be controlled via various channels
  - IPbus, if 100Mb/s Ethernet connection is available
  - Optical GBT link, after the link is configured (requires automatic configuration by J1B CPU)
  - UART connected directly to J1B CPU (for debugging and testing mainly)

Flexible design

- GBTxEMU uses the internal Wishbone bus with address space managed by the AGWB system.
- It enables easy adding of new internal blocks, and parameterization of the internal structure.
- Application of J1B enables interactive debugging and development of initialization procedure (thanks to use of Forth language).



Results

- Correct operation of GBTxEMU connected to AFCK boards with specially modifed DPB firmware has been achieved.
  - Forward Error Correction in downlink direction is available.
  - The deterministic latency in downlink direction is achievable, allowing transmission of trigger and synchronous commands.
- The GBTxEMU automatically initializes the GBT link and accepts control commands via IC interface.
- Synchronization of E-Links for communication with STS-XYTER (SMX2.1) ASICs is possible both at 40 MHz and at 80 MHz E-Link clock frequency.
- Transmission of commands and reception of hit data from SMX2.1 ASICs is possible.

Conclusions

- GBTxEMU may be used instead of GBT-based CROB boards in DAQ chains, delivering the clock and bidirectional data transmission.
- The maximum confirmed uplink rate is 160Mb/s (twice less than in original GBTX).
- Assessment of long-term reliability is needed.
- Further investigations on more flexible adjustment of E-Link clock and input data delay are possible.
- For full utilization of available ZIF connectors at 160Mb/s, a possibility of providing the second uplink via the second SFP+ cage should be investigated.
- Further work an a light version of DPB for GBTxEMU (GERI board) is needed


Thank you for your attention!