ATLAS17LS – a large-format prototype silicon strip sensor for long-strip barrel section of ATLAS ITk strip detector

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Abstract -- A new inner tracker (ITk) is to be installed inside the solenoid magnet of the upgraded ATLAS detector for the high-luminosity large hadron collider (HL-LHC) at CERN. Silicon strip detectors cover outer layers of ITk with ~165 m^2 of silicon sensors. The barrel section is composed of "short strips (SS)" (2.41 cm long) and "long strips (LS)" (4.83 cm long) sections in the inner and outer layers, respectively, split at a radius of ~75 cm to cope with the density of tracks.

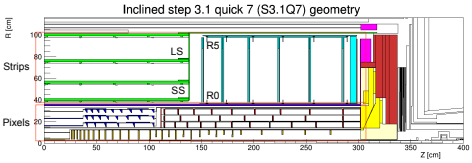
A prototype silicon strip sensor for the "long strips" in the barrel section, ATLAS17LS, was laid out having the largest sensor in the 6-in. silicon wafer, with an outer dimension of 9.80 (width) × 9.76 (length) cm^2, two rows of strip segments, strip pitch of 75.5 µm, and an edge space of 450/550 µm in the longitudinal/lateral direction to the strips (slim edge), as well as miniature sensors and test structures in the wafer periphery for validating and monitoring the sensors. The sensor is a single-sided n-in-p AC strip sensor, made of n$^+$ implant strips for signal collection in p-type wafer material, AC-coupled to readout electronics, and implementing knowledge for high voltage operation up to 1000 V, to have good signal-to-noise ratio until the end of life of the HL-LHC operation.

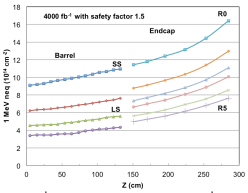
The ATLAS17LS sensors had two purposes: (1) qualification of the sensor itself, technology and capability of fabricating vendors, and (2) serving for prototyping the building block of the strip detector, the strip modules. Hamamatsu Photonics (HPK) was one of two vendors participating in the evaluation along with Infineon Technologies (IFX). The sensors at HPK were fabricated in 3 batches: 1st with the silicon wafer (320 µm physical thickness) and the active thickness of standard or as thin as 240 µm, 2nd with a small number of supplementary sensors with special passivation to investigate the influence of passivation on humidity sensitivity, and 3rd with a dicing scheme of structures in the wafer periphery in the series-production style.

Introduction

Silicon strip detectors is laid out to cover outer layers of ITk , with 4 layers of double-layer single-sided detectors, rotated each other to form a stereo view, in the barrel and 6 layers of disks in the endcap region to ensure approximately 8 hits detection, totaling ~165 m^2 of silicon sensors[1].

A limit of 1% channel occupancy is designed to ensure efficient and stable pattern recognition. With a strip length of 2.4 cm in SS and 4.8 cm in LS, and a strip pitch of 75 µm, occupancies (occ) are 0.92% and 0.57%, respectively, at a pile-up of 200 events of minimum-bias events. The particle fluences to cope with are 1.1×10^{15}, 5.6×10^{14} 1MeV neq/cm^2, respectively, for a life time of 10 yrs to accumulate 4000 fb^{-1} with a safety factor 1.5 [2].

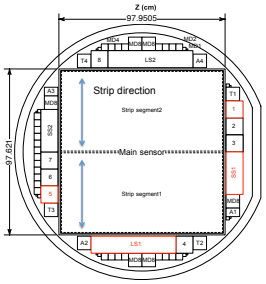




Mask Layout

A prototype silicon strip sensor, ATLAS17LS, was laid out for the "long strips" in the barrel section, having the largest sensor in the 6-in. silicon wafer.

Conceptual layout of ATLAS17LS wafer:
- A large-format main sensor in the middle,
- Minis of 1 to 8 approximately 1×1 cm^2,
- Short strips (SS) of SS1 and SS2 of approximately 2.6×1 cm^2,
- Long strips (LS) of LS1 and LS2 of approximately 5×1 cm^2,
- T1 to T4 are the test structures of vendors,
- A1 to A4 are the test structures of ATLAS.
- The diodes (8×8, 4×4, 2×2, and 1×1 mm^2) are placed wherever space is available.
- Outer dimension of 9.80 (width) × 9.76 (length) cm^2,
- two rows of strip segments,
- strip pitch of 75.5 µm,
- an edge space of 450/550 µm in the longitudinal/lateral direction to the strips (slim edge),
- miniature sensors and test structures in the wafer periphery for validating and monitoring the sensors.



Mask Requirements

The sensor is
- a single-sided n-in-p AC strip sensor,
- n$^+$ implant strips in p-type wafer material,
- implementing knowledge for high voltage operation up to 1000 V, to have good signal-to-noise ratio until the end of life of the HL-LHC operation.

Mask Parameters	Values
Number of strip segments	2
Number of implanted strips per segment	1282
Number read out strips per segment	1280
Pitch of the strips	75.5 µm
Implant strip width	16 µm
Read-out metal strip width	22 µm
Polysilicon bias resistors	overlapping over strip implant
Isolation of n-strips	common narrow width p-stop, 6 µm
AC-coupling protection against beam splash	PTP gap ≤20 µm, with field plate

Mechanical/Electrical Properties

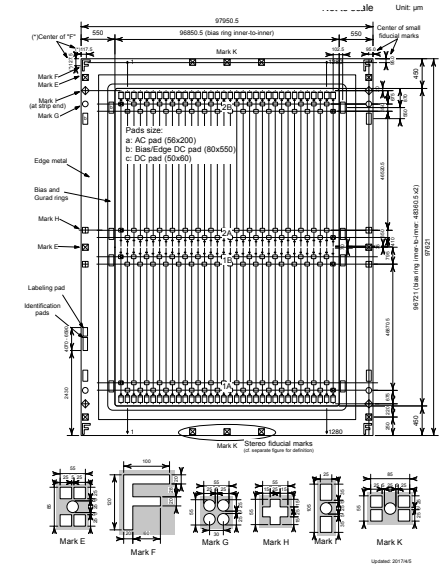
Drawings in below show
- details of mechanical layout and
- fiducial mark definition.
- Major parameters are listed in the table.

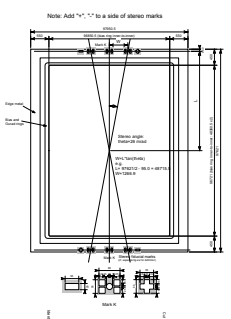
Maximum operating voltage and the onset voltage of microdischarge (*) are
- 700 V for the most of the fabrication,
- reduced to 500 V for later fabrications as the requirement for the amount signal charge is reduced due to a better performance of new readout ASIC.

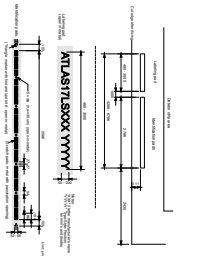
Bad strips
- AC coupling punch-thru, metal/implant open/short to neighbor, Polysilicon bias resistor break/out of range, ...

Fiducial markers, Identification
- Fiducial markers (E, F, G, H, I, K) in the lateral edges to strips,
- Stereo fiducial markers at the longitudinal edges, for optical alignment.
- Scratch pads for 6 digits, each digit with binary code of 0-9.

Mechanical/Electrical Parameters	Values
Wafer physical thickness	320±15 µm
Active thickness	>270 µm
Wafer type	p-type FZ <100>
Wafer resistivity	>3.5 kΩcm
Full depletion voltage (*Vfd*)	<300 V
Maximum operating voltage (*)	700 V
Polysilicon bias resistor (*Rb*)	1.5±0.5 MΩ
Inter-strip resistance/capacitance (at 300 V)	>10×*Rb*/<1pF/cm
Leakage current (@25°C)	<0.1 µA/cm^2
Onset voltage of Microdischarge (*Vmd*)(*)	>700 V
Bad strips	<1% per segment & <1% per sensor



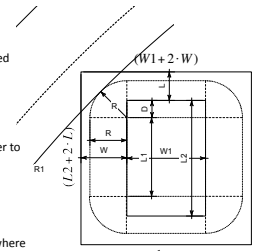




Sizing the dimensions

Maximum active area, narrow width of sensor edge (**Slim design**)
- The minimum distance from the inner edge of the bias ring to the dicing edge is verified being ~450 µm for 1kV operation [3],
- enabling maximum usage of silicon in a wafer,
- minimum dead space between the modules which are arranged "flat" (rather than "shingling") in the macro structure of the layer.

Calculations
- *R1*: maximum radius of implant with high electric field, given by vendor
- *L*, *W*: edge space (longitudinal(strip dir.), Lateral) distance, 450/550 µm; Lateral is wider to allow placing wire-bonding pads on the bias ring
- *W1*: active strip area, = strip pitch×No. strips
- Width(W1+2*W)×Height(L2+2*L) to be (near) square.



$$R1 = R + \frac{1}{2}\sqrt{W1^2 + L1^2}$$

$$L2 = L1 + 2 \cdot D$$

Special Features

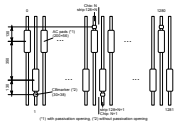
Design for high voltage operation
- We have analysed and practiced the rules that have enabled high voltage operation, where critical issue is reducing the local electric field strength [4]. The practices are
- n$^+$-strip: with wide AC metal,
- p-stop: narrow, common, symmetric in distance from neighbour n-implants including bias ring.

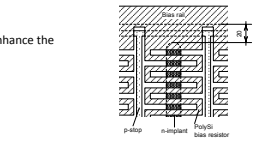
Surface passivation
- Tuned to try minimizing pin-holes and cracks in the passivation

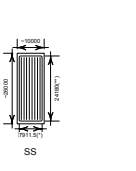
Punch-through protection structure (PTP)
- "Full coverage" with PolySi resistor sheet extending from the bias rail, in order to enhance the breakdown characteristics [5, 3].

Chip boundary (CB) markers of wire-bonding pads
- in the pad rows of 1A, 1B, 2A, and 2B,
- for identification of wire-bonding pads of the 1st and the last channels of an ASIC.

Layouts of the miniature sensors
- Minis (1×1 cm^2),
- Short-strips (SS: 2.6×1 cm^2)
- Long-strips (LS: 5×1 cm^2).
- The strip and edge structures shall follow those defined in the main sensor.





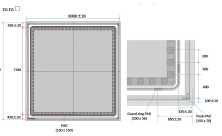


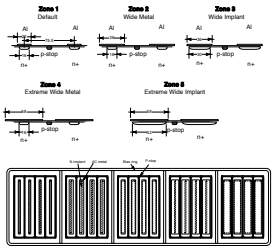
Wafer Test Structures

R&D minis
- 2 Minis (#1 and 5), 1 SS (SS1), and 1 LS (LS1) – Red in wafer layout
- variation of metal/implant width: Zone 1 to 5
- Each zone has 20 strips, encircled with common p-stop

MD8 diode
- with contact pads on the "guard" ring, to separate currents in the pad and from the edge; others (MD4, MD2) are without the pads.

(*) Bias ring inner-to-inner, 104 strips of 75.5 µm pitch
(**) Bias ring inner-to-inner





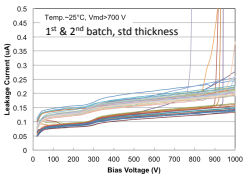
Fabrication and Initial Measurements

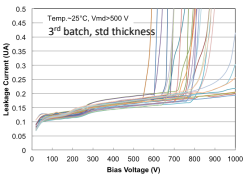
Two purposes:
- (1) Qualification of the sensor, the technology and capability of fabricating vendors. The other vender than HPK is described elsewhere [6].
- (2) Serving for prototyping modules and macro structures

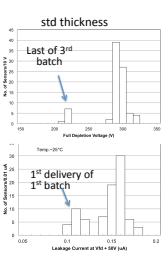
The sensors at HPK were fabricated in 3 batches:
- 1st with the silicon wafer (320 µm physical thickness) and
- the active thickness of standard or thin as 240 µm,
- 2nd, in addition with a small number of special passivation to investigate the influence of passivation on humidity sensitivity [7].
- 3rd for additional sensors, with a dicing scheme of structures in the wafer periphery in the series-production style.

Initial measurement at vendor
- Microdischarge onset voltage (*Vmd*): >700V (1st batch), >500 V(3rd batch)
- Leakage current << 10 µA
  - Low leakage current in the 1st delivery of the 1st batch could be a systematics.
- *Vfd* < 300V was too tight
  - Low *Vfd* of the last batch of the 3rd delivery is due to usage of higher resistivity wafers.
- Bad strips <<1%

Batch	Thickness	Quantity	Wafers#
1st	standard	30	W003-040
	thin	5	W044-049
2nd	standard	25	W053-128
	thin	5	W149-154
	special	5	--
3rd	standard	60	W114-234







Acknowledgements

The research was supported and financed in part by KAKENHI, under Contract No. 16H06491A, by the Ministry of Education, Youth and Sports of the Czech Republic coming from the project LM2015058 - Research infra-structure for experiments at CERN, and by Charles University grant GAUK 942119, by the U.S. Department of Energy, Grant DE-SC0010107, by the U.S. Department of Energy, Office of Science, High Energy Physics, under Contract No. DE-AC02-05CH11231, by Natural Sciences and Engineering Research Council of Canada (NSERC), grant SAPP-J-2018-00, by the Spanish Ministry of Science, Innovation and Universities through the Particle Physics National Program, ref. FPA2015-65652-C4-1-R (MICINN/FEDER, UE), the Spanish Ministry of Economy and Competitiveness through the Particle Physics National Program, ref. FPA2015-65652-C4-4-R (MINECO/FEDER, UE), and co-financed with FEDER funds.

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[6] cf. presentation #270 in this conference
[7] cf. presentation #230 in this conference for the study of humidity sensitivity