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Measured Effectiveness of Deep N-well Substrate Isolation in a 65nm Pixel Readout Chip Prototype

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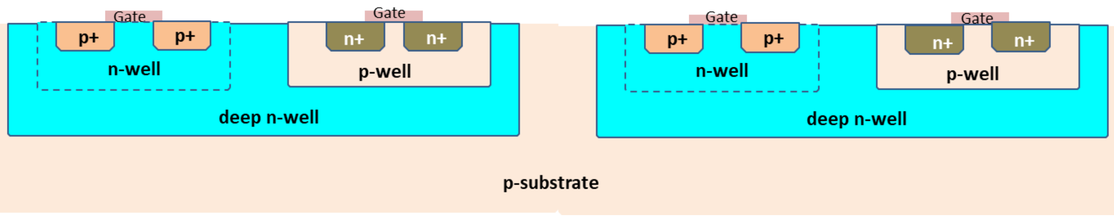
1. Introduction

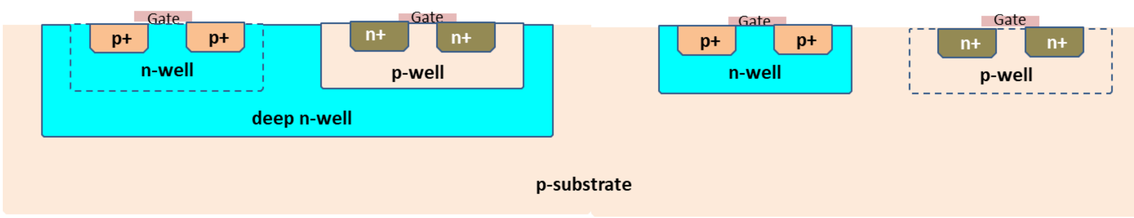
FE65-P2 chip (65nm bulk CMOS process) was fabricated twice with different isolation strategies.

A very rare opportunity to prototype and test the same complex circuit with different isolation strategies.

Double Isolation: both digital and analog are in deep n-wells



Digital Isolation: only digital is in deep n-well; analog is on substrate



2. Single pixel measurements w/o noise injection

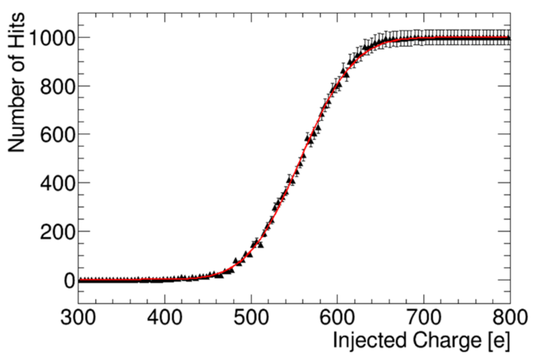
- **If isolation is not enough, noise in digital spreads into analog**
- **Noise observed in analog**

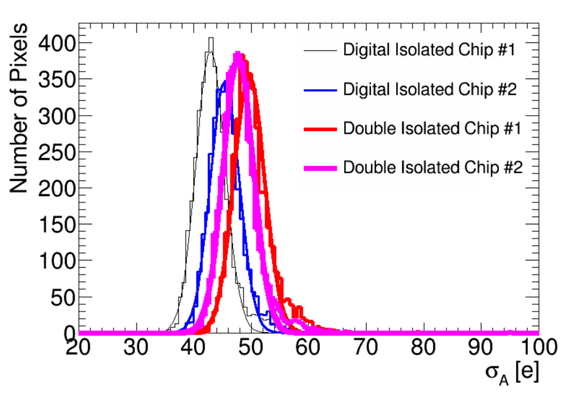
$$\sigma_{A\otimes D} = \sqrt{\sigma_A^2 + \sigma_D^2}$$

σ_A : **Intrinsic analog noise width**

σ_D: **Width of the noise spreads from digital to analog**

- σ_A is obtained with **digital off** by fitting S-curve in each pixel.

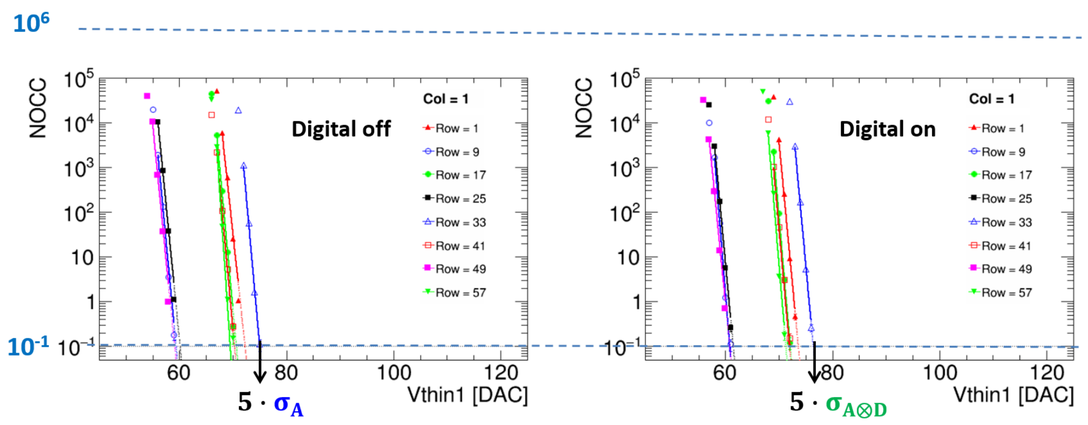




- How to measure $\sigma_{A\otimes D}$? **Measure $5\cdot\sigma_{A\otimes D}$ ➔ to detect smaller σ_D**

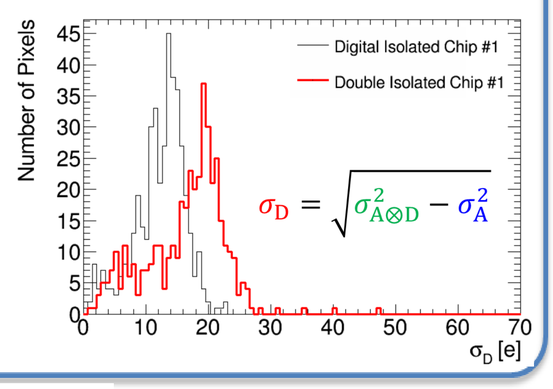
  - Pixel Noise OCCupancy (**NOCC**) : #noise observed in one pixel in 1s interval
  - Assuming that noise is Gaussian and at zero threshold the NOCC is of order 10^6

  "floor" NOCC of 0.1 → critical threshold is ~ 5σ away from zero.



Zero threshold varies among pixels ➔
To measure the change of critical threshold

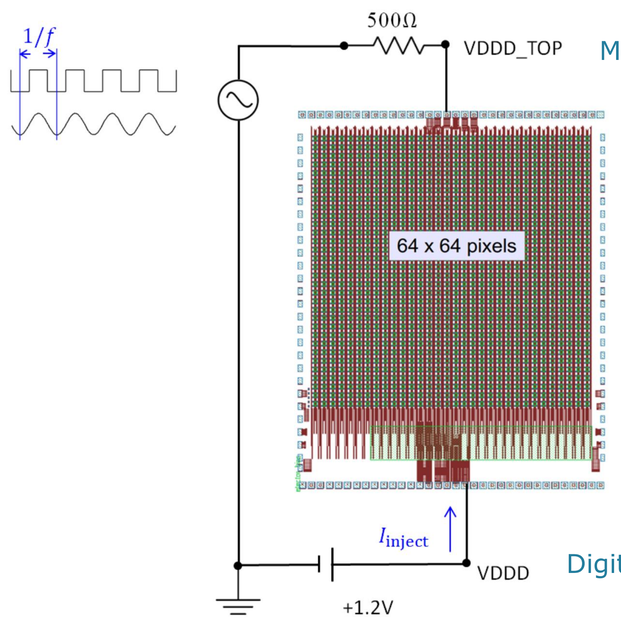
$\delta = 5\cdot\sigma_{A\otimes D} - 5\cdot\sigma_A$



- **Did see noises spreading into analog from digital**

3. Pixel matrix measurements w/ noise injection

- **To induce noise in digital by varying current in the pixel columns**

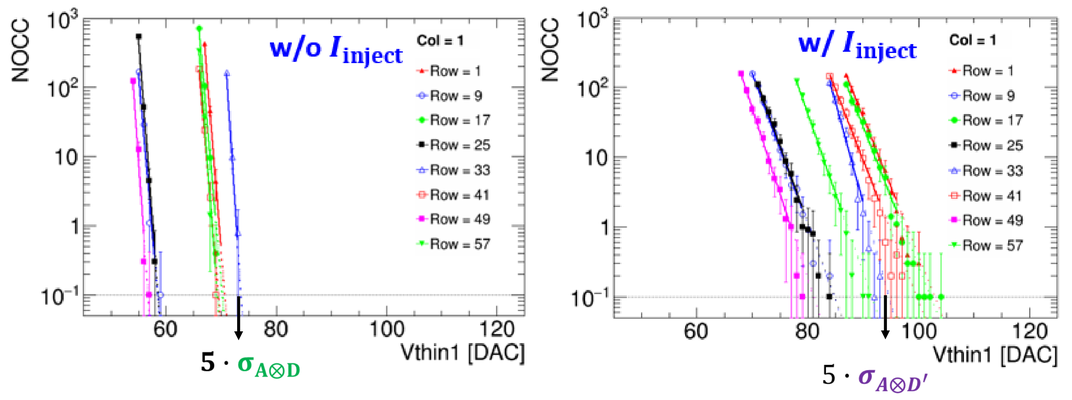


The highest voltage of the A/C signal is always 1.2V, while the lowest voltage changes to produce different I_{inject}

The analog power supply is kept at 1.2V.

Analog and digital grounds are separated on the chip all the way to the bonding pads.

- f = 1MHz square wave with I_{inject} = 4.8mA (Internal current = 23mA)

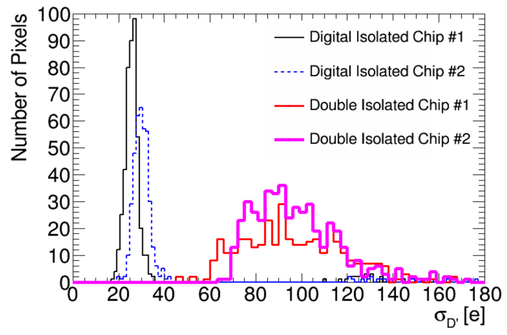


To measure the change of critical threshold

$\delta = 5\cdot\sigma_{A\otimes D'} - 5\cdot\sigma_{A\otimes D}$

$\sigma_{D'} = \sqrt{\sigma^2_{A\otimes D'} - \sigma^2_A}$

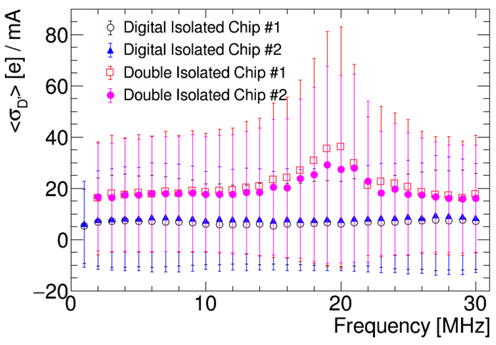
The digital isolation is better.



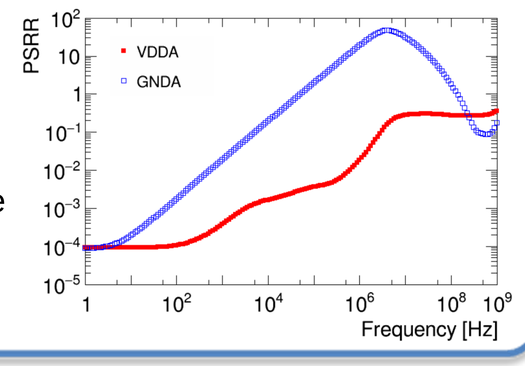
- **Frequency dependence of the noise coupling obtained using sine waveform**

I_{inject} = 1.2mA for double isolated chip

I_{inject} = 2.4mA for digital isolated chip



- **Simulated Power Supply Rejection Ratios** for the power and ground rails of the FE in the double isolated chip
- The digital noise coupling in the double isolated chip is due to noise injection from the digital power network to the FE ground, rather than through the isolated substrate.



4. Summary

The digital isolation is better than the double isolation.

Noise is coupling through the metal stack rather through the substrate.

The double isolation has a higher impedance analog ground that is easier to shake by noise coming from the metal stack.