Belle II Pixel Detector

Commissioning and Performance

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On behalf of Belle II PXD - DEPFET Collaboration

HSTD12, Dec.14-18, 2019, Hiroshima

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

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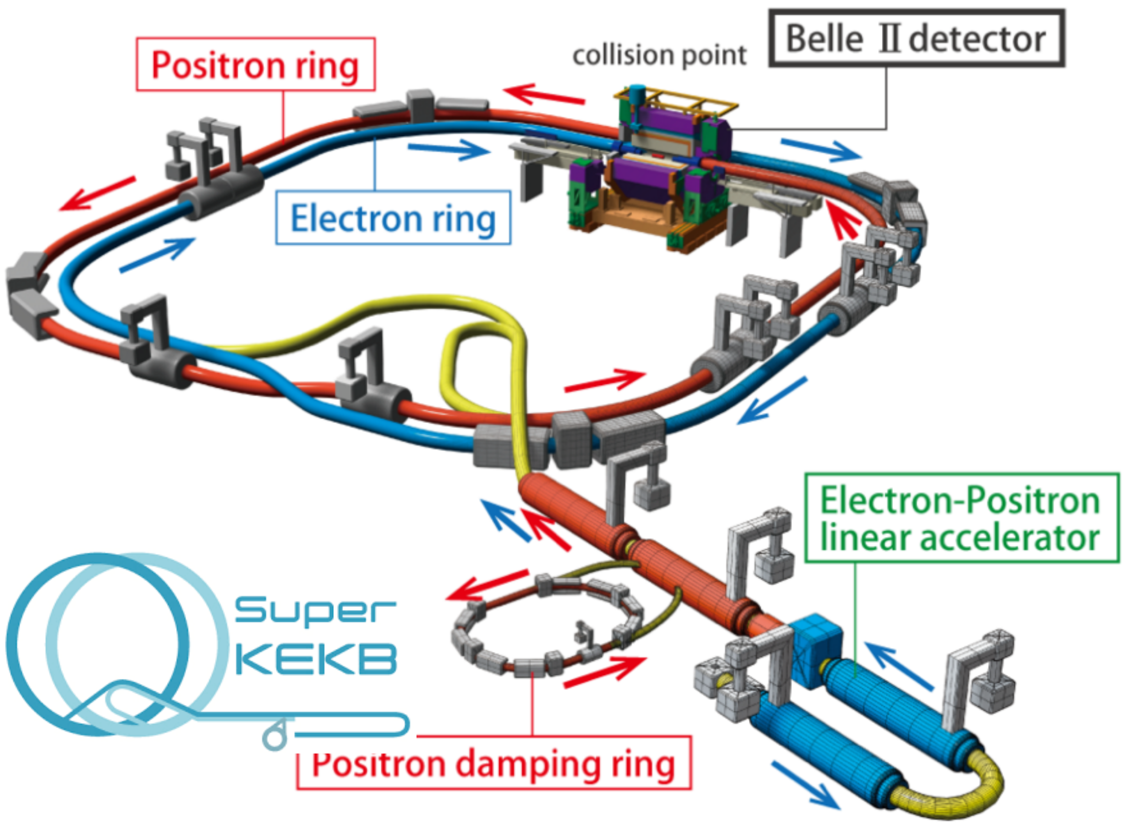
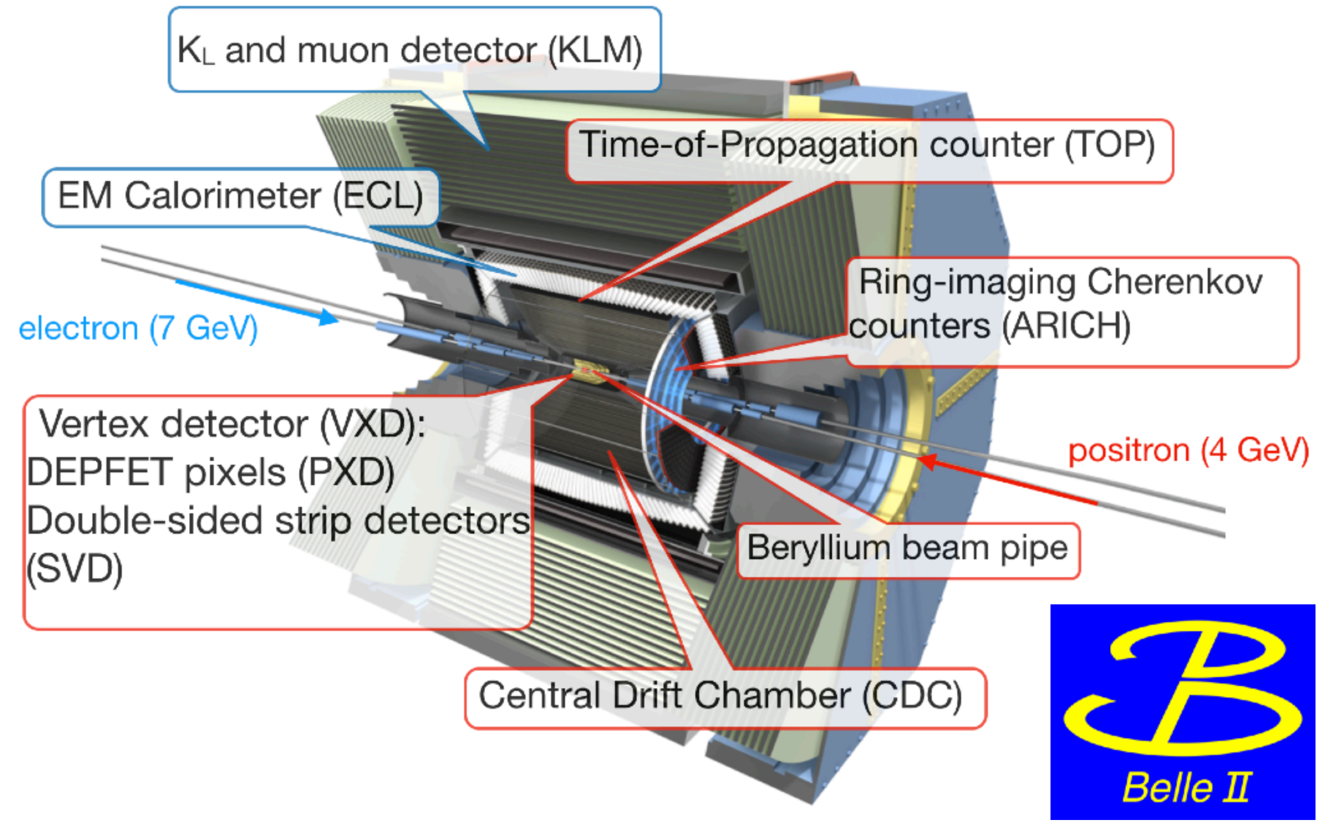
JENNIFER2 EU grant n.822070

Belle II

DESY.

SuperKEKB and Belle II

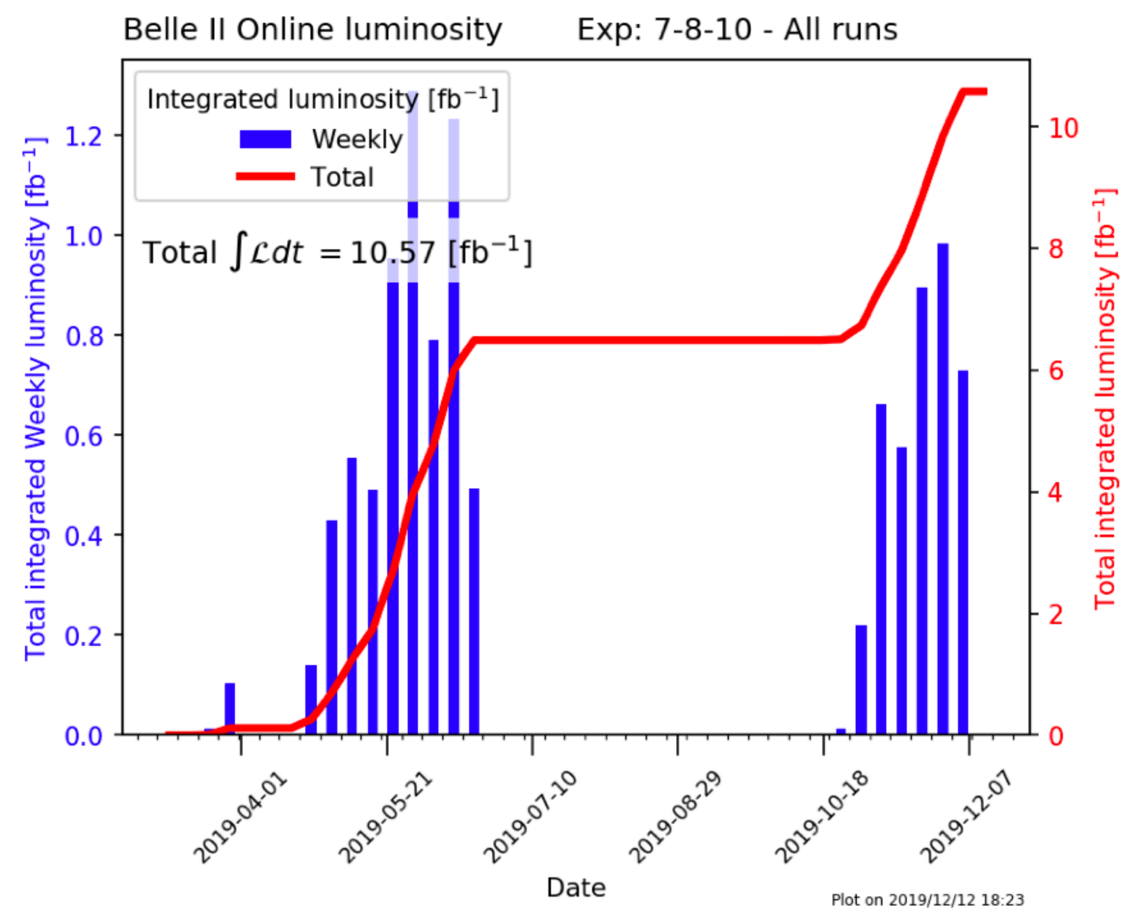


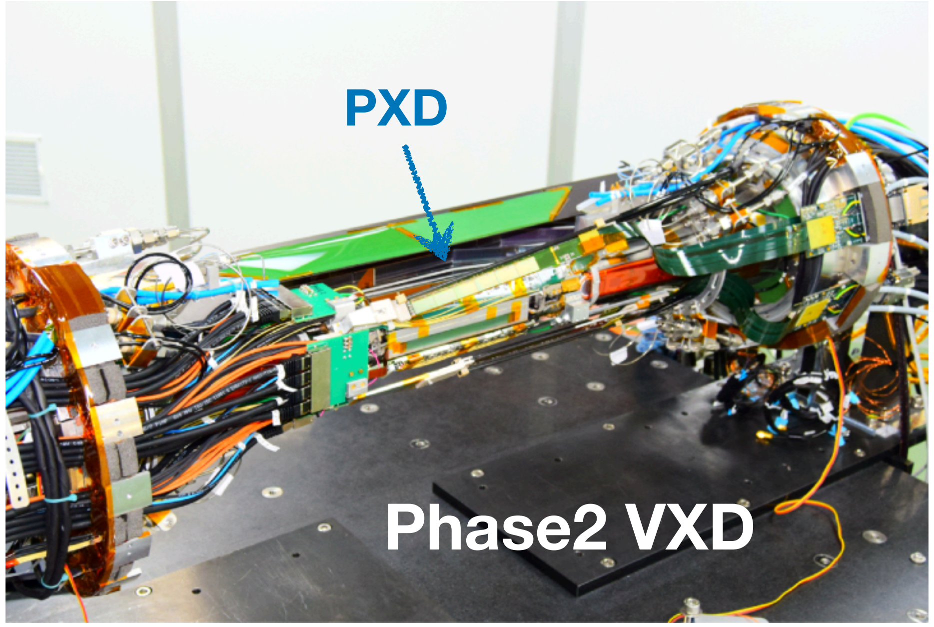


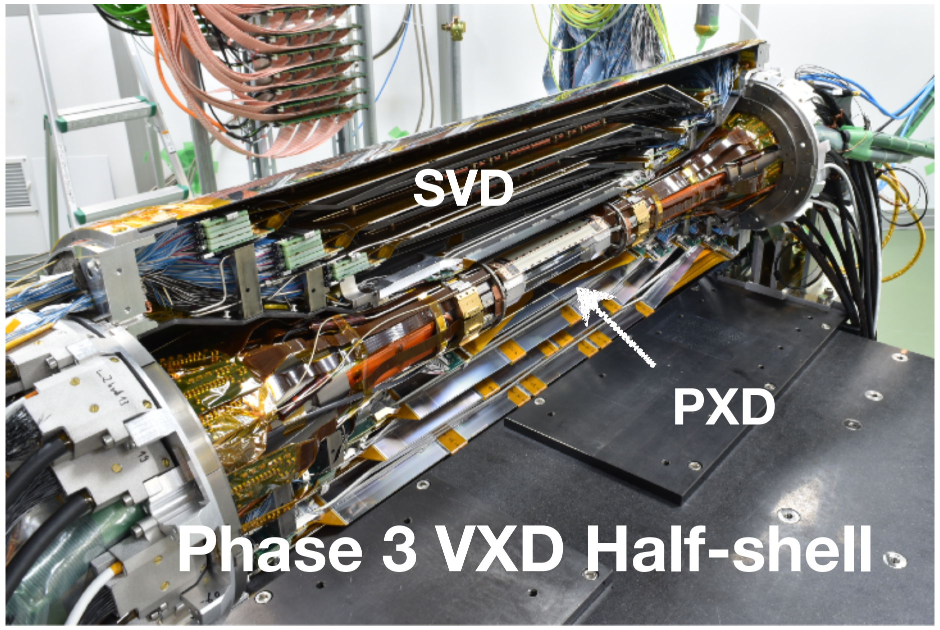
- SuperKEKB delivers e^+e^- collisions at 10.58 GeV ($M_{\Upsilon(4S)}$), with a target peak luminosity of 8×10^{35} $cm^{-2}s^{-1}$, 40 times larger than that of KEKB.
  - Increase beam currents twice
  - Reduce vertical beam spot size by a factor of 20
- Belle II detector has accomplished a series of upgrades to
  - Improve the overall performance
  - Cope with the increased background and high trigger rate.
- Aim to accumulate a dataset of 50 ab^{-1} by ~2027, to study flavour physics and explore new physics beyond the standard model.

Highlights of Belle II Status

- Collisions started in Spring 2018, "Phase 2".
  - Mainly for beam commissioning,
  - with a dedicated vertex detector to study beam background.
  - **0.5 fb^{-1} data recorded.**
- Physics data taking has started in March 2019, "Phase 3".
  - With Belle II VXD
  - **10 fb^{-1} data recorded.**
  - Aim to collect 200 fb^{-1} by summer 2020.
- On Dec.3, Belle II achieved to record data at luminosities in excess of 10^{34} $cm^{-2}s^{-1}$ (KEKB design luminosity)







DEPFET PXD for Belle II

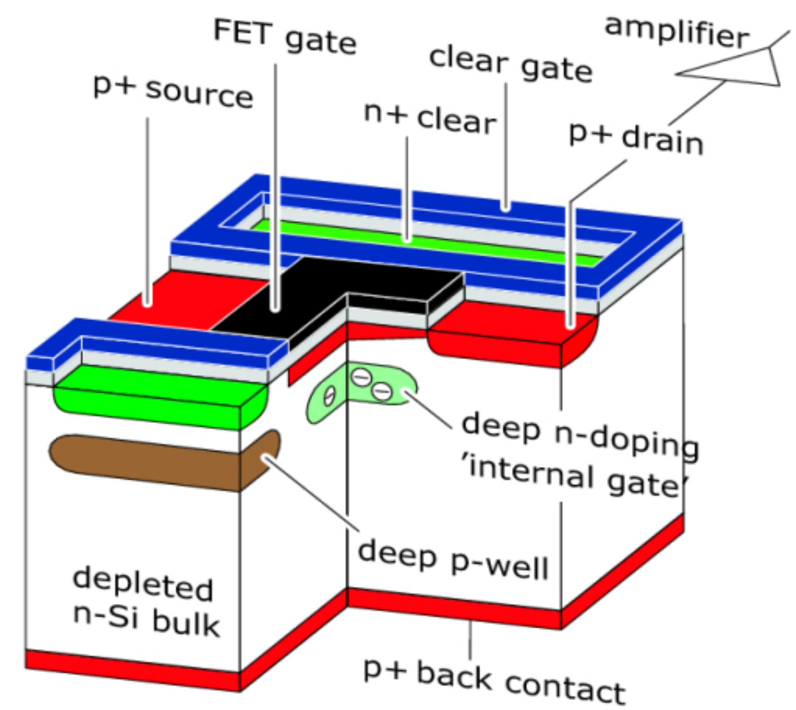
Depleted P-channel Field-Effect Transistor (DEPFET) combines detection and amplification within one device.

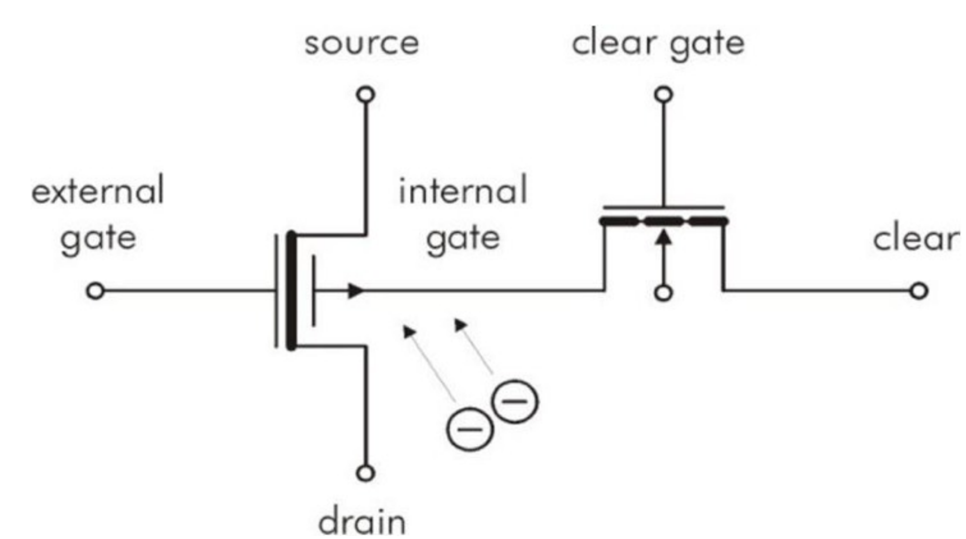
Each pixel is a p-channel FET on top of fully depleted silicon bulk

- Fast charge collection (~ns)
- Charges collected in the “internal gate”
- Readout of modulated drain current
  - ➡ internal amplification

$$g_q = \frac{\partial I}{\partial q} \approx 500 \, \frac{pA}{e^-}$$

- High Signal to Noise Ratio (SNR)
- Periodical clearing of “internal gate” required to reset the pixel

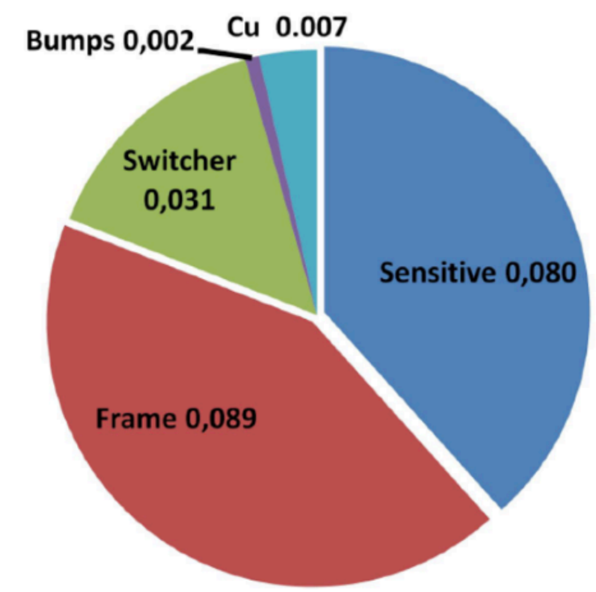


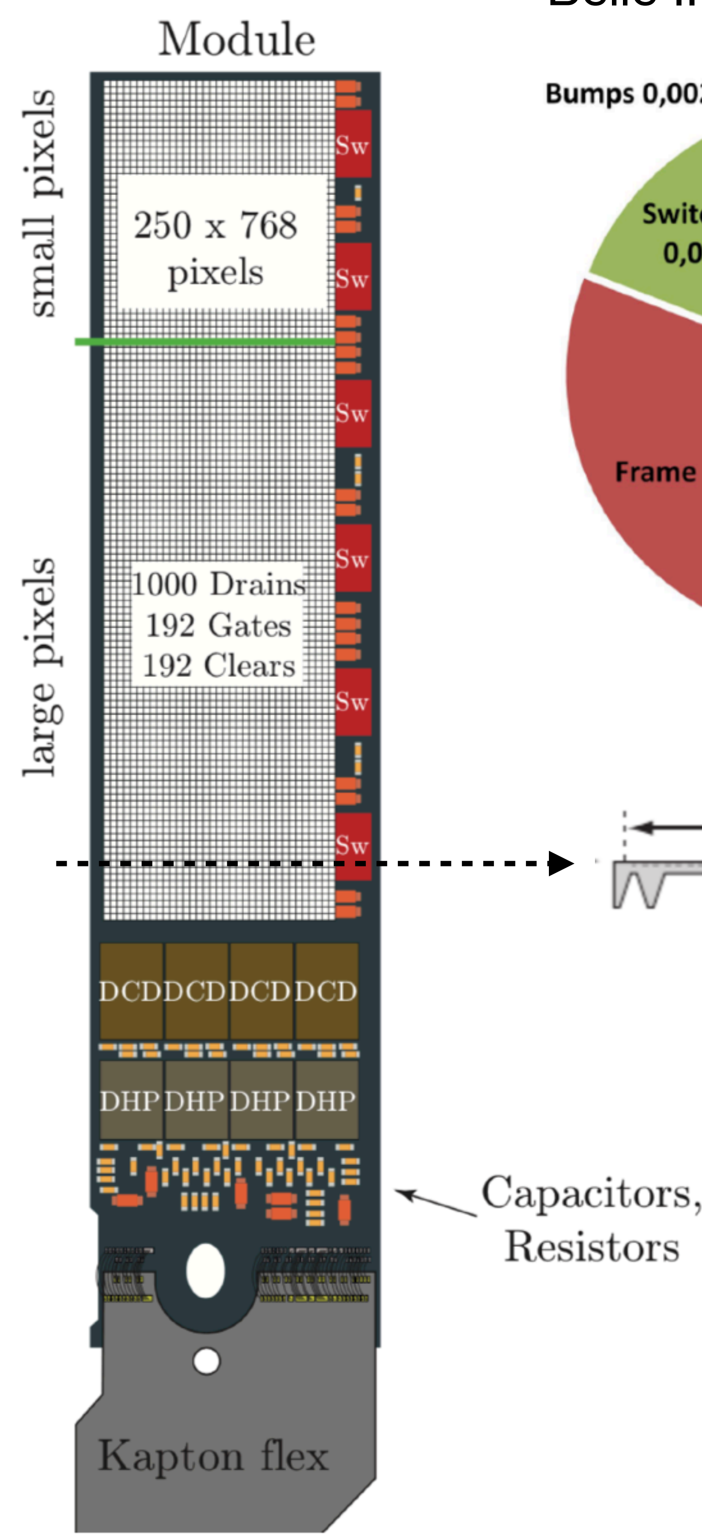


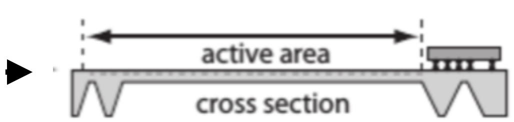
PXD Module Concept

- Pixel size: varies in z direction, 50 x 55-85 μm²
  - optimized to have the best resolution in forward direction around 45° incident angle
- 250 x 768 pixels per module
- By thinning the active sensor thickness can be reduced to as little as 50 μm.
- For optimal position resolution (COG) 75μm were chosen for PXD
- 3 Metal layers for circuitry
  - 2Al + 1Cu
- Mechanically self-supporting device

Belle II module: 0.21% X_0





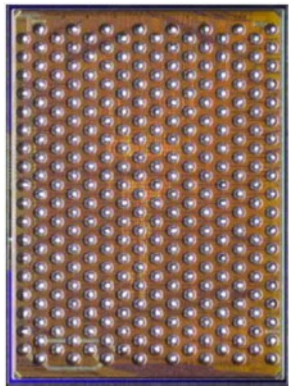


ASICs

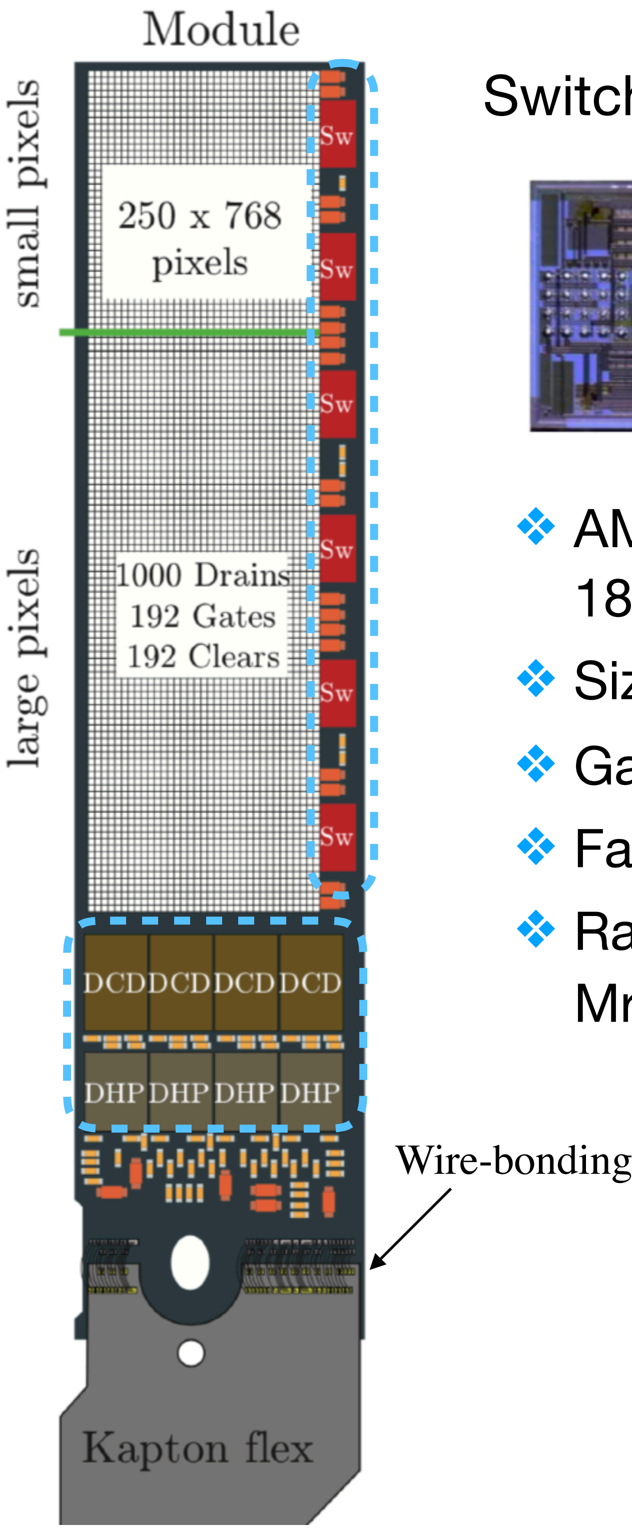
DCD:Drain Current Digitizer,

- UMC 180 nm
- 256 input channels
- pipeline 8-bit ADC per channel
- 92 ns sampling time
- Rad. hard proved (10 Mrad)

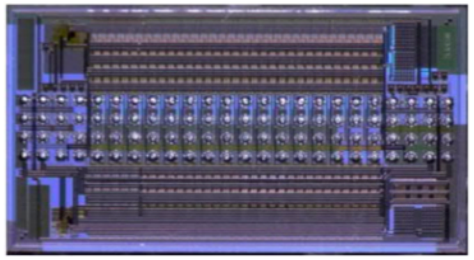
DHP: Data Handling Processor



- TSMC 65 nm
- Size 4.0x 3.2 mm²
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Transmit 1.6 Gbit/s of data over a 15 m cable to the backend.
- Rad. Hard proved (100 Mrad)



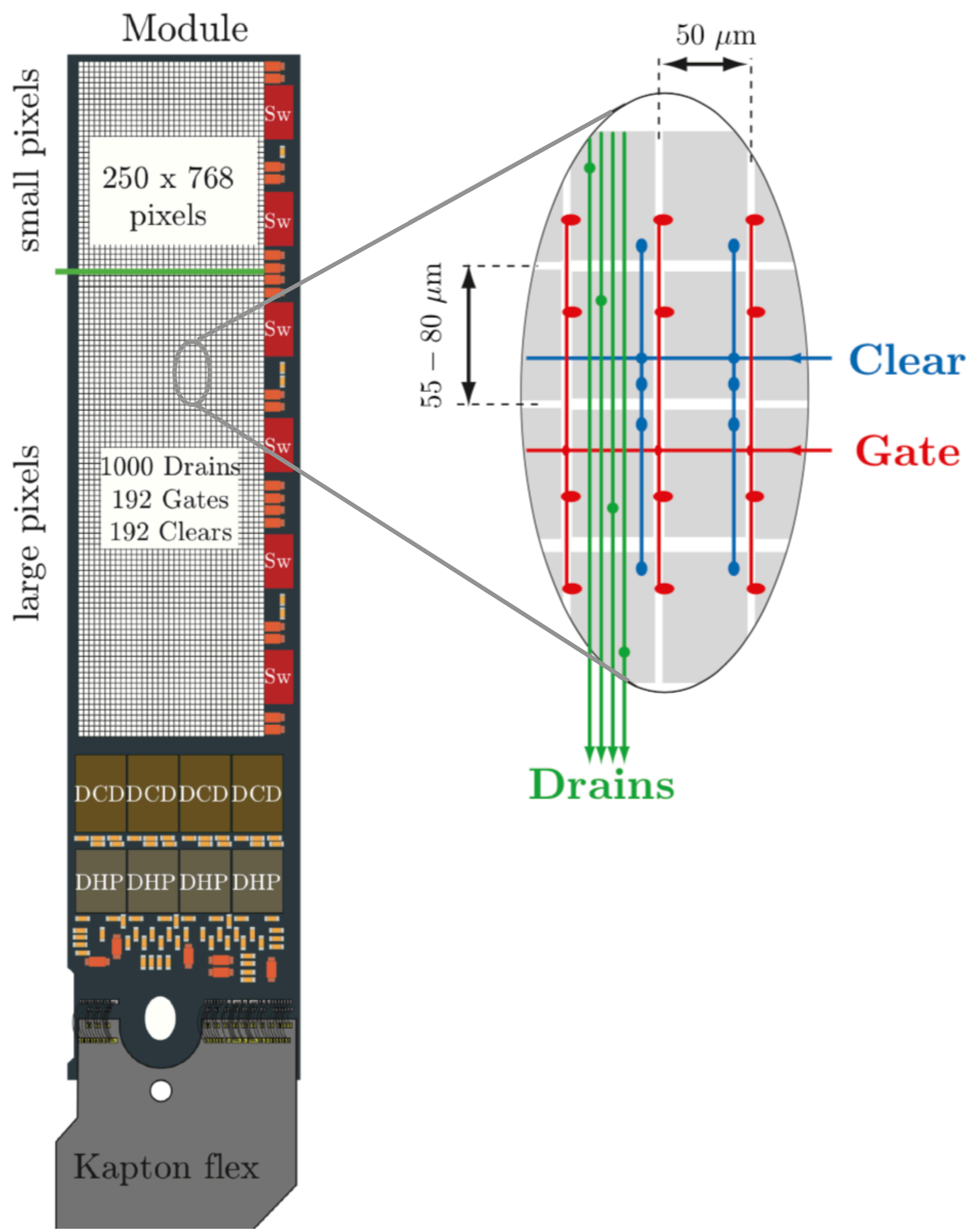
Switcher: Row control



- AMS/IBM HVCMOS 180 nm
- Size 3.6 x1.5 mm²
- Gate and Clear signal
- Fast HV ramp for Clear
- Rad. hard proved (36 Mrad)

Readout Mode

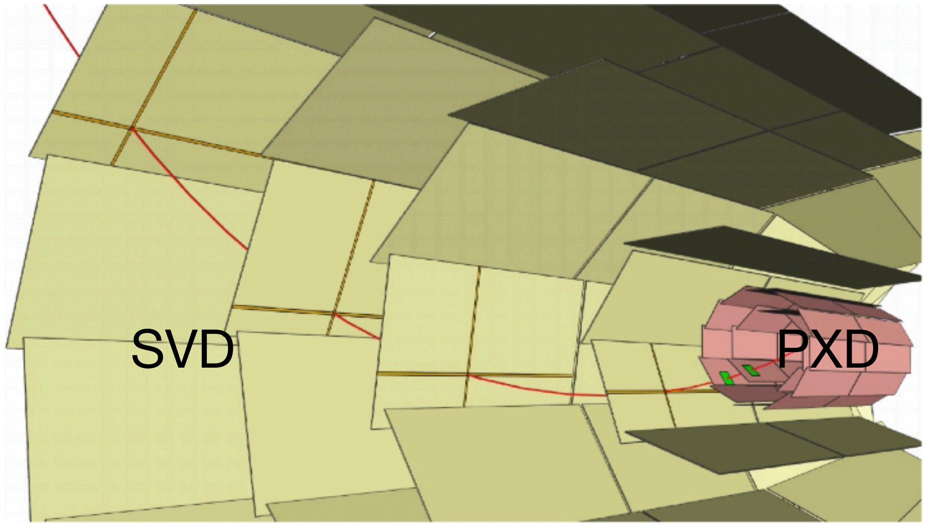
- Rolling shutter mode
  - Read signals gate by gate
  - one gate combines 4 adjacent rows
  - Read-Clear cycle in ~100ns
    - Full integration time is 20μs (twice the revolution time of SuperKEKB)
  - Only 'activated' rows consume power
    - Low sensor power consumption
- Max. acceptable average occupancy <3%. otherwise,
  - data loss,
  - degrade tracking performance.

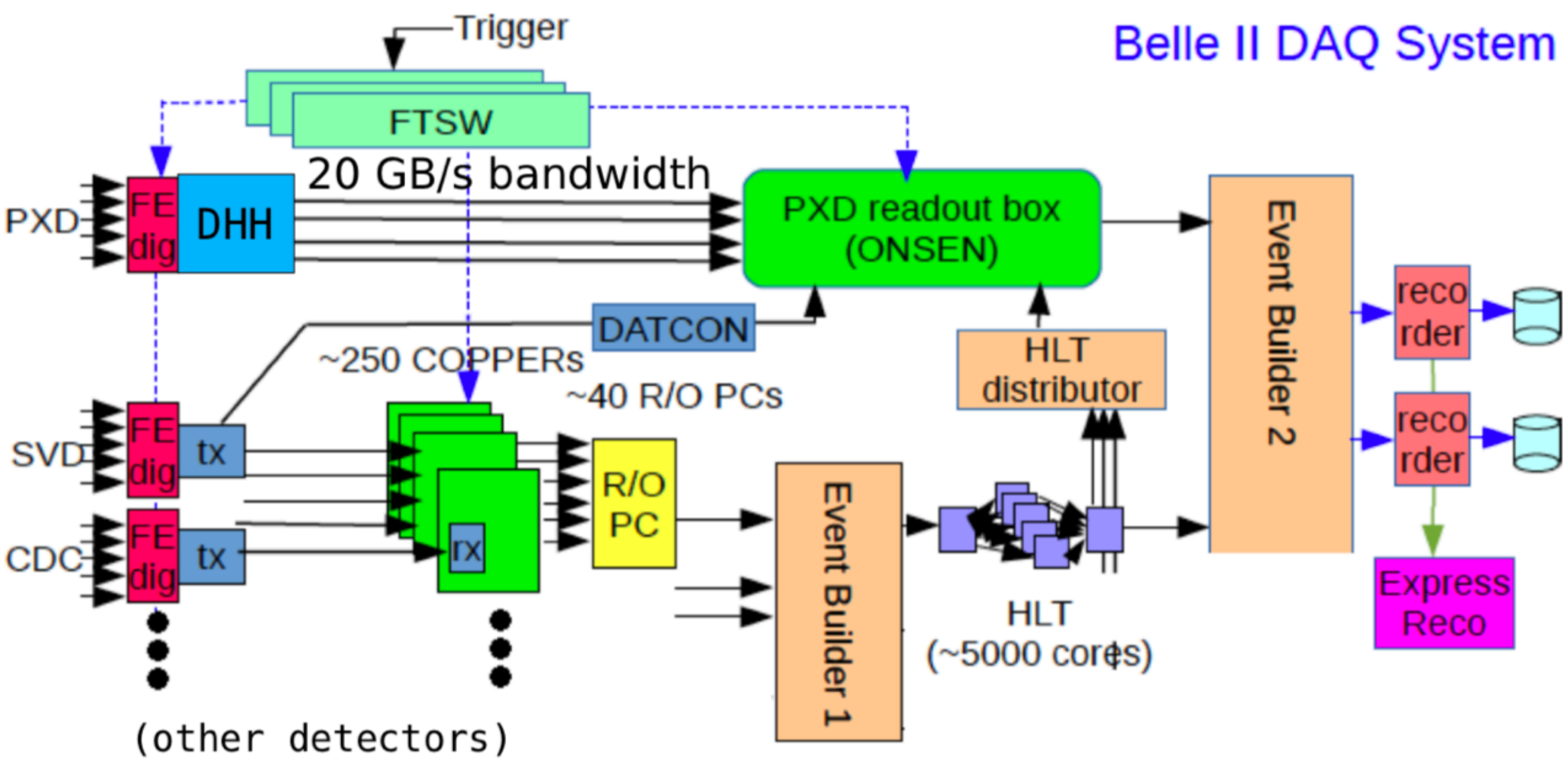


PXD DAQ Scheme

- PXD unfiltered data rate → 10x sum of other Belle II detectors
  - Therefor need separate readout path
  - Data reduction to 1/10 by HLT based ROI calculation from CDC and SVD track information
  - Feedback to PXD readout, selection of pixels within rectangular ROIs

ROI extrapolation on HLT





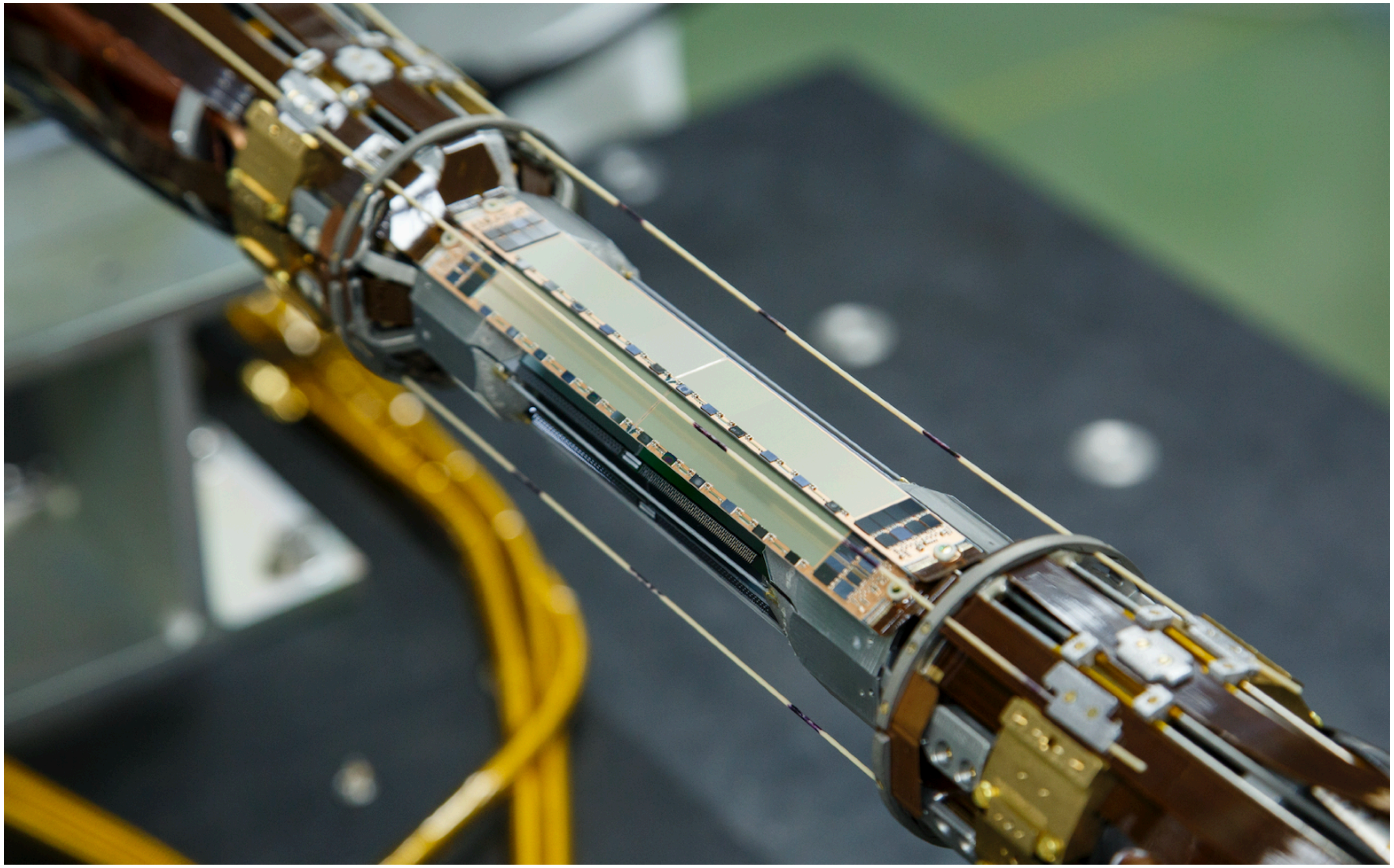
DHH: Data Handling Hub

HLT: High Level Trigger

FTSW: Frontend-Timing-SWitch

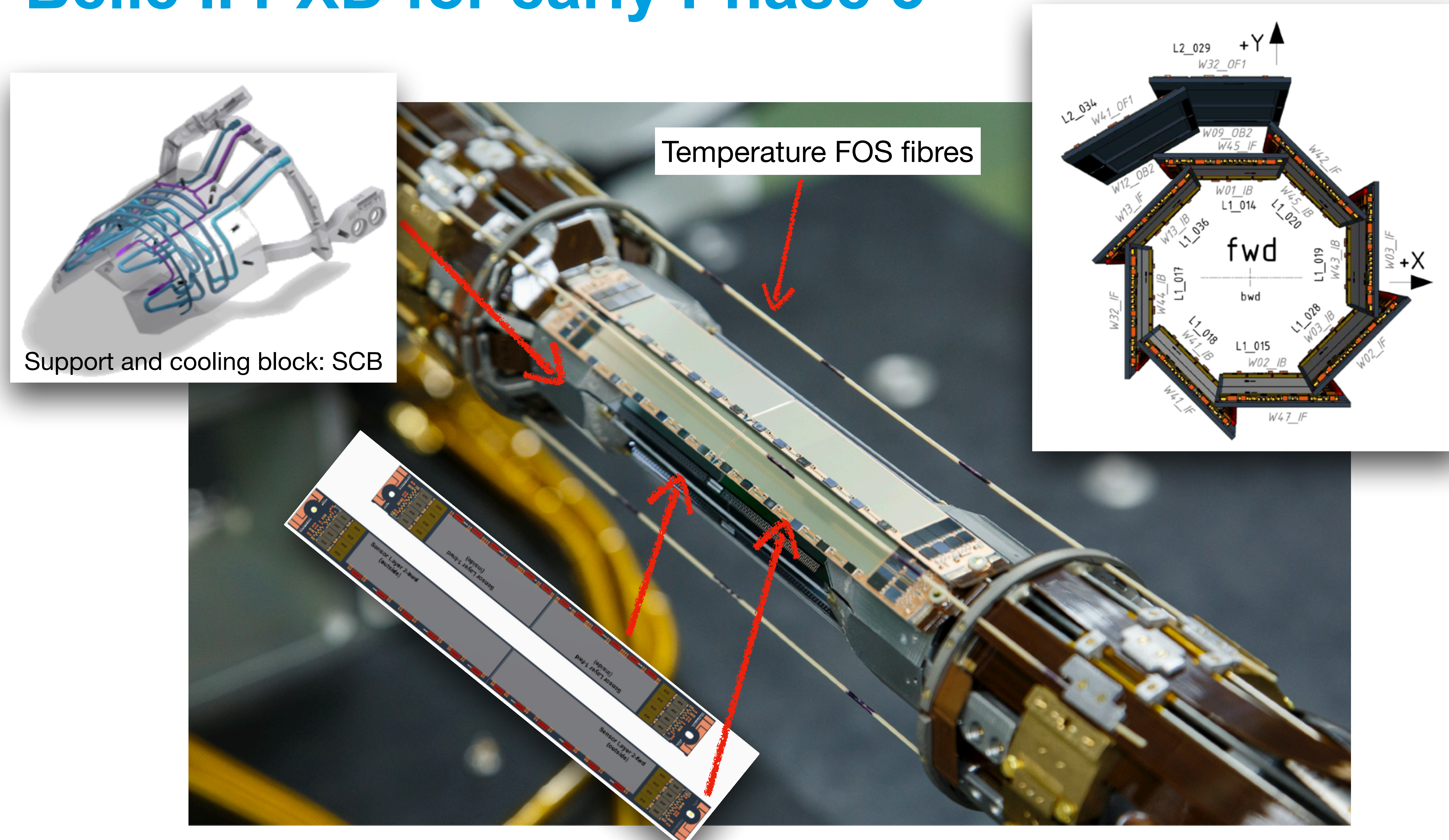
ROI: Region Of Interest

Belle II PXD for early Phase 3



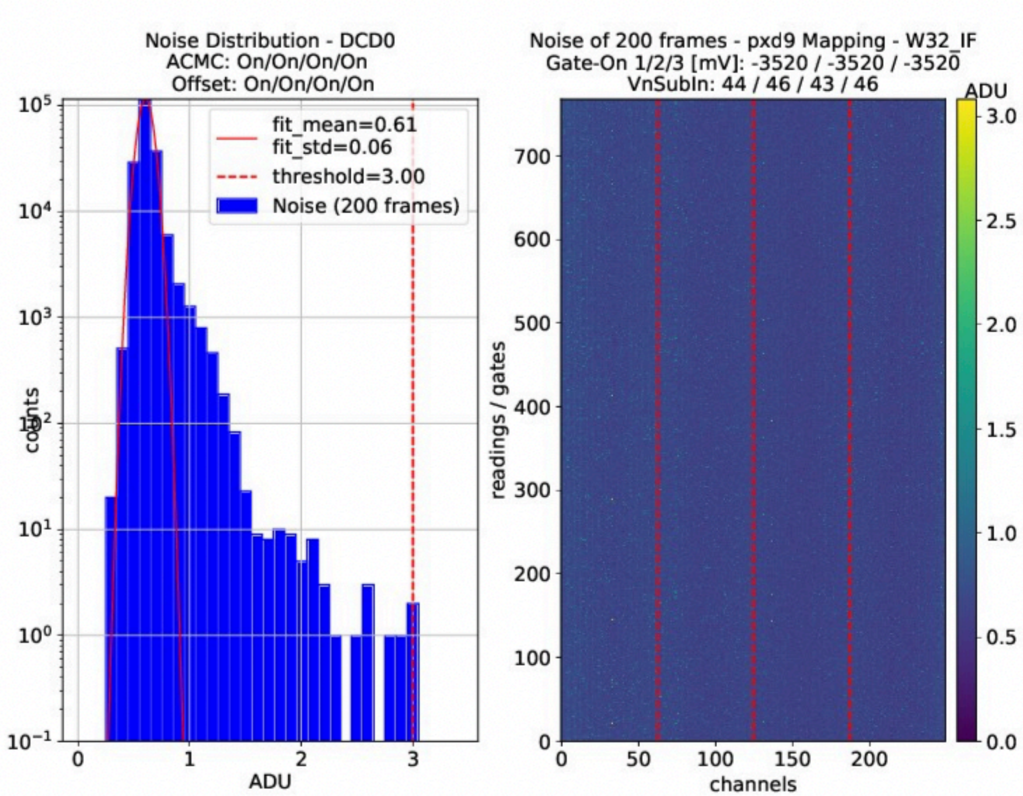
- 2 layers of DEPFET sensors @ r = 14(22) mm
- Sensitive area per module: L1: 12.5mm x 44.8mm, L2: 12.5mm x 61.44mm
- Sensor thickness: 75 µm, 0.21% X_0 per layer

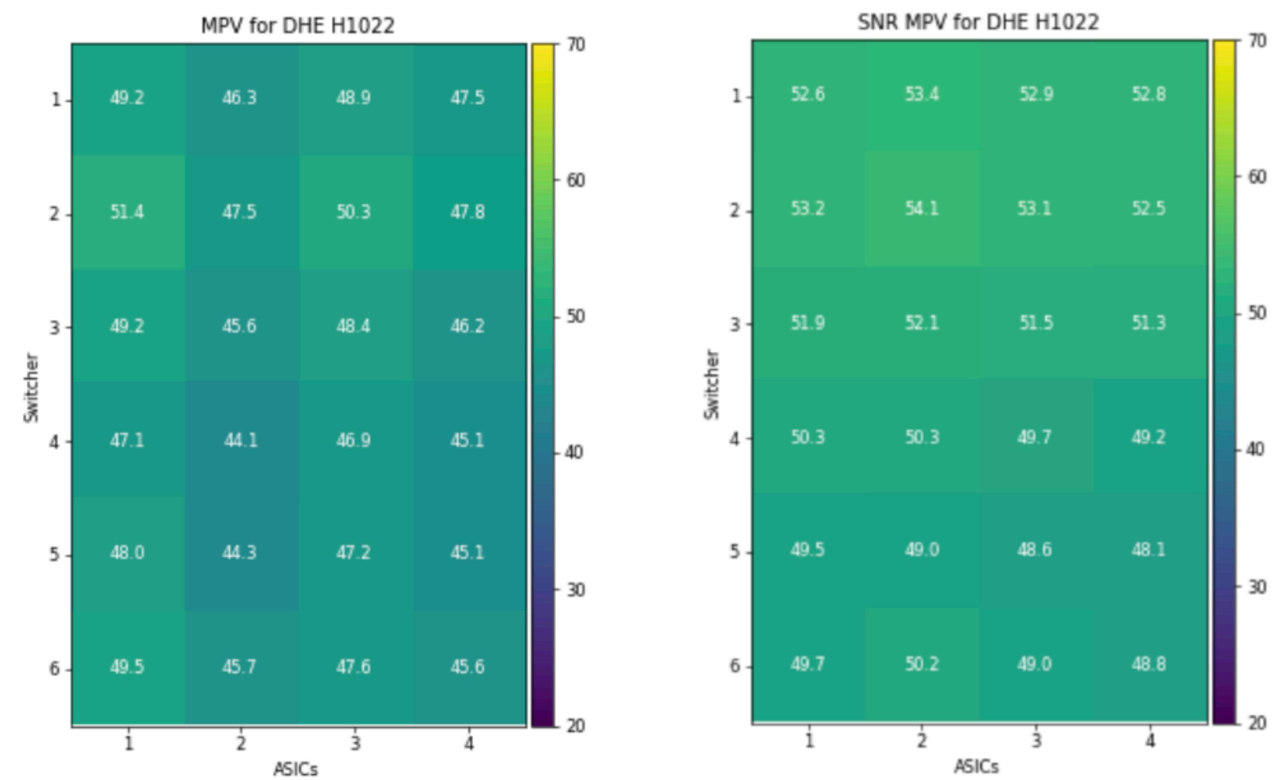
Belle II PXD for early Phase 3



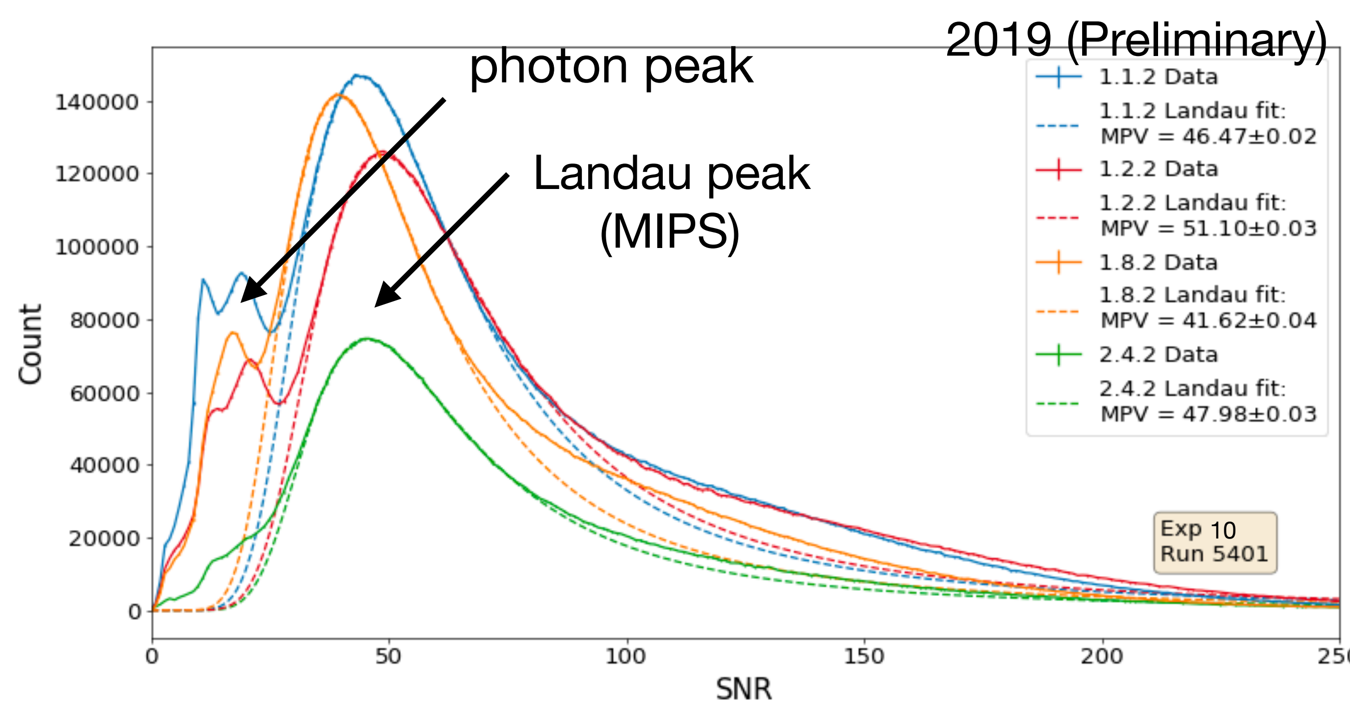
- Each ladder is formed by a pair of mirrored DEPFET sensors
- Due to problems in ladder gluing, only half of designed PXD (full L1+2 L2 ladders) was installed in 2018/2019, will be finalized in 2021.

Signal to Noise Ratio





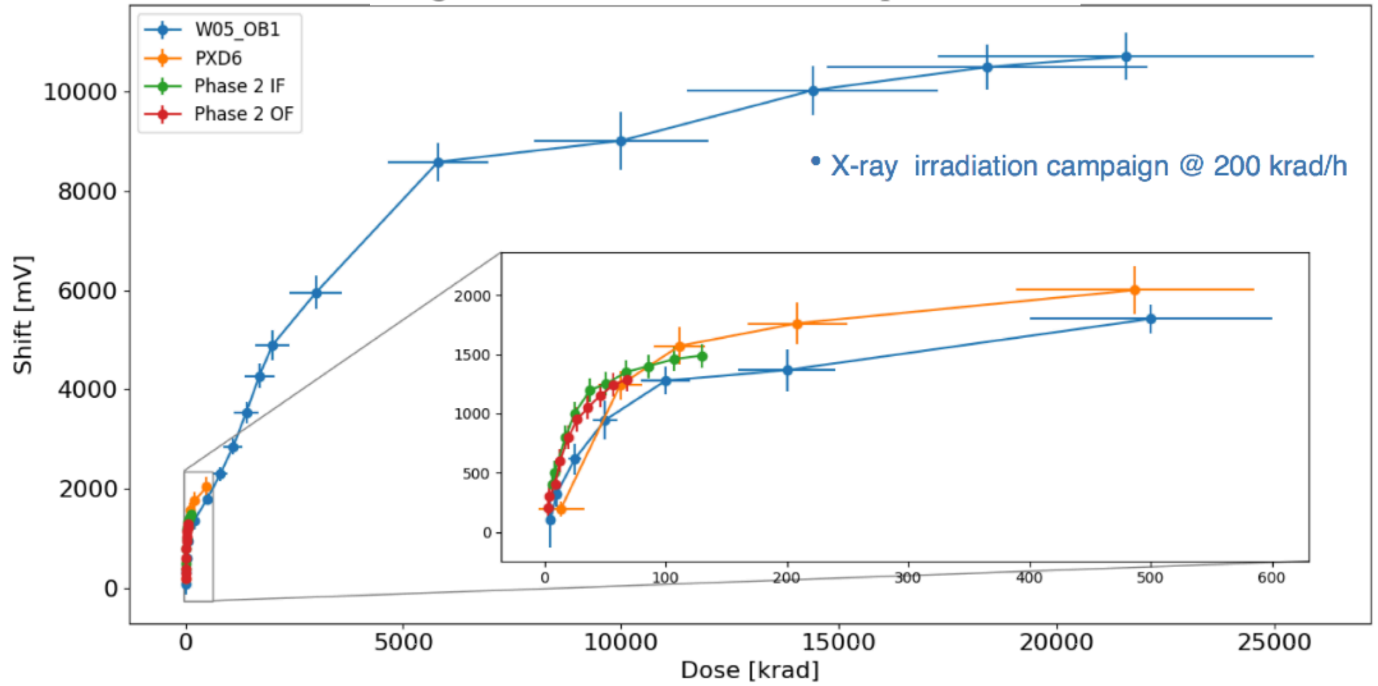
- Low noise (<1ADU, <100e ENC)
- Signal to Noise Ratio ≈ 50
- Most probable value and SNR uniform over ASIC combinations within one module.
- The inner modules feature more prominent contribution originated from low energy synchrotron radiation photons.

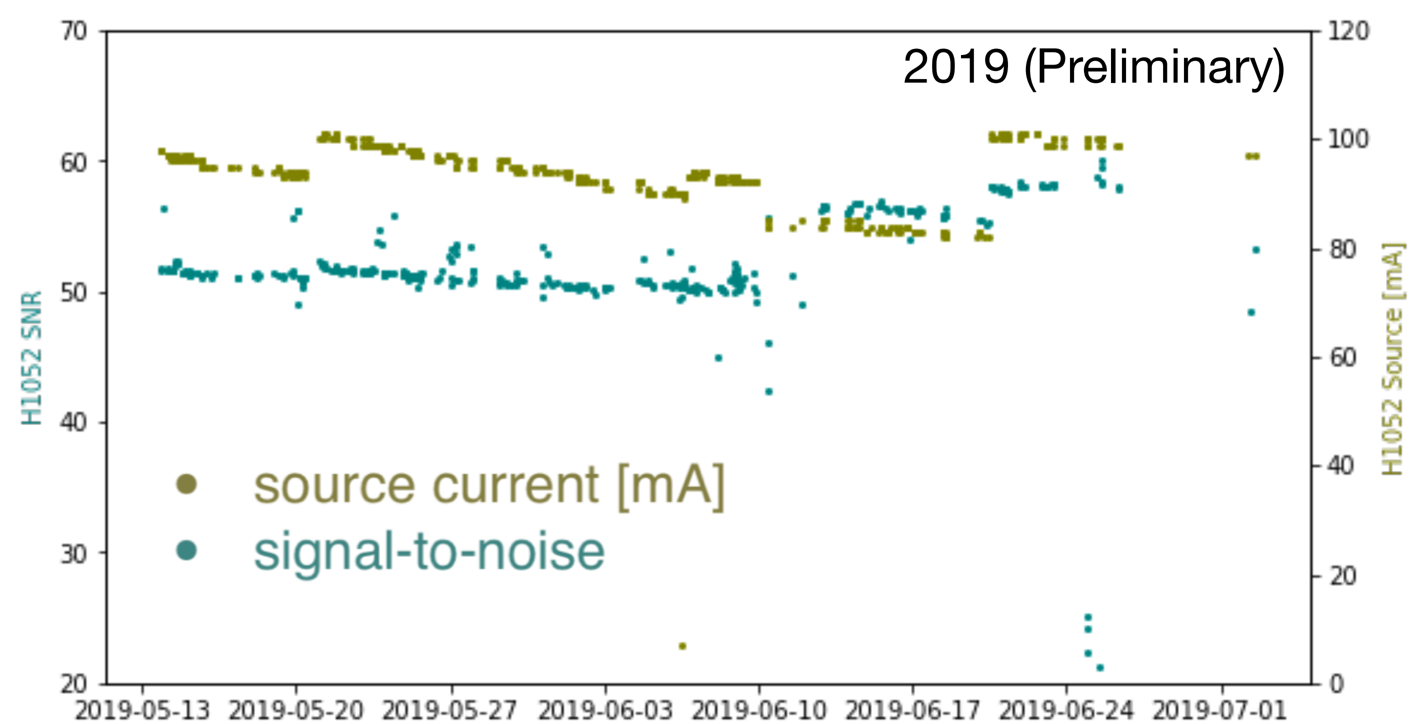


Compensation for Radiation Damage

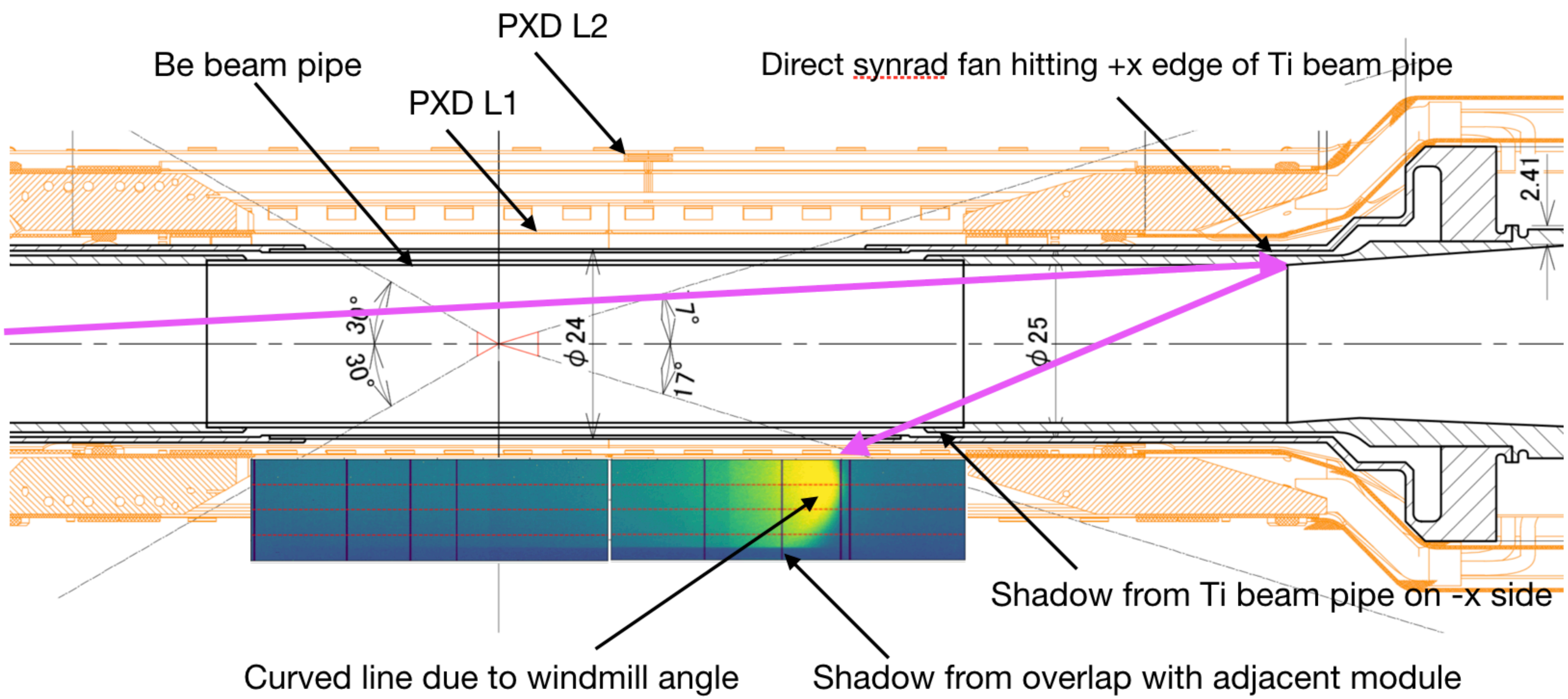
- Defects of SiO_2 cause shift of threshold voltage.
- NIEL is not expected to be an issue.
- Module still functional after > 25 Mrad (corresponding to 250mrad/s for 10 smy)
- In Phase3 operation, voltages are regularly adjusted to have the source current of ~100mA.
  - Tune the internal amplification
  - Tune the coupling between internal gate and clear.

$$(V_{gs} - V_{Thr}) \propto \sqrt{I_D} \propto g_q \propto \mathrm{MPV}$$





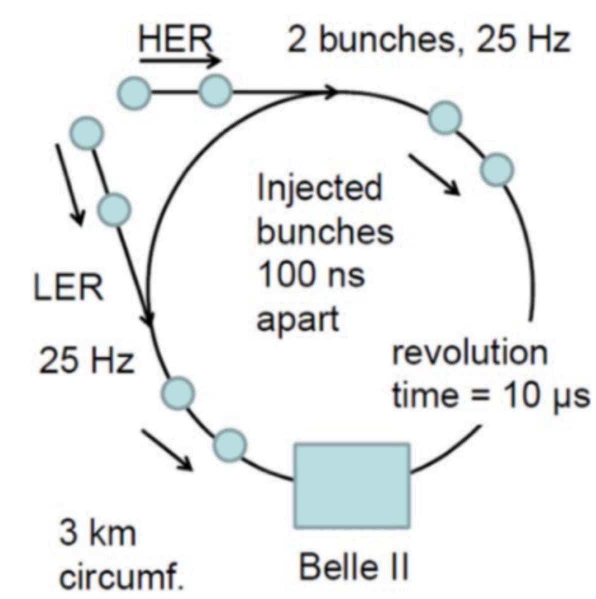
Synchrotron Radiation Background



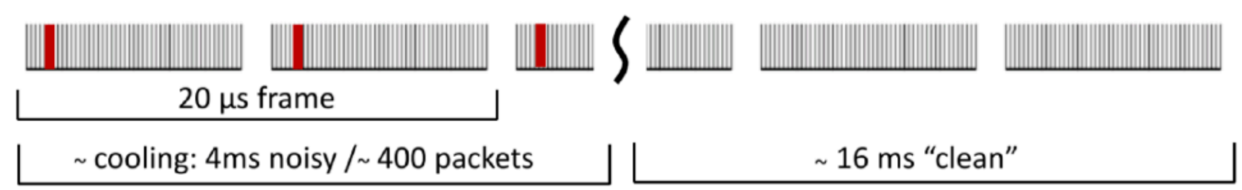
- IR designed such that no direct SR photons hit the central Be beam pipe.
- Large SR background was observed for some runs in a few modules in -x direction.
  - Secondary photons — single pixels, low energy (<10keV)
    - Back scattering photons from direct synrad fan hitting +x edge of Ti beam pipe
    - photons which may be originated from synrad that backscatters further downstream
  - May cause inhomogeneous irradiation

Gated Mode Operation

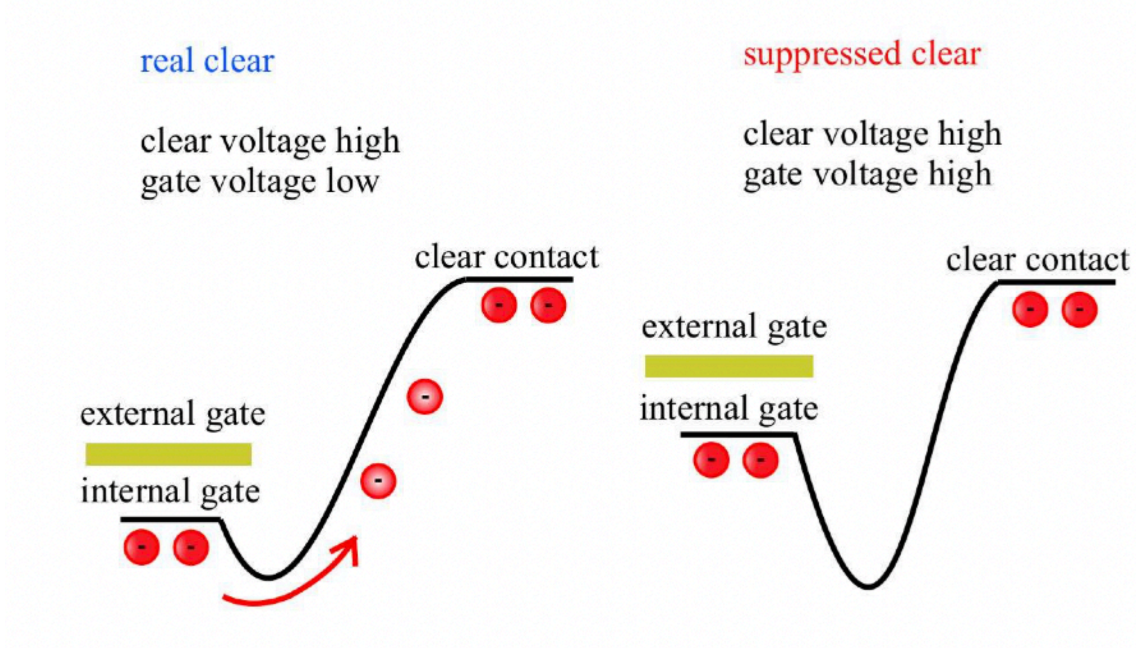
- SuperKEKB is operated in top-up mode: continuous injection
  - At design luminosity Touschek effects limit beam life time to 10 mins
  - Accumulating integrated luminosity effectively.
- Freshly injected bunches produce high background
  - Damping time few ms
- Gated Mode can blind PXD when noisy bunches pass.
  - Newly created charges are not collected
  - Charges in internal gate are preserved

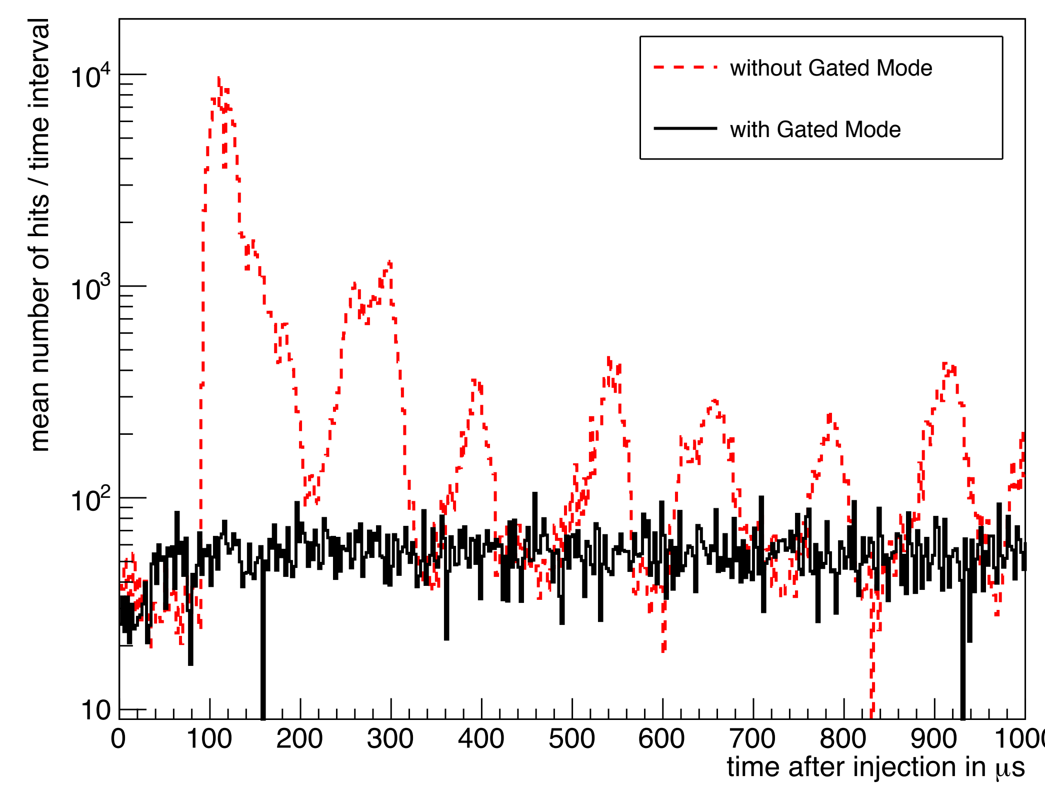


SuperKEKB bunch pattern



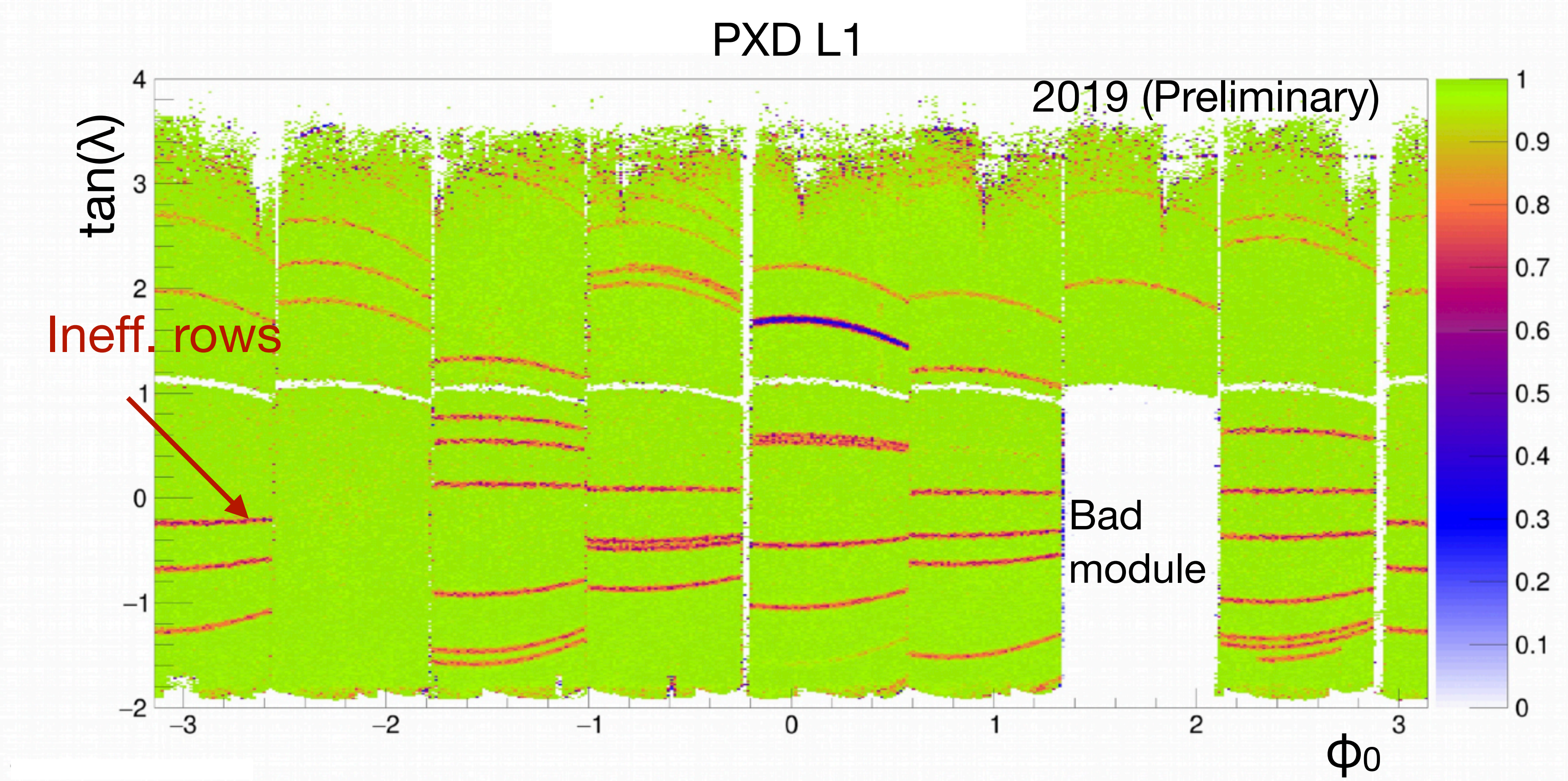
DEPFET Gated Mode





PXD Operation & Performance

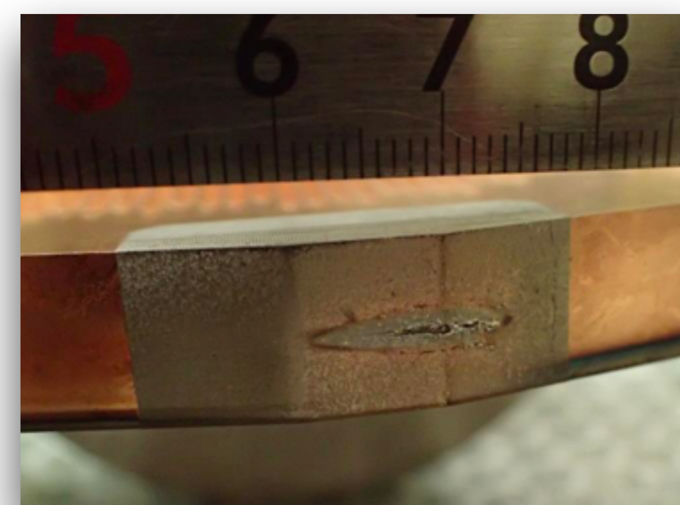
Hit Efficiency



λ ≡ π/2 – θ, angle between a track and the plane ⊥ to the beam.

LER beam loss event

- 150mA beam current lost in 40 μs, estimated dose in PXD: ~ 5 Gy (0.5krad).
- Severely damaged vertical collimator
- Major quench of final focus magnet system
- Damage in PXD

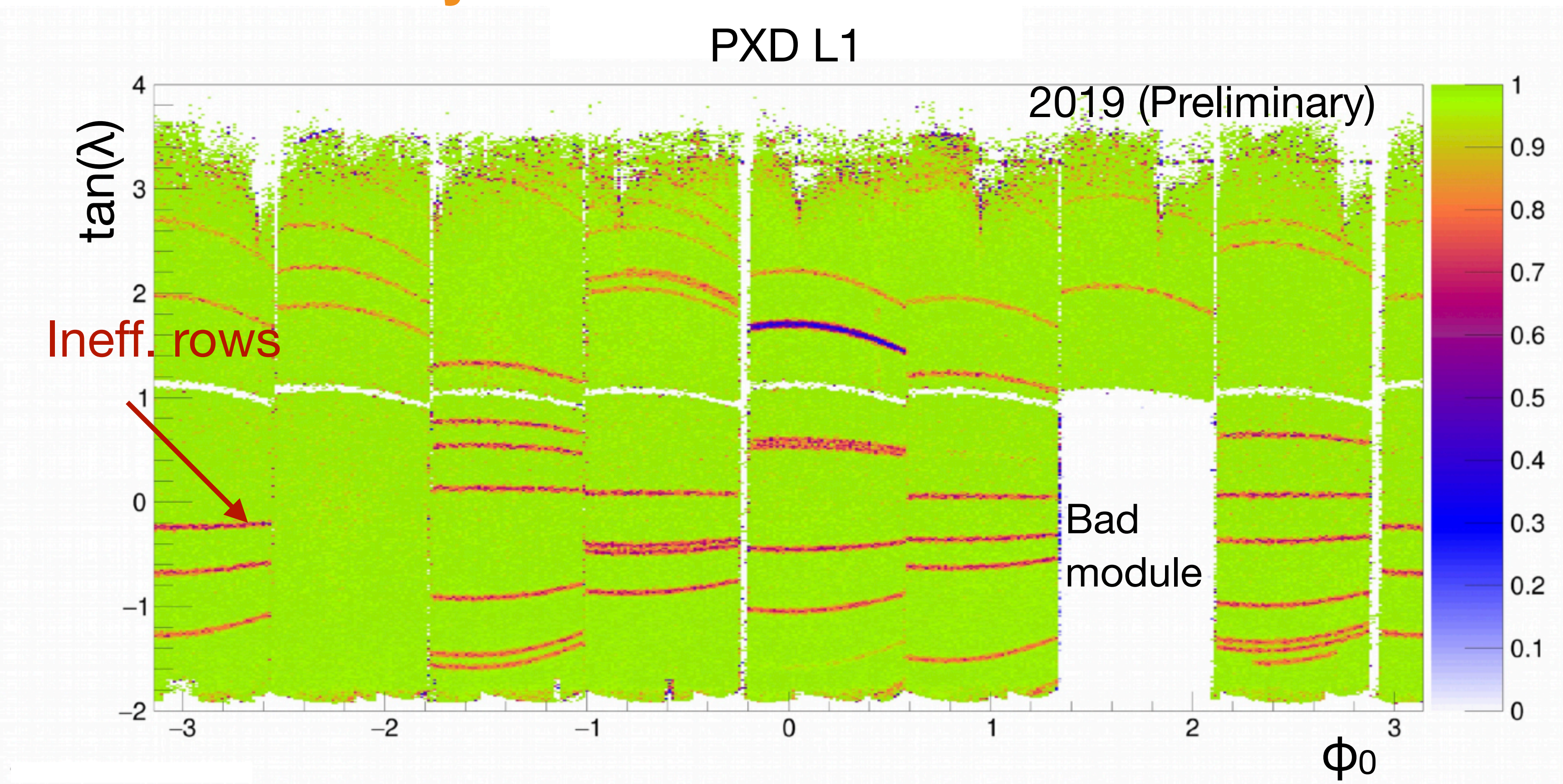


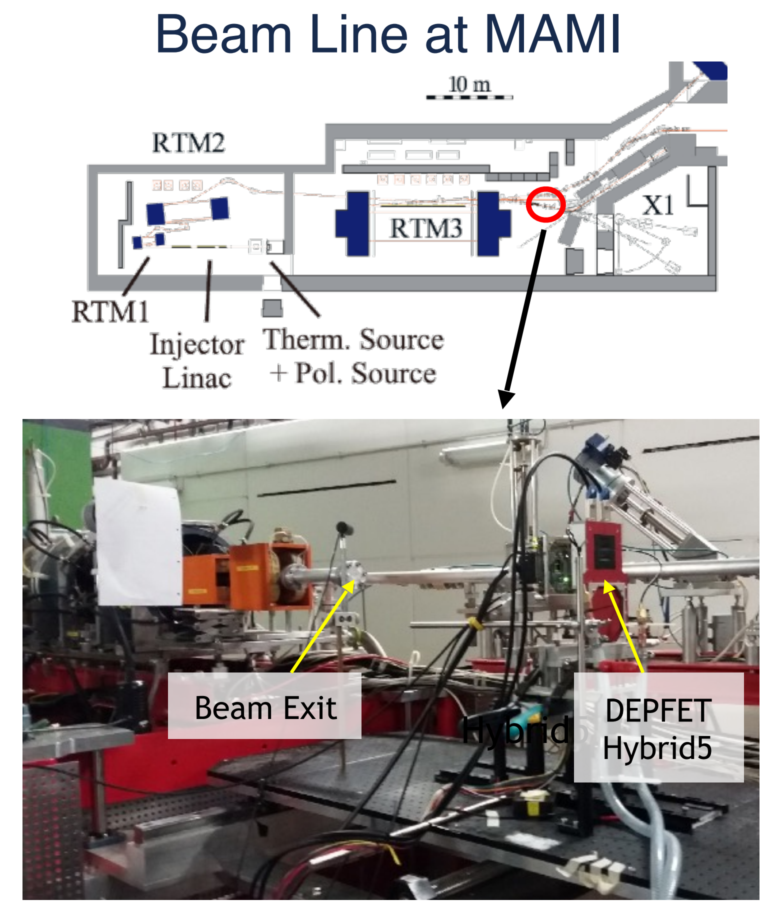
The high radiation dose in the beam loss is a threat to the machine (collimator, final focus magnets) and pixel detector.

- Inoperable PXD module, recovered afterwards.
- Working point shifted.
- Increased number of inefficient rows (~2%). → points to possible damages in Switcher

PXD Operation & Performance

Hit Efficiency



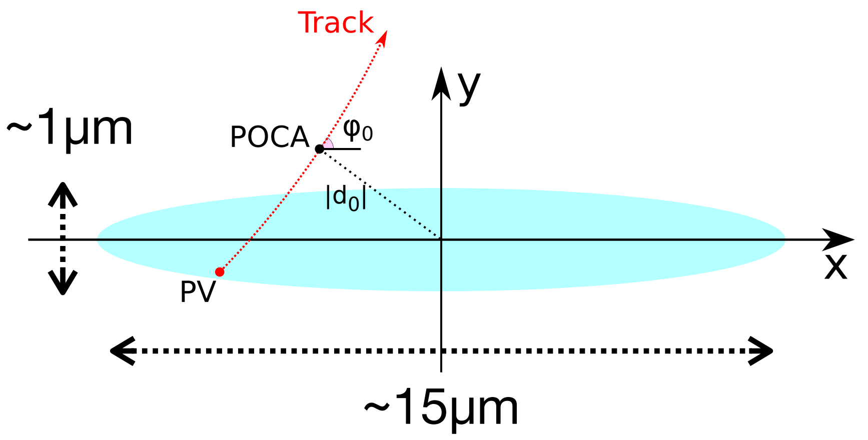


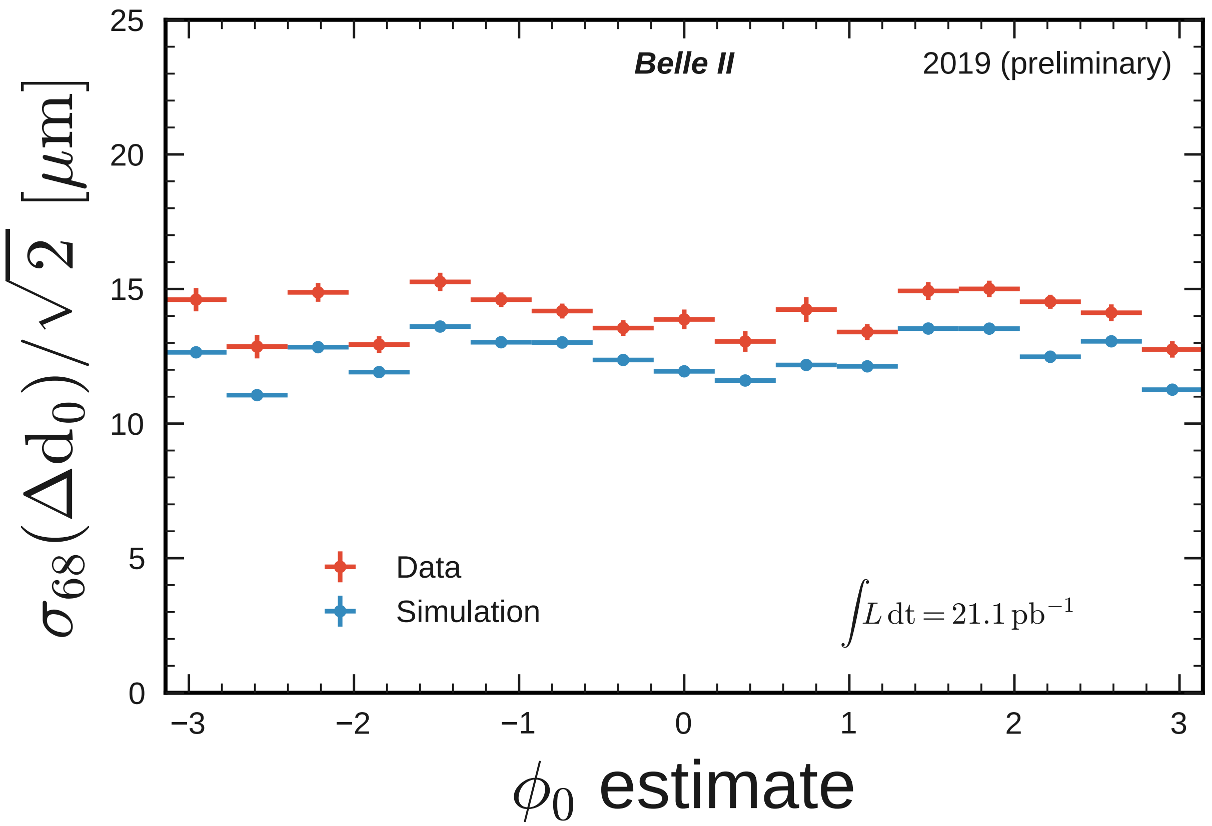
- Radiation burst tolerance Study
  - Switchers and DEPFET matrix have been irradiated with a focused pencil beam of electrons (855 MeV) at MAMI, Mainz
  - A particular region of the Switchers where the voltage regulators is located, is found to be sensitive to the radiation bursts.
  - The dose is compatible with the estimate at the beam incidents.
- Improving the protection scheme
  - PXD: the scheme of fast emergency shutdown is prepared, O(100ms) -> O(100μs)
  - Machine side: faster abort logic , increase number of abort gaps (1->2), modify the collimator system.

VXD Performance

Transverse Impact Parameter Resolution

- Exploit small and flat transverse beam spot size in SuperKEKB
  - Use ϕ-dependence of track impact parameter (d_0) resolution to study beam profile
  - Use dimuon events to measure intrinsic d_0 resolution
- Unfold the beam profile: size consistent with expectations.

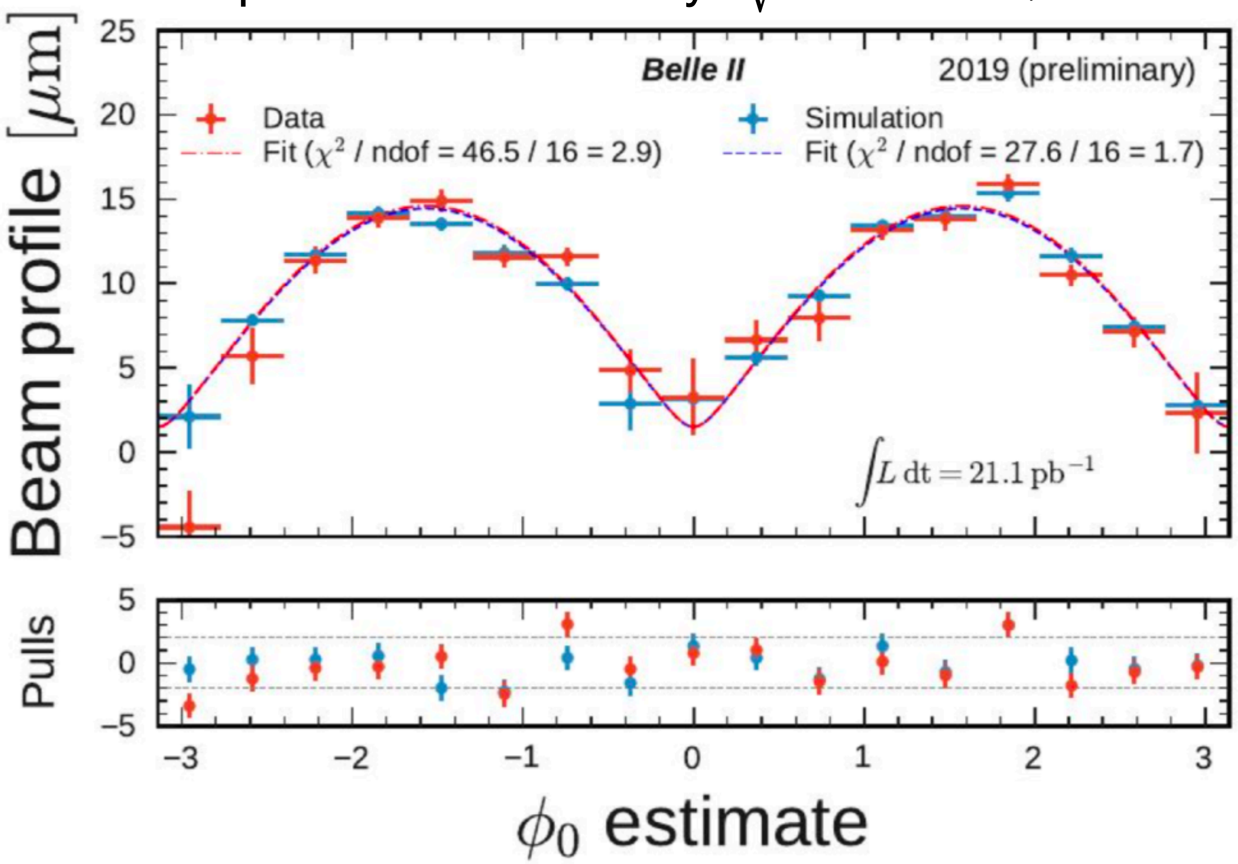




Data: $\sigma_i = 14.1 \pm 0.1\mu m$

MC: $\sigma_i = 12.5 \pm 0.1\mu m$

Beam profile described by $\sqrt{(\tilde{\sigma}_x sin\phi_0)^2 + (\tilde{\sigma}_y cos\phi_0)^2}$



VXD Performance

Transverse Impact Parameter Resolution

- Exploit small and flat transverse beam spot size in Supe
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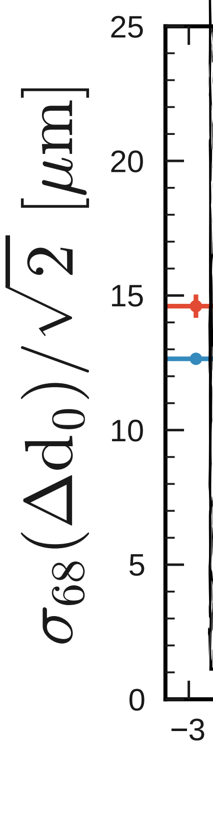

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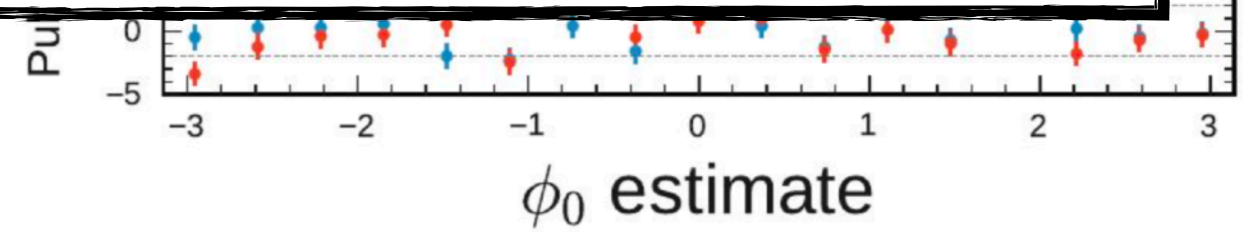
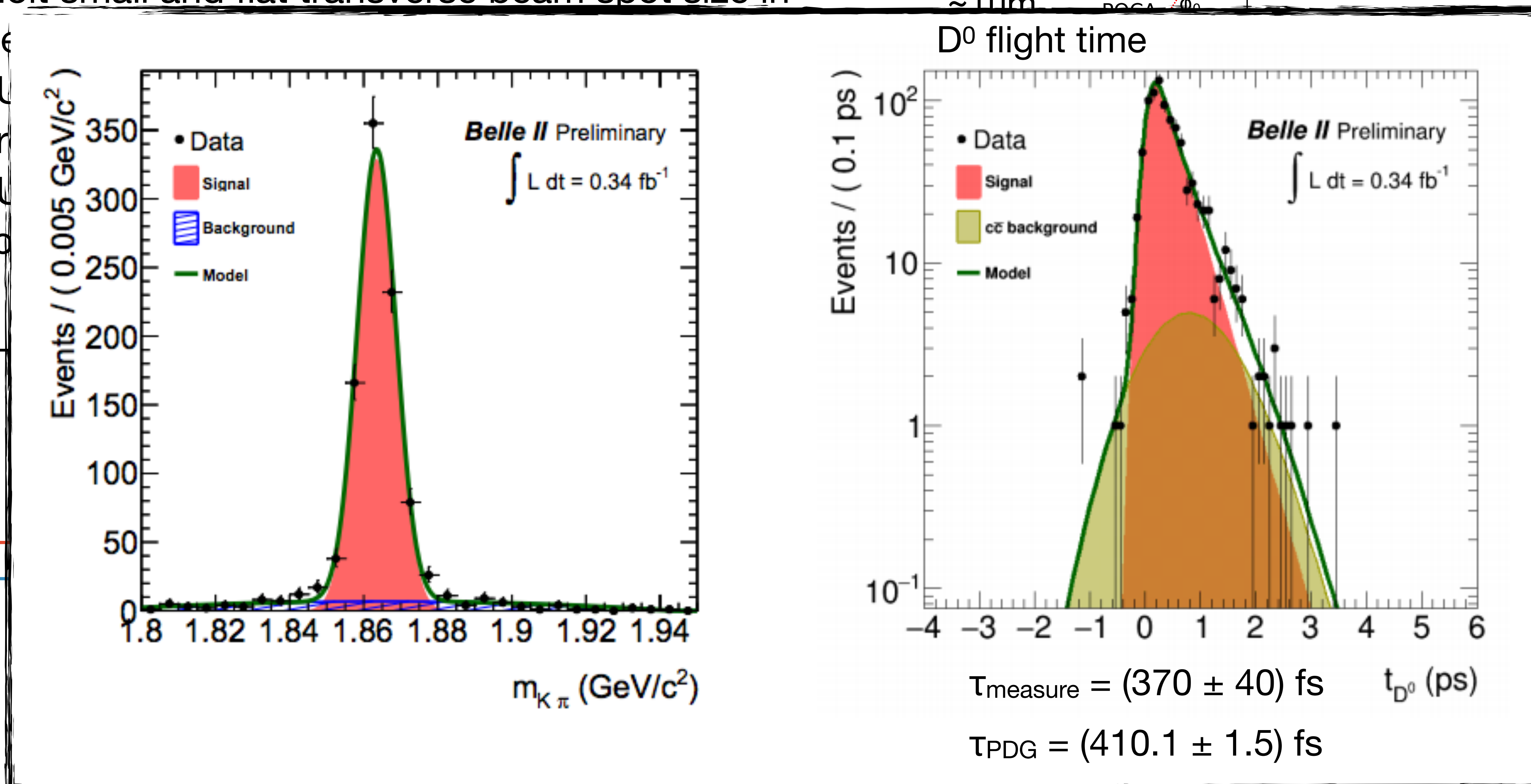




$\tau_{measure}$ = (370 ± 40) fs

τ_{PDG} = (410.1 ± 1.5) fs

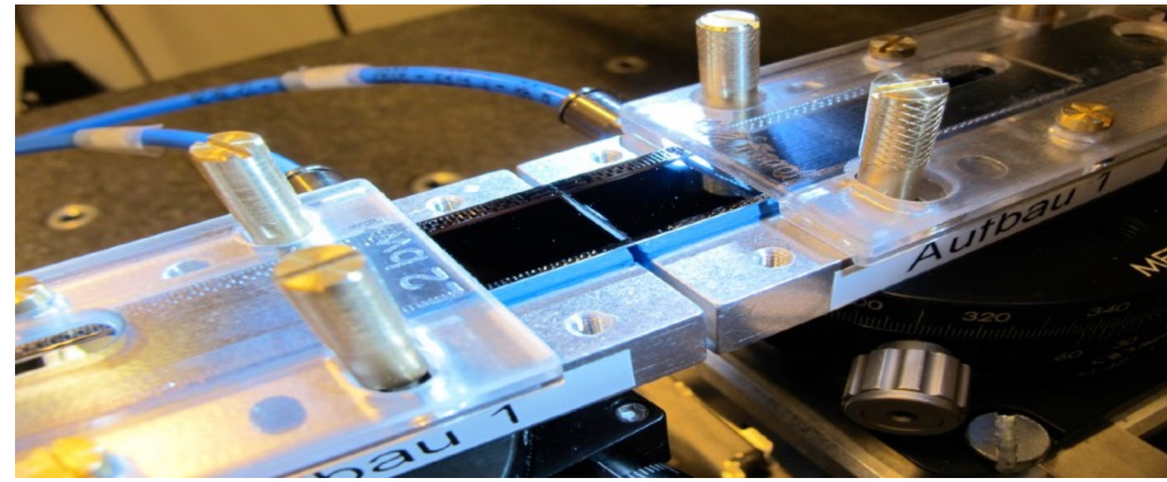
Summary

- The first beam collision experience with the new pixel concept (DEPFET) and half of the full scaled detector has been achieved.
  - Challenging operating conditions close to the IP at a very ambitious machine like SuperKEKB
- PXD system has been continuously improved and optimized during the 2019 runs.
- Good PXD performance is demonstrated.
- Irradiation damage to PXD from beam loss events is under investigation.
  - SuperKEKB and Belle II need to minimize the probability and impact of major un-controlled beam losses.
  - Protection scheme is being improved.

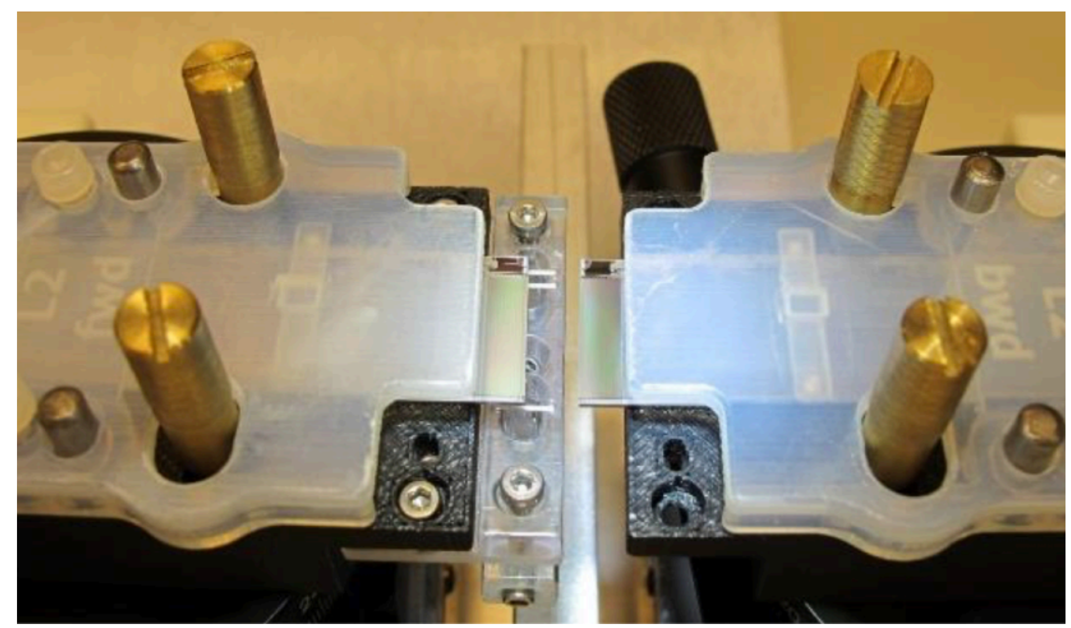
Backup

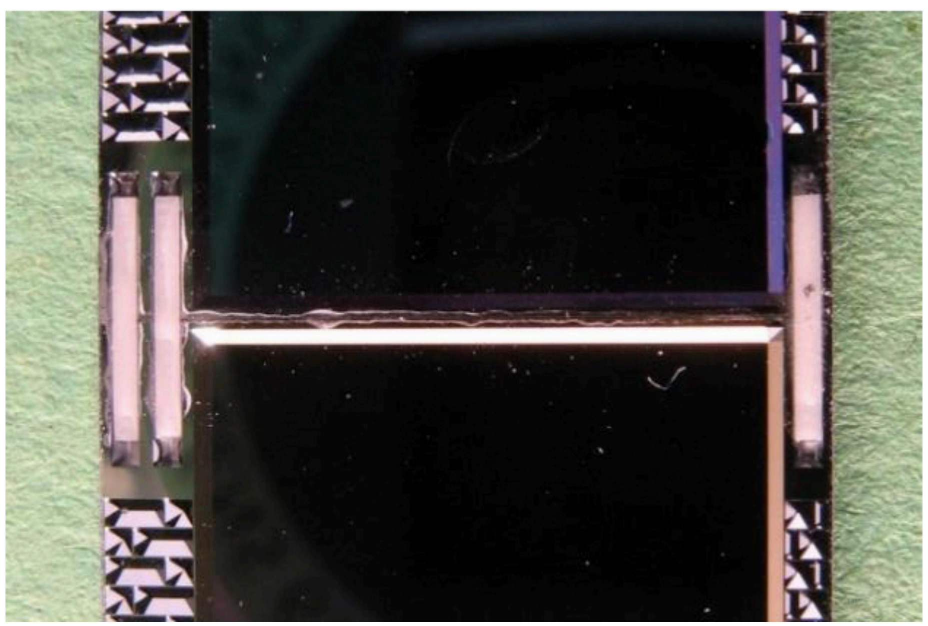
Ladder Gluing

- De-scoped PXD was installed in 2018/2019,
  - Due to relatively high failure rate in ladder gluing procedure → solved!
  - Replacement with full PXD is scheduled in 2021.



Improved ladder gluing scheme

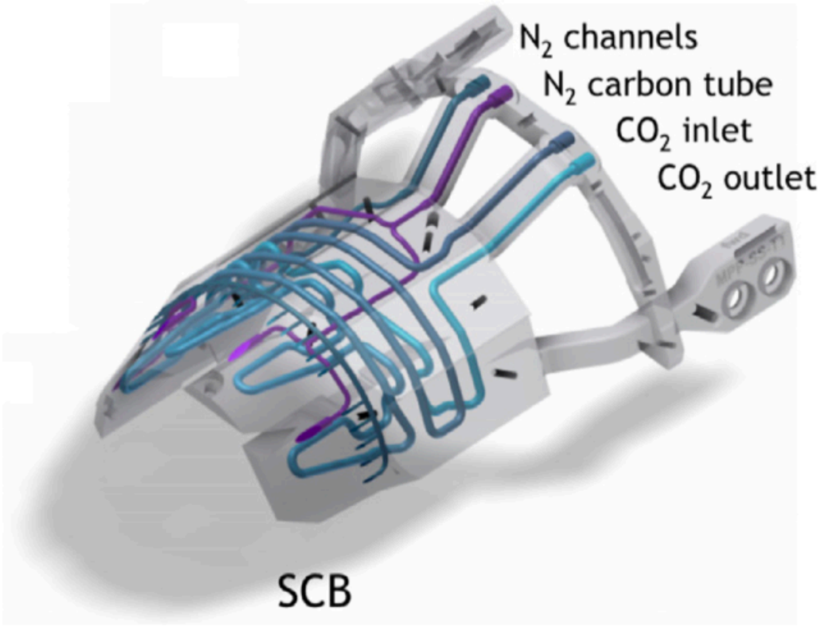




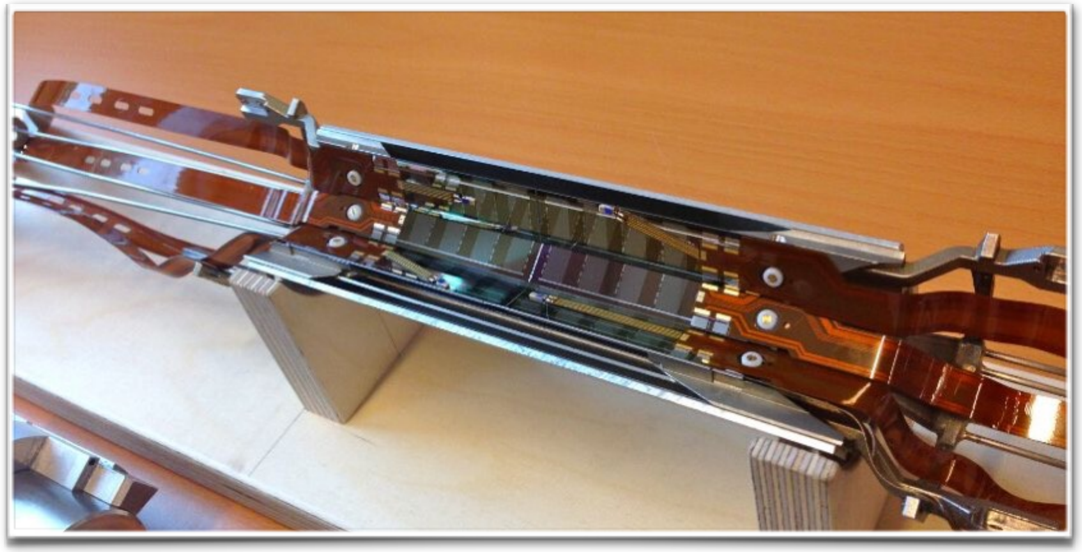
Small ceramic inserts on the back side
→ reinforcement of the joint

Thermal Management

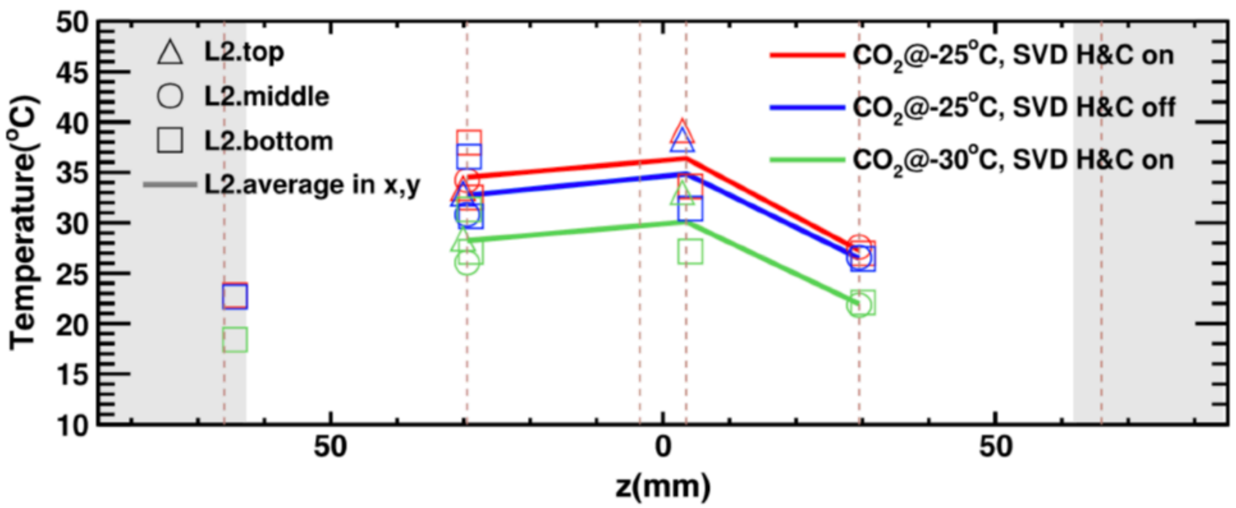
- The power consumption of full PXD is 420W,
  - 360W are contributed from DCD/DHP, which are located in the end of stave.
    - ➡ Active 2 phase CO2 cooling is required there.
  - Little power derived from matrix (0.5W per module) and Switchers (1W per module)
    - ➡ Forced N_2 cooling is sufficient in the sensitive area.



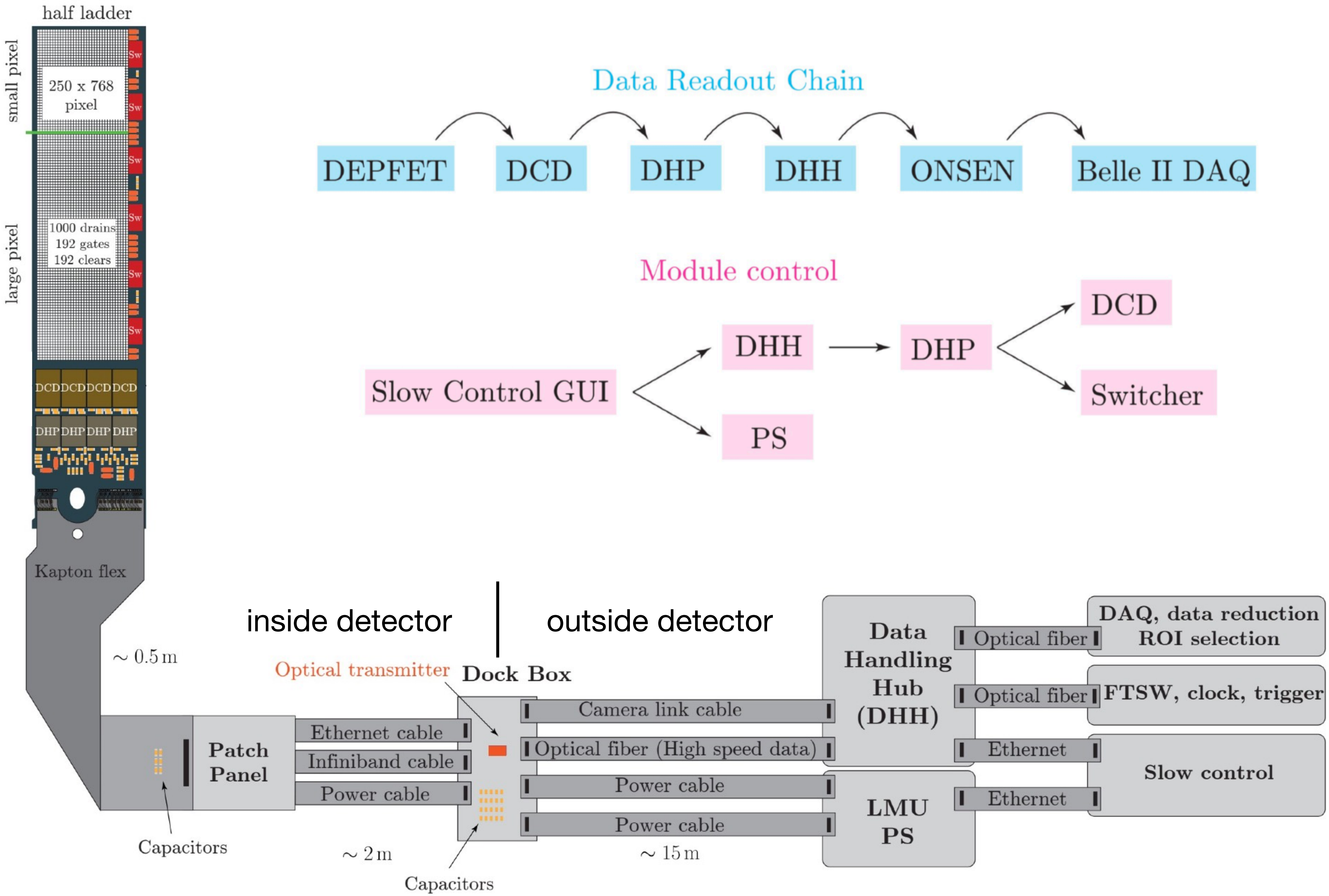
Thermal mock-up (half-shell)



Temperature along the PXD ladder



PXD Layout



half ladder
small pixel
large pixel
250 x 768 pixel
1000 drains
192 gates
192 clears
Sw
DCD DCD DCD DCD
DHP DHP DHP DHP
Kapton flex
Data Readout Chain
DEPFET
DCD
DHP
DHH
ONSEN
Belle II DAQ
Module control
Slow Control GUI
DHH
PS
DHP
DCD
Switcher
inside detector
outside detector
~ 0.5 m
Optical transmitter
Dock Box
Patch Panel
Ethernet cable
Infiniband cable
Power cable
Camera link cable
Optical fiber (High speed data)
Power cable
Power cable
Data Handling Hub (DHH)
LMU PS
Optical fiber
Optical fiber
Ethernet
Ethernet
DAQ, data reduction ROI selection
FTSW, clock, trigger
Slow control
Capacitors
~ 2 m
Capacitors
~ 15 m

Module Calibration

- Optimization of ASIC and DEPFET parameters, e.g.
  - DHP input delay elements
  - DCD internal current source
  - charge collection
- Narrow and stable pedestals
- Low noise (<1ADU, <100e ENC)

ADC Transfer Curve