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Development of high resolution low power CMOS pixel sensor for the CEPC vertex detector

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On behalf of the JadePix3 design team

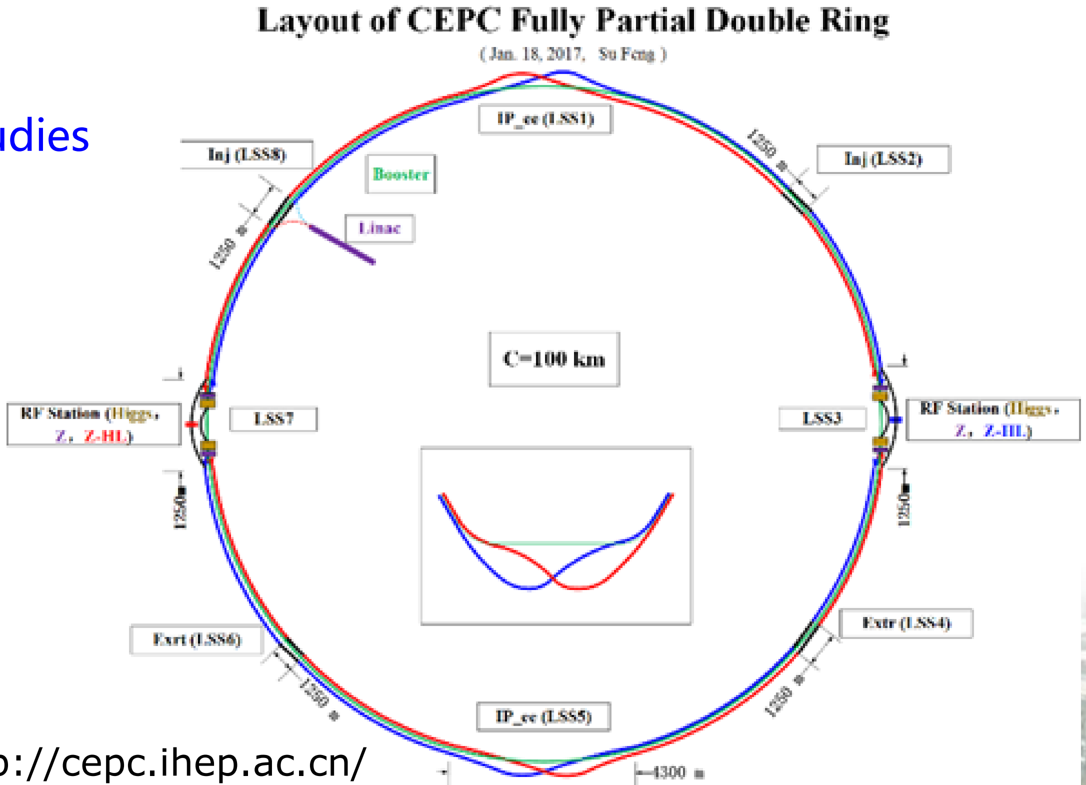
Dec. 16, 2019

Outline

- Introduction
  - CEPC and its Vertex detector
- Key design choices
  - Readout: binary vs analog
  - Discriminator: In-pixel vs end-of-column
- R&D activities
- Design of JadePix3
  - Diode
  - Front-end
  - Readout architecture
- Outlook on further development
  - Vertical integration with SOI-3D

Physics goals of CEPC

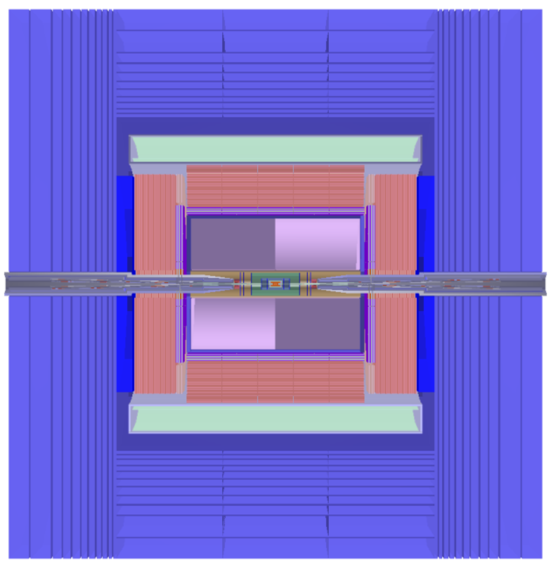
- Circular Electron-Positron Collider (90, 160, 250 GeV)
  - Higgs factory (10^6 Higgs)
    - Precision study of Higgs, similar & complementary to ILC
    - Looking for hints of new physics
  - Z & W factory (10^{10} Z^0)
    - Precision test of SM
    - Rare decays
  - Flavor factory: b, c and QCD studies

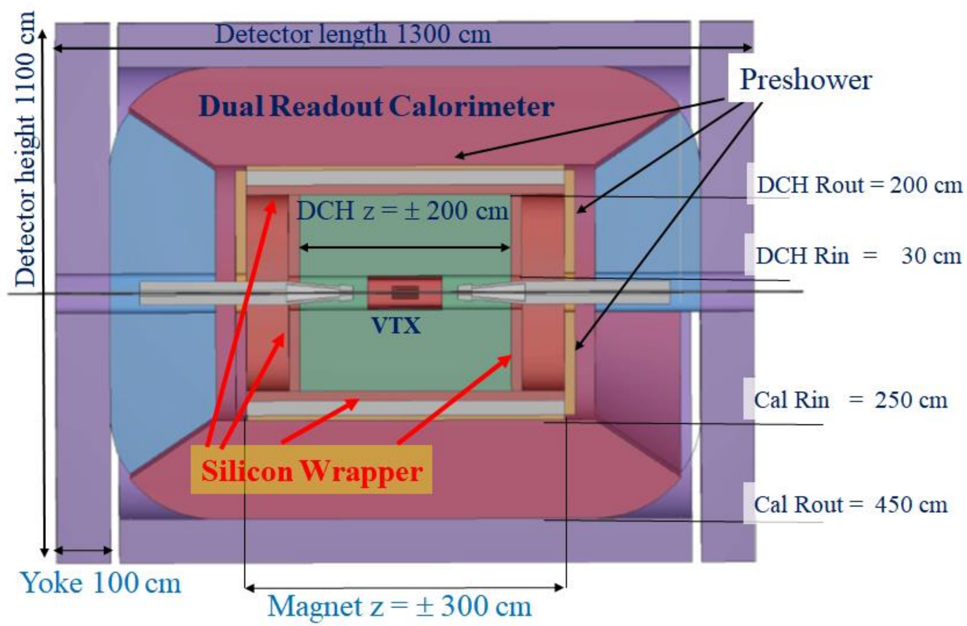


Conceptual Design Report available at http://cepc.ihep.ac.cn/

Two Detector Concepts

- Baseline detector concept
  - either Silicon tracker + TPC or Full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector
- Alternative detector concept, IDEA
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber





Pixel Sensor Specifications

- Efficient tagging of heavy quarks (b/c) and τ leptons

→ impact parameter resolution

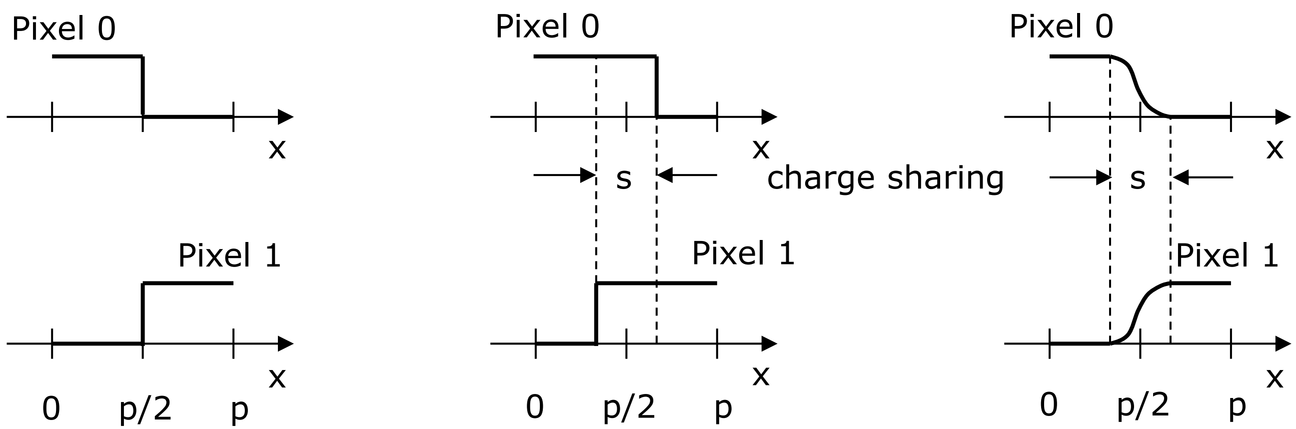
$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\ (\mu m)$$

Physics driven requirements	**Running constraints**	**Sensor specifications**
$\sigma_{s.p.}$ 2.8 μm →		Small pixel 16 μm
Material budget 0.15% X_0 / layer →		Thinning 50 μm
Material budget →	Air cooling →	Low power 50 mW / cm^2
r of Inner most layer 16 mm →	beam-related background →	Fast readout 1 ~ 100 μs
r of Inner most layer →	radiation damage →	Radiation tolerance *3.4 Mrad / year* *6.2×10^{12} n_{eq} / (cm^2 year)*

Readout: binary vs analog

- Influential factors of spatial resolution
  - Pixel pitch 'p'
  - Readout mode and charge sharing region 's'

Signals in two adjacent pixels as function of the impact position x



Binary readout without charge sharing

$$\sigma_{position} = p/\sqrt{12}$$

Binary readout with charge sharing

$\sigma_{position} = s/\sqrt{12}$, inside the s region

$\sigma_{position} = (p-s)/\sqrt{12}$, outside the s region

Analog readout

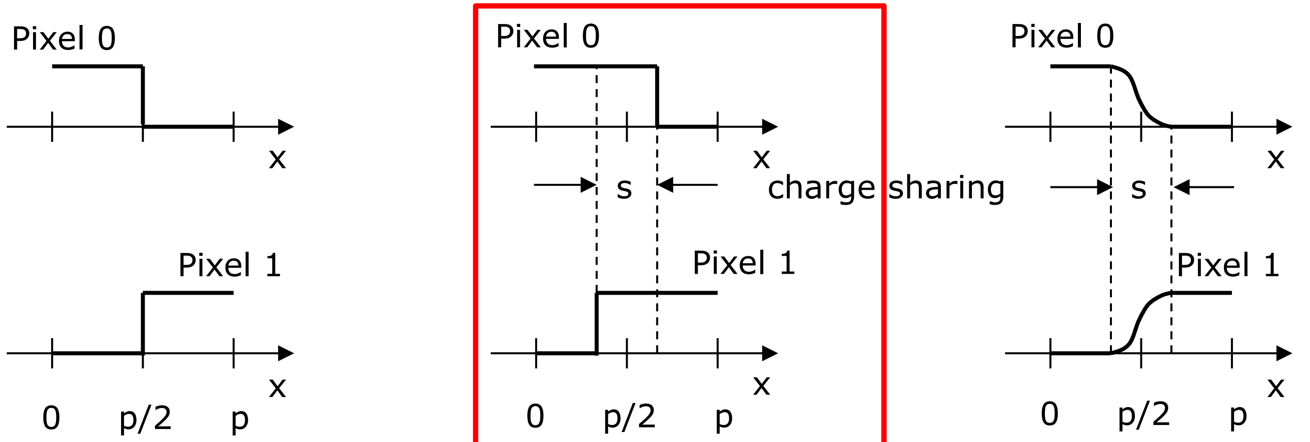
$\sigma_{position} = \frac{s}{S/N}$ inside the s region

$\sigma_{position} = (p-s)/\sqrt{12}$, outside the s region

Readout: binary vs analog

- Binary readout with charge sharing
  - $\sigma_{position} = \frac{p/2}{\sqrt{12}}$, when s = p/2.
  - 16um < p <20um required for CEPC

Signals in two adjacent pixels as function of the impact position x



Binary readout without charge sharing

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Analog readout

$\sigma_{position} = \frac{s}{S/N}$ inside the s region

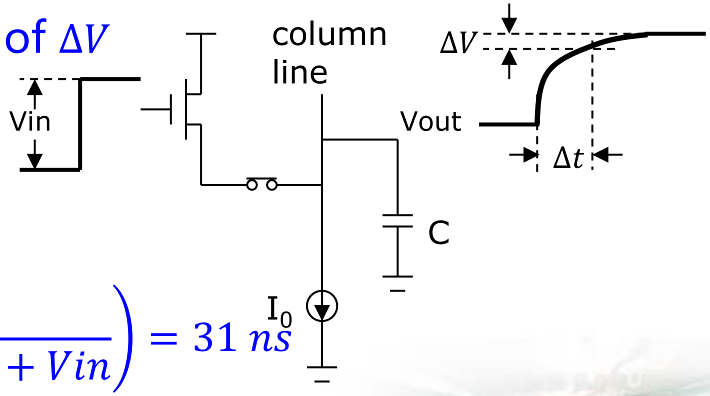
$\sigma_{position} = (p - s)/\sqrt{12}$, outside the s region

Discriminator: in-pixel vs end-of-column

- In-pixel discriminator is enabled by deep sub-micron process
  - Chosen for the CEPC R&Ds
- Benefits of in-pixel discriminator
  - Reduced power to transmit bits of 'Hit' out of matrix

    p= $CV^2 * Hit\_density = 0.2\ \mathrm{mW/cm^2}$, assumed 1 cm column line
  - Decreased digital settling time, a few to 10 ns
- End-of-column discriminator for comparison
  - Consume power to sustain the DC current I_0
  - Settling time Δt increases with the improvement of ΔV

A source follower to drive the column line



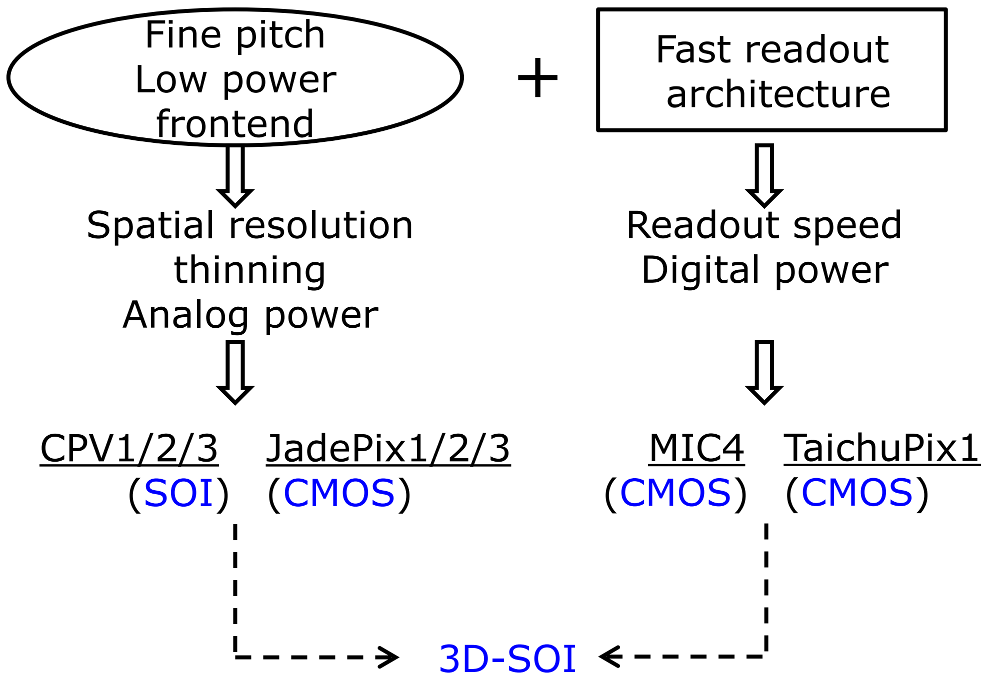
$$\Delta t = \frac{C(VGS - V_{th})}{2I_0} \ln\left(\frac{2(V_{GS} - V_{th}) + \Delta V}{\Delta V} \cdot \frac{Vin}{2(VGS - Vth) + Vin}\right) = 31\ ns$$

$assume\ VGS - \mathrm{V_{th}} = 100\ \mathrm{mV},\ Vin = 100\ mV, \Delta V = 3\ mV$

$while\ I_0 = 10\ \mu A,\ equivalent\ to\ 11\ mW/cm^2$

R&D activities on pixel sensors

- Step 1: optimized separately either for spatial resolution or for readout speed;
  - CPV1/2/3 and JadePix1/2/3
  - MIC4 and TaichuPix1
- Step 2: combine the two parts with advanced technologies
  - 3D-SOI is being pursuing



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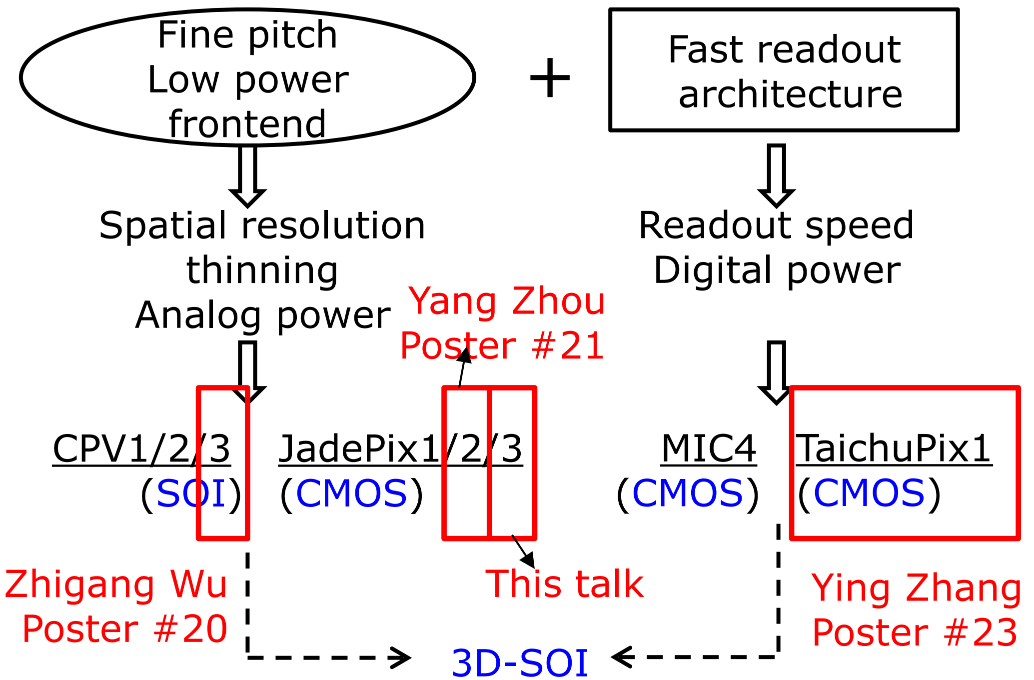
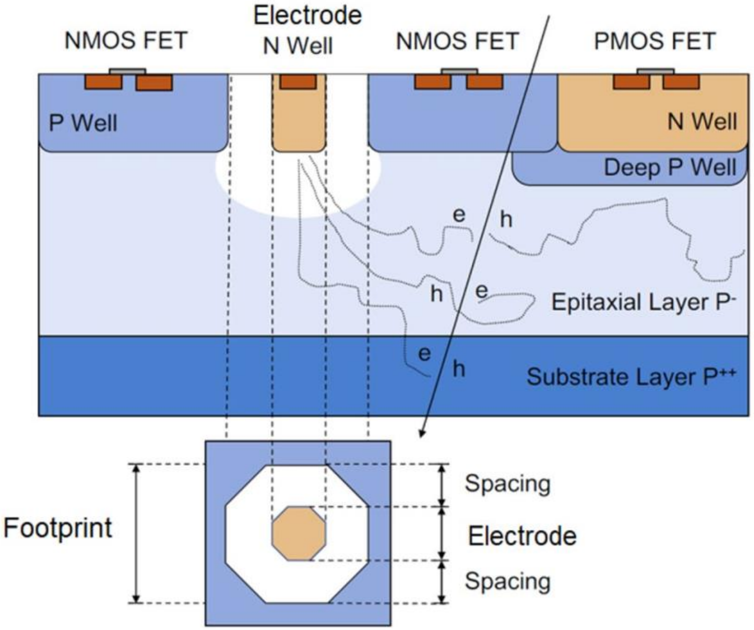


CMOS Pixel Sensor (CPS)

- TowerJazz CIS 0.18 μm process
- Quadruple well process
- Thick (~20 μm) epitaxial layer
- with high resistivity (≥1 kΩ•cm)
- Very small C_{diode} ~ a few fF



$$N \propto \frac{1}{\sqrt{g_m}} \qquad S = \frac{Q}{C}$$

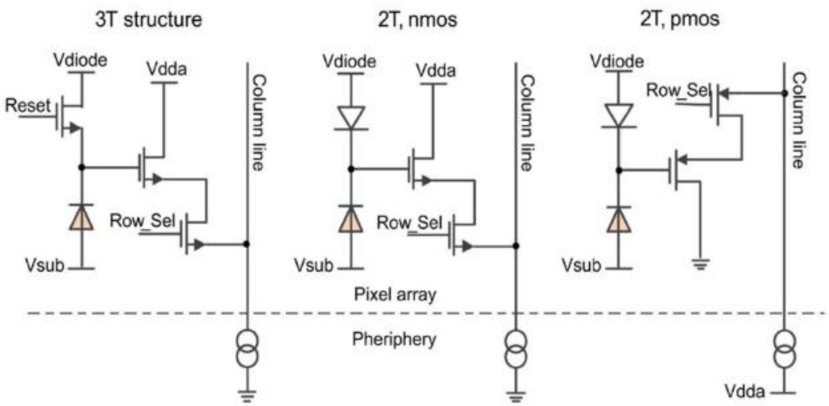
$$\frac{S}{N} \propto \frac{Q}{C}\sqrt{g_m} \propto \frac{Q}{C}\sqrt[2a]{I} \quad \Rightarrow \quad \downarrow P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a}$$

$$g_m \propto I^{\frac{1}{a}}$$

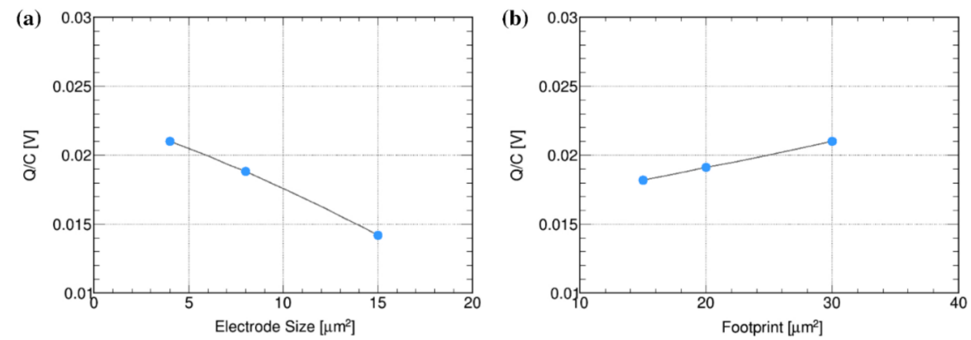
a = 2 in strong inversion
a = 1 in weak inversion

Fixing the S/N for a given bandwidth

Sensing diode verified on JadePix1



Ref: L.J.Chen, et al, RDTM (2019)

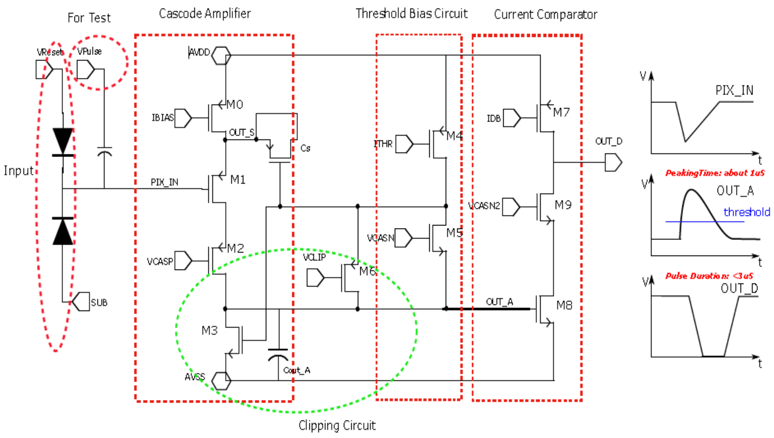


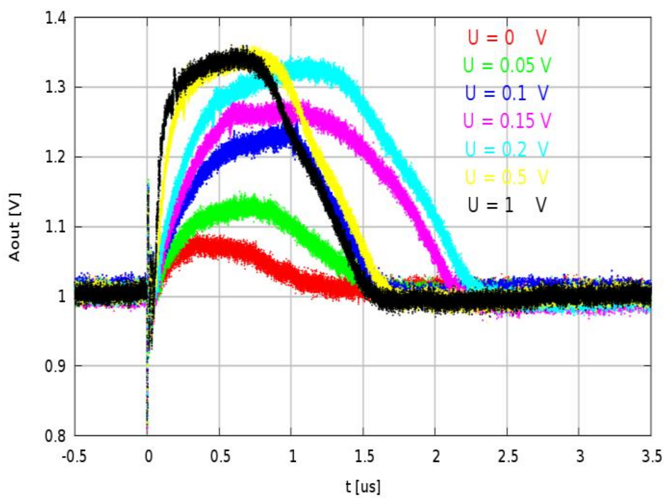
Q/C measured on JadePix1

- Sensing diode characterized on JadePix1
  - C_{diode} = 4.8 fF ~ 7.7 fF with maximum Vdiode = 1.8V
  - Essential to increase the bias voltage via V_{sub}
- Electrode size = 4 um^2 , Footprint = 36 um^2 chosen for JadePix3
  - Comprehensive considerations on the layout area, diode capacitance, and charge collection efficiency
  - V_{sub} biased negatively

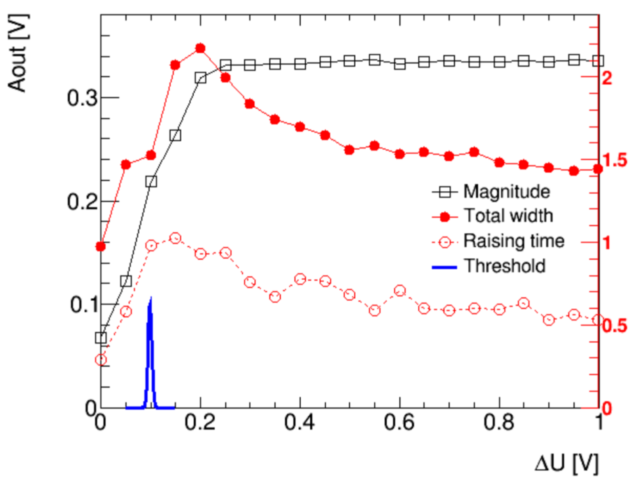
Front-end verified on MIC4

- MIC4: an ALPIDE structure optimized for fast timing
  - Peaking time < 1us
  - Pulse duration < 3us
  - Increased power to 110nW/pixel
- Measurement results:
  - Applied threshold = 99 e-
  - TN = 6 e^-, FPN = 31 e^- (< 20e^- is required)





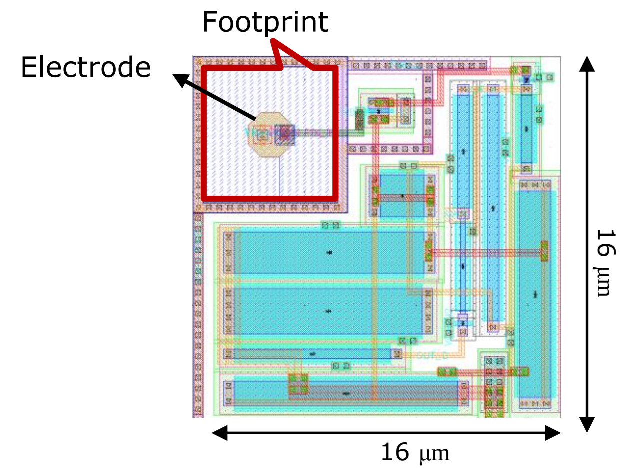
OUT_A waveform measured on MIC4

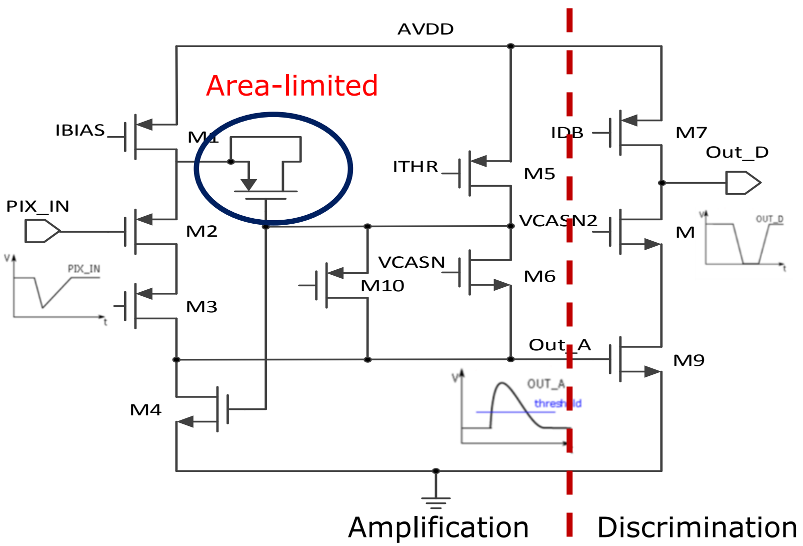


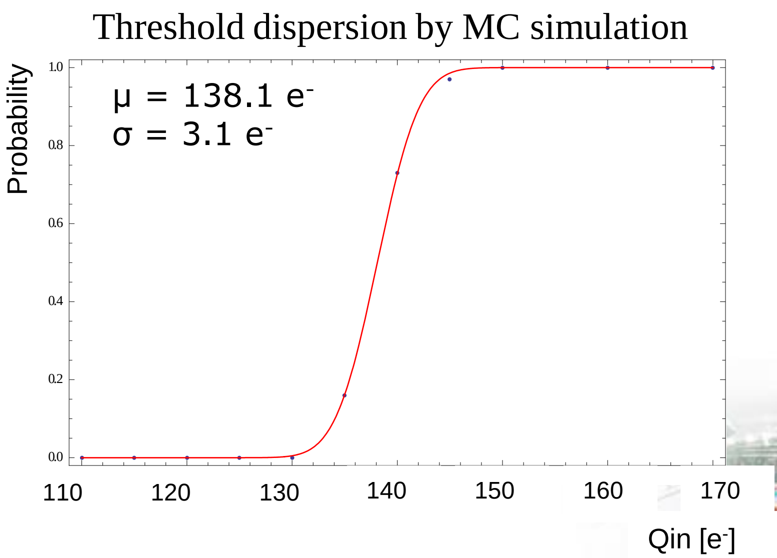
Peaking time and pulse duration

JadePix3: Diode & Front-end design

- Design goals: small pixel size and low power consumption
- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 μm^2, with a small footprint 36 μm^2
- Frontend: tradeoff between layout area and FPN
  - Reduction on the layout area, ~200 μm^2
  - Improvement on the FPN = 3.1e$^-$ (simulation)
  - A low power version (20nA), equivalent to 9 mW/cm^2

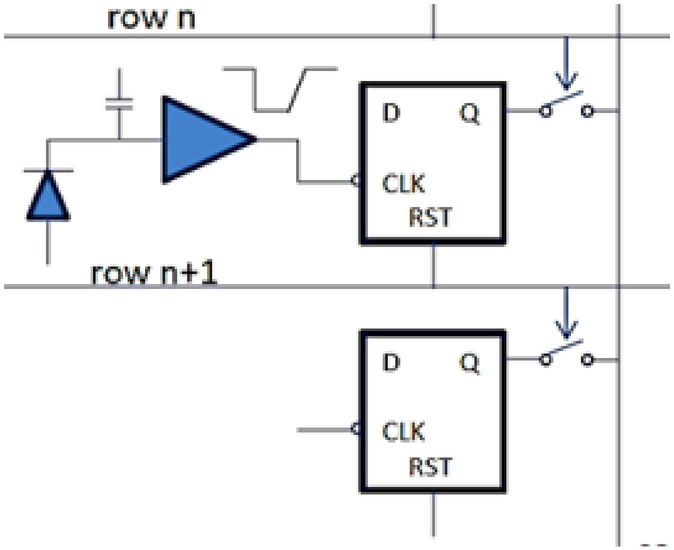


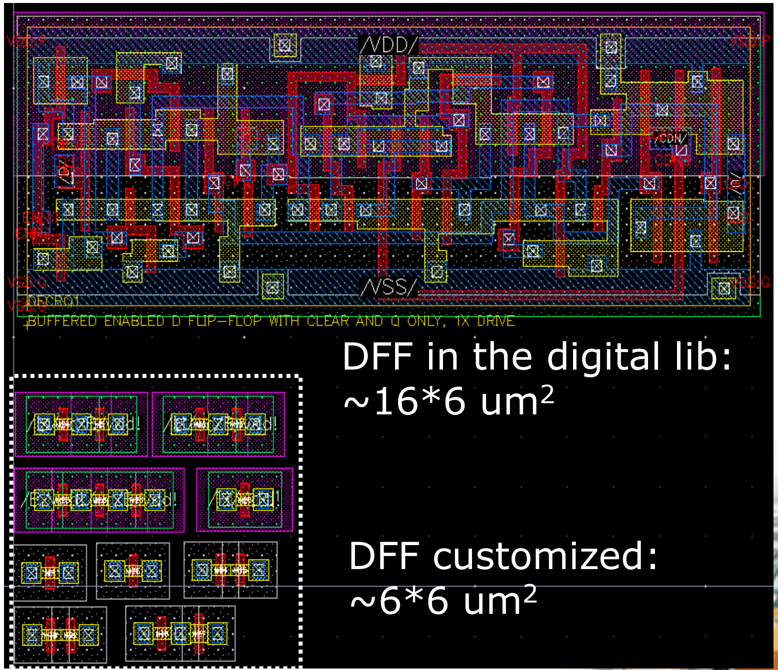




JadePix3: Customized D-FlipFlop

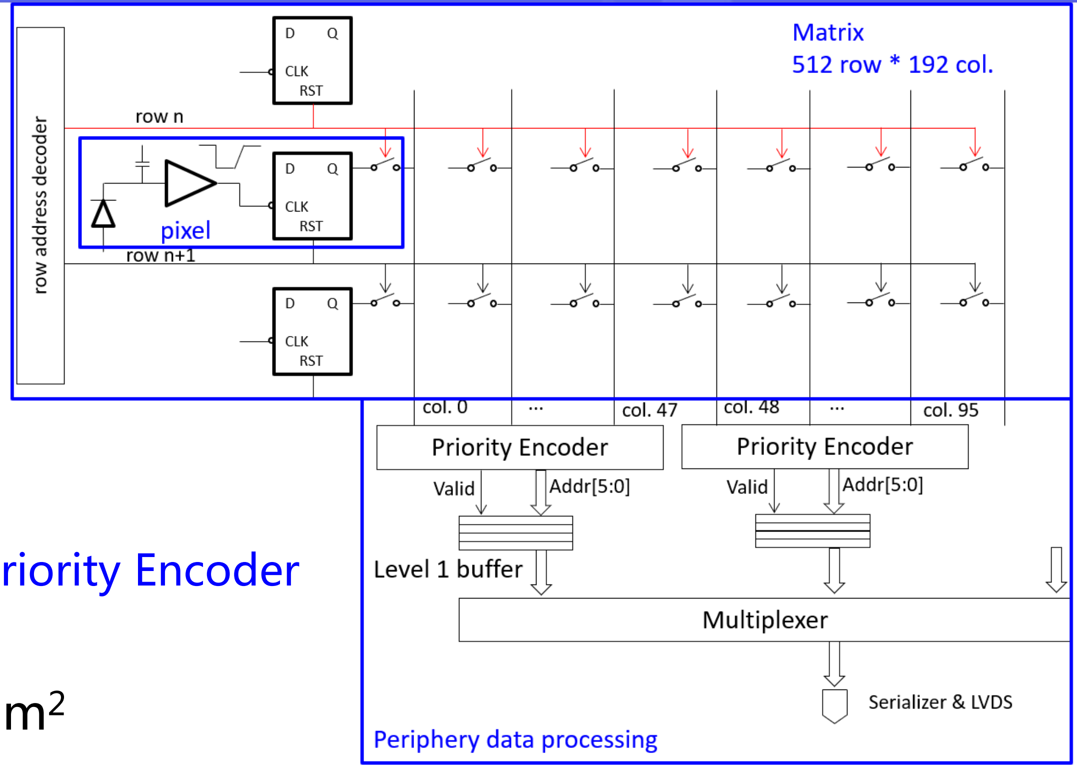
- D-FlipFlop (DFF) used to register the 'Hit' from the discriminator
  - Set to 1 by the leading (falling) edge of discriminated pulse
  - Reset to 0 by the shared row line
  - Enhanced to drive the column line (capacitive)
  - Customized design to reduce the layout area



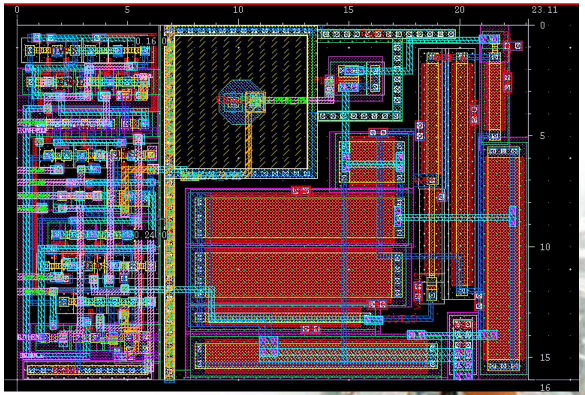


JadePix3: Rolling shutter readout of matrix

- In-pixel circuit
  - Low power binary front-end
  - Optimized DFF
- Rolling shutter readout
  - 512 row * 192 col.
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Encoder at the end of columns.
- Minimum pixel size 16× 23.11 μm²
  - 4 variants to investigate possible optimizations



Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	2 + 2 μm	FE_V0	DGT_V2	16× 23.11 μm²
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

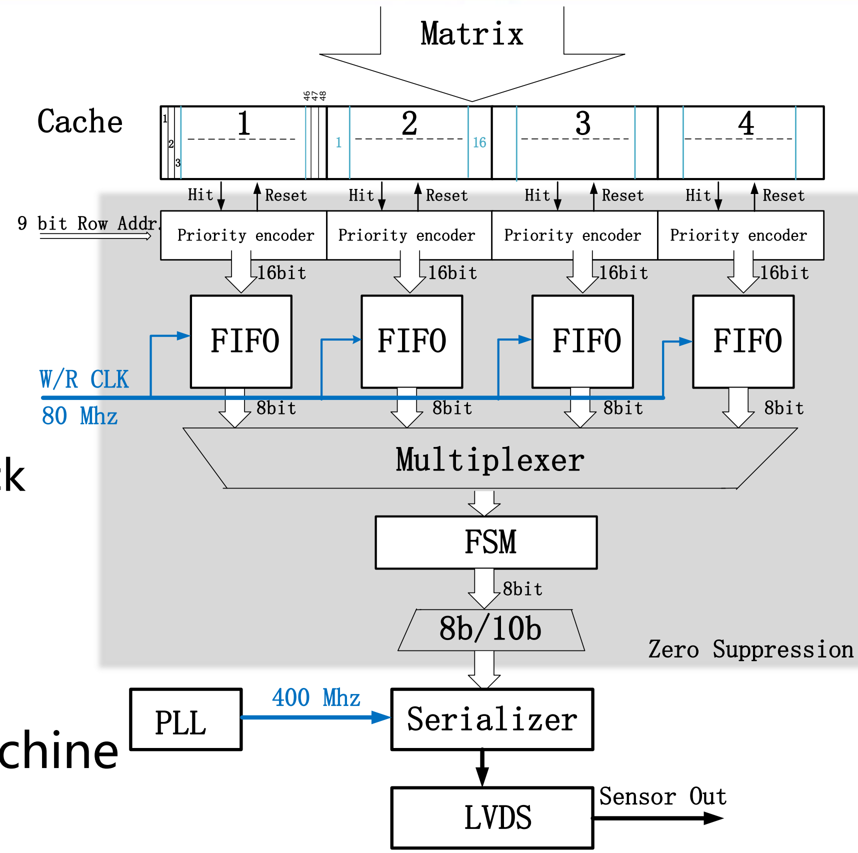


JadePix3: Periphery data processing

- Zero suppression at the end of column
  - Each 48 columns divided into 16 blocks
  - 'Fired' blocks identified sequentially by a 4-bit priority encoder
  - 12.5 ns * 16 blocks = 200 ns/row
- Only hit information fed into FIFO

Row #	Block #	hits in block
9-bit	4-bit	3-bit

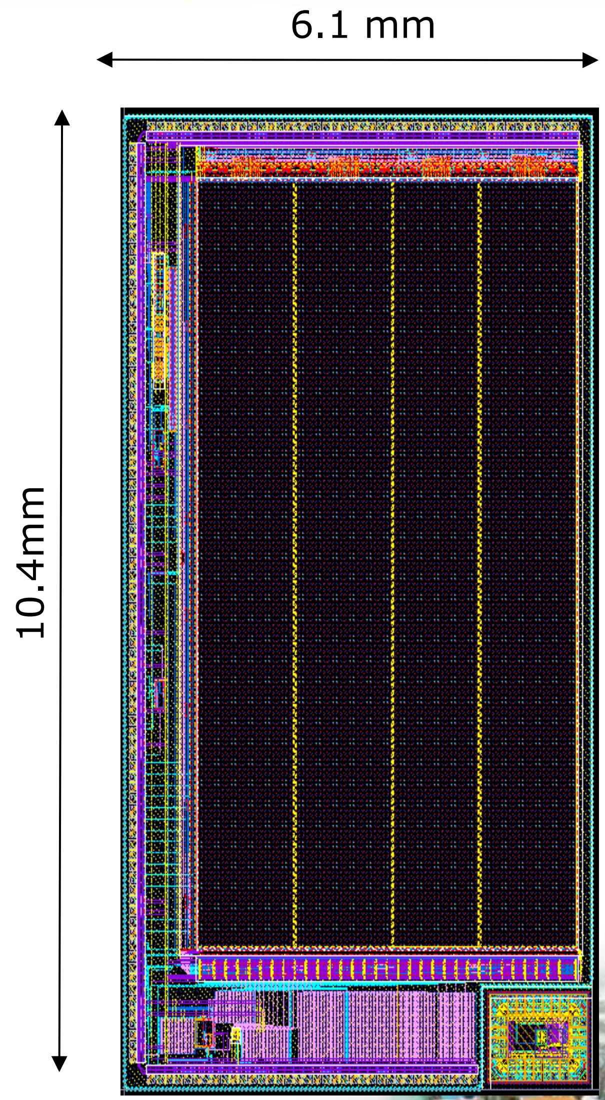
  - FIFO R/W clk: 80 MHz
  - FIFO depth: 48
- Data stream steered by a Finite State Machine
- Data after 8b/10b: 800 Mbit/s
- Estimated Power consumption 76mW
  - 15mW (Zero suppression), 25mW (Serializer), 20mW (PLL), 16mW (LVDS)



JadePix3: Status

- Submitted in Oct. 2019
  - 10.4mm * 6.1 mm
- Minimum pixel size 16× 23.11 μm^2
  - Rolling shutter readout 102 us/frame
- Estimated power consumption ~ 55 mW/cm^2
  - 9mW/cm^2 (Pixel)
  - 30mW/cm^2 (Zero suppression)
  - 6.25mW/cm^2 (Serializer)
  - 5mW/cm^2 (PLL)
  - 4mW/cm^2 (LVDS)

  } If shared by 1 * 2 cm^2 chip

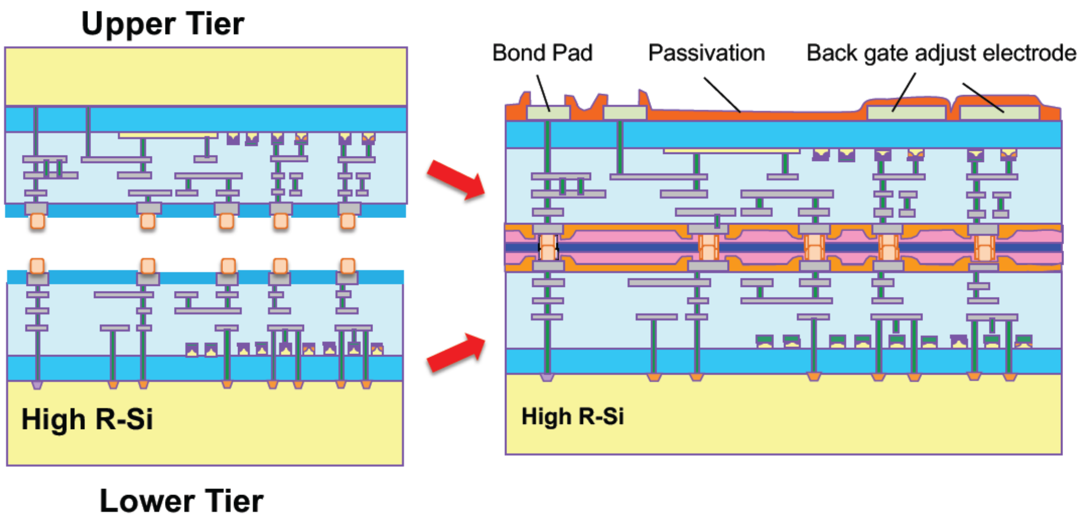


Perspectives on SOI-3D

- SOI-3D has been demonstrated by the SOFIST 3D chip for the ILC

Ref: M. Yamada, IEEE 3DIC, Oct. 8th, Sendai, Japan, 2019
& the talk by Toru Tsuboyama at the symposium.

- The lower tier can be either SOI or CMOS pixel sensor
- 3D integration can be greatly simplified by using SOI as the upper tier
  - Etching of through via
  - Removal of handle wafer
- IHEP group is to explore the potential of SOI-3D



Summary

- High resolution low power CMOS sensor is in development for the CEPC vertex
  - Minimum pixel size $16\times 23.11\ \mu m^2$
  - Estimated power consumption ~ 55 mW/cm^2
  - Rolling shutter readout 102 us/frame
- SOI-3D may bring about new design space in terms of shrinking the pixel size.

JadePix3 design team

- IHEP: Yunpeng Lu, Ying Zhang, Yang Zhou, Zhigang Wu, Qun OuYang
- CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng, Anyang Xu, Xiangming Sun
- Dalian Minzu Unv: Zhan Shi
- SDU: Liang Zhang

Thank you for your time!

Acknowledgements

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- the National Natural Science Foundation of China (11605217)
- the CAS Center for Excellence in Particle Physics (CCEPP)

- Backup slides

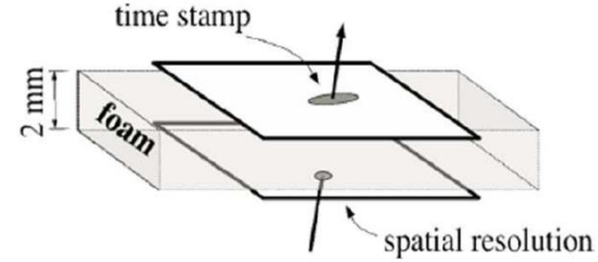
CEPC and Its Beam Timing

	Higgs	W	Z (3T)	Z (2T)
Center-of-mass energy (GeV)	240	160	91	
Number of IPs	2			
Luminosity/IP (10^{34} cm^{-2} s^{-1})	3	10	16	32
Number of years	7	1	2	
Total Integrated Luminosity (ab^{-1}) - 2 IP	5.6	2.6	8	16
Total number of particles	1×10^6	2×10^7	3×10^{11}	7×10^{11}
Bunch numbers (**Bunch spacing**)	242 (**680 ns**)	1524 (**210 ns**)	12000 (**25ns + 10% gap**)	

- Continuous colliding mode
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
- General requirements on the detector development:
  - Precise measurement, Low power, Fast readout, Radiation-hard

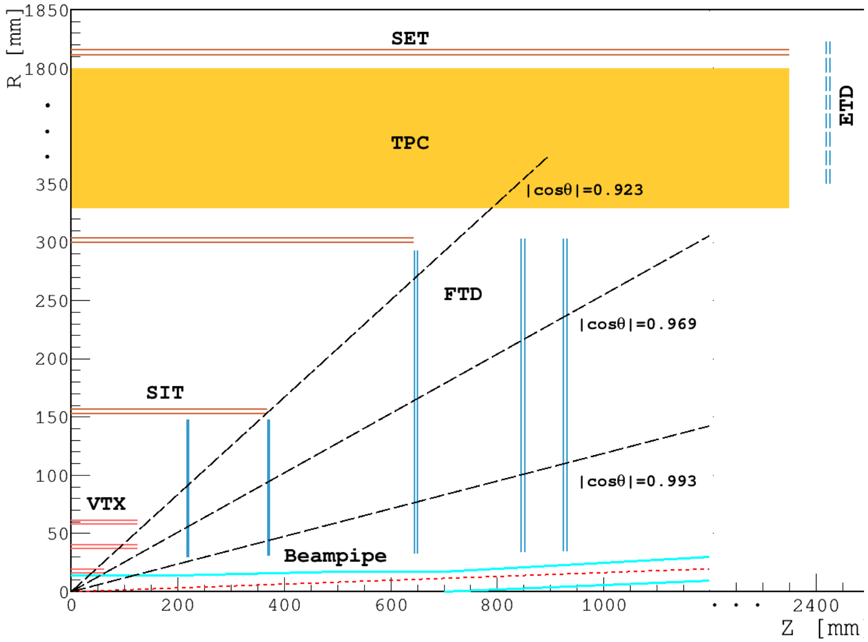
Baseline Silicon Tracker Layout

- Vertex part: 6 pixel layers in double-sided way
  - Layer 1: best s.p. resolution
  - Layer 2: very fast readout
- Tracking part: microstrip + pixel
  - SIT, SET, ETD, and 3 outer disks of FTD, ETD: single-sided strips mounted back to back
  - 2 inner disks of FTD: pixel



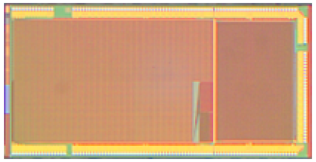
Design parameters for the Vertex

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

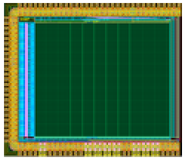


Developed CMOS Pixel Sensor prototypes for CEPC

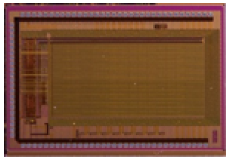
Prototype	Pixel size (μm^2)	Collection diode bias (V)	In-pixel circuit	R/O architecture	Main goals	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer, analog output	Rolling shutter	Sensor optimization	Lab. and beam test finished
JadePix2	22 × 22	< 10 V (ac-coupled)	amp., discriminator, binary output	Rolling shutter	Small pixel, Power < 100 mW/cm^2	Electrical functionality verified
MIC4	25 × 25	reverse bias	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout	Electrical functionality verified
TaiChuPix1	25 × 25	reverse bias	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout with time stamp	In measurement
JadePix3	16 × 26 16 × 23.11	reverse bias	Low power front-end, binary output	Rolling shutter with end of col. priority encoder	Small pixel, low power	In fabrication



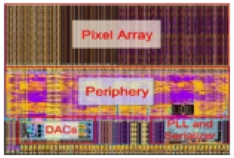
JadePix1 (IHEP)
3.9 × 7.9 mm^2



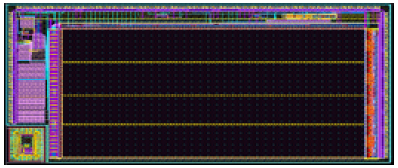
JadePix2 (IHEP)
3 × 3.3 mm^2



MIC4 (CCNU & IHEP)
3.2 × 3.7 mm^2



TaiChuPix1 (IHEP, SDU, NWPU, IFAE, CCNU)
5 × 5 mm^2



JadePix3(IHEP, CCNU, Dalian Minzu Unv., SDU)
10.4 × 6.1 mm^2

All prototypes in TowerJazz 180 nm CIS process

Beam-Induced Backgrounds (CDR)

- Detector occupancy <1%
  - assuming 10 μs readout interval, 16 um pixel pitch with a multiplicity of 9 per hit

Radiation level at the first vertex layer

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

Occupancy at the first vertex layer

	H(240)	W(160)	Z(91)
Hit density (hits $\cdot$ cm^{-2} $\cdot$ BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23