

Development of high resolution low power CMOS pixel sensor for the CEPC vertex detector

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Circular Electron Positron Collider is proposed as the future higgs factory. There are two different detector concepts and their variants being in the process of optimization. In either concepts, the vertex sub-detector is important for the flavor tagging. The relevant physics cases require high spatial resolution, low occupancy and low material budget; and the operation condition requires low power consumption and high radiation tolerance. These specifications have to compromise with each other. In particular the specifications of spatial resolution and power consumption are contradictory in terms of pixel pitch. For a spatial resolution of 3 μm , the pixel pitch needs to reach 16~18 μm . In the development of CMOS pixel sensor for the CEPC vertex, an in-pixel signal discrimination and a sparsified readout are identified as the key points for low power design, while keeping focus on the reduction of pixel pitch.

Based on the above design choices, a CMOS pixel sensor has been designed and submitted for tape-out. The pixel matrix is 512 rows by 192 columns, divided into 4 sectors with 48 columns per each sector. The vertical pitch is 16 μm for each sector, which is assumed to be the $r\phi$ direction in the vertex sub-detector. The horizontal pitch is increased to be able to accommodate the complete pixel circuit, 26 μm for sector 0, 1, 3 and 23.11 μm for sector 2 due to different configuration of circuit blocks. Hit information is scanned one row after another (rolling shutter) at 200 ns/row and then feed into the asynchronous encoders at the end of column. These encoders and associated buffers are organized for each sector independently, so that the matrix can be expanded to a full size by increasing the number of sectors in the future. Total power consumption is estimated to be < 100 mW/cm².

Submission declaration

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