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A Readout Network ASIC for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

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Among the current and planned experiments of neutrinoless double-beta decay (0νββ), the high-pressure gaseous TPC stands out for its excellent energy resolution, low radioactive background and good scalability. Moreover, high position resolution can be maintained with an appropriate charge readout scheme for TPC to further suppress the background through ionization imaging. A low noise sensor, Topmetal-S, is being developed which, even without gas gain, the energy resolution requirement could be met. Since 0νββ tracks are extended to tens of cm in high-pressure gas, Topmetal-S is designed to have a mm-sized electrode, followed by an amplifier and an ADC in the first prototype. To realize a ton-scale TPC, approximately one hundred thousand Topmetal-S need to be laid on a meter-sized plane. The greatest challenge is reliable high-density sensor readout. A distributed, self-organizing and fault-tolerance readout network ASIC is implemented and will be integrated into Topmetal-S as a router. The scheme establishes local connection between nearby sensors to form a network. Each sensor not only generates and transmits their own data, but also forwards data from nearby sensors, and data are finally received by a computer connected to the edge of the network. 2D-Mesh is chosen as the topology of the network. A distributed routing algorithm, Fault-Tolerance-XY (FT-XY), is implemented. The routing algorithm relies only on local information. The algorithm is also fault-tolerant, so that failed sensors will not disable a large section of the network. By sending fault detection packets, the computer will form a set of rectangular region called faulty blocks to contain detected faults. The FT-XY routing follows the regular XY routing until the packet reaches faulty block. Then, the packet will routed around the block to pass through. The throughput and latency of the readout network reaches 11641 Mbit/s and 120 us. The design is implemented on a 130-nm CMOS process and submitted in June 2019. The details of the routing algorithm, the fault detection scheme, the micro-architecture of the router, and preliminary test results will be presented.

Submission declaration

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