Readout demonstrator for a Large-Scale Pixel-Detector conforming to the ATLAS Phase-II Upgrade

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On behalf of the ATLAS TDAQ Collaboration

OUTLINE

ATLAS Pixel off-detector readout overview

Current status

ROD vs **FELIX** cards

Readout Evolution

RD53A-to-FELIX readout chain

Phase-I **FELIX** board

πLUP board

DAQ demonstrator

Conclusions and Future developments

Also see "ATLAS ITk Pixel Detector Overview" by Craig Buttar and…..

«Data-acquisition system developments for ATLAS pixel QA/QC test toward High Luminosity LHC» by Kazuki Todome

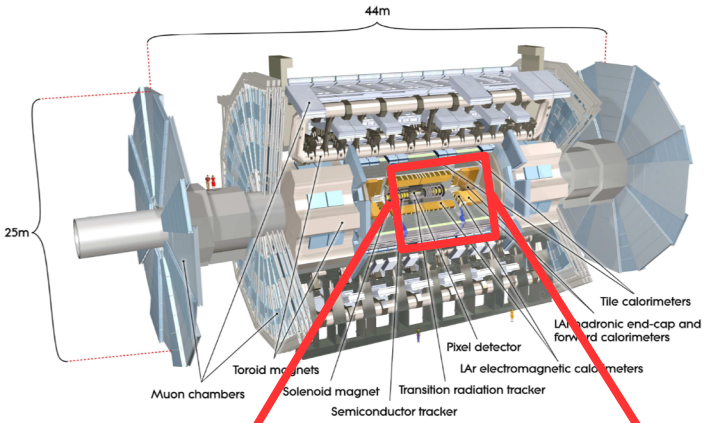
The ATLAS Pixel Detector

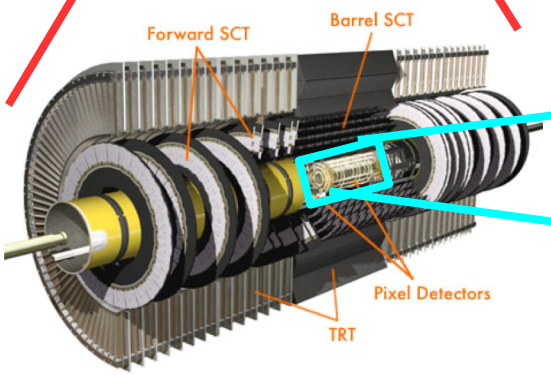
The **Pixel Detector** is the innermost sub-detector of the **ATLAS** Experiment and part of the **Tracker** (Inner Detector)

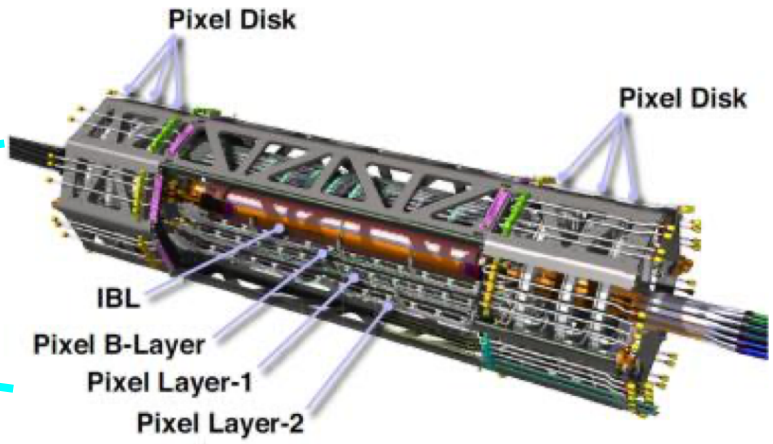
Very **critical** area!
Exposed to extremely **high dose of radiation**

Today we have **92 million** channels (pixels) altogether being read out

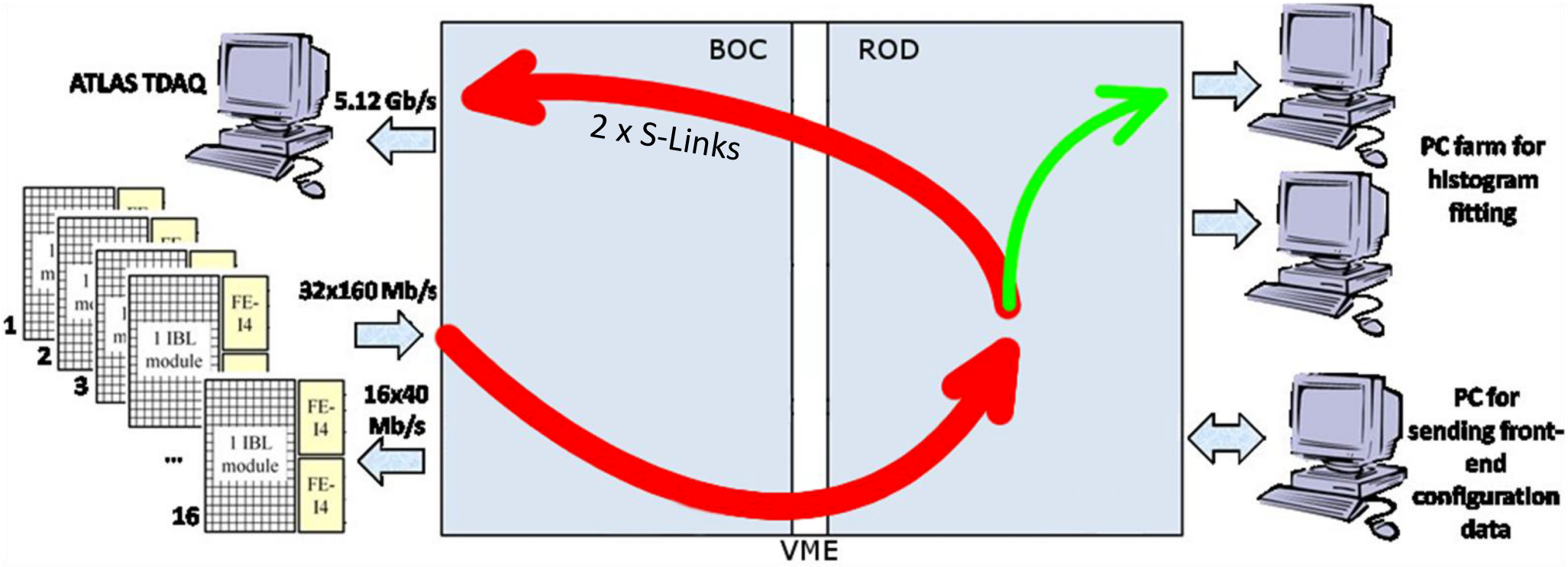
Phase-II ITK detector will consist of 9416 modules, 12.98m^2, **5 billion channels**







ATLAS Current Pixel Detector Readout
IBL/B-Layer/L1/L2/Disks - BOC ROD features



BOC	Back Of Crate
ROD	ReadOut Driver
IBL	Insertable B-Layer read out with 32 FEI4 chips (readout chips)
	FEI4 data rate up to 160 Mbps → (32 x 160 = 5.12 Gbps)

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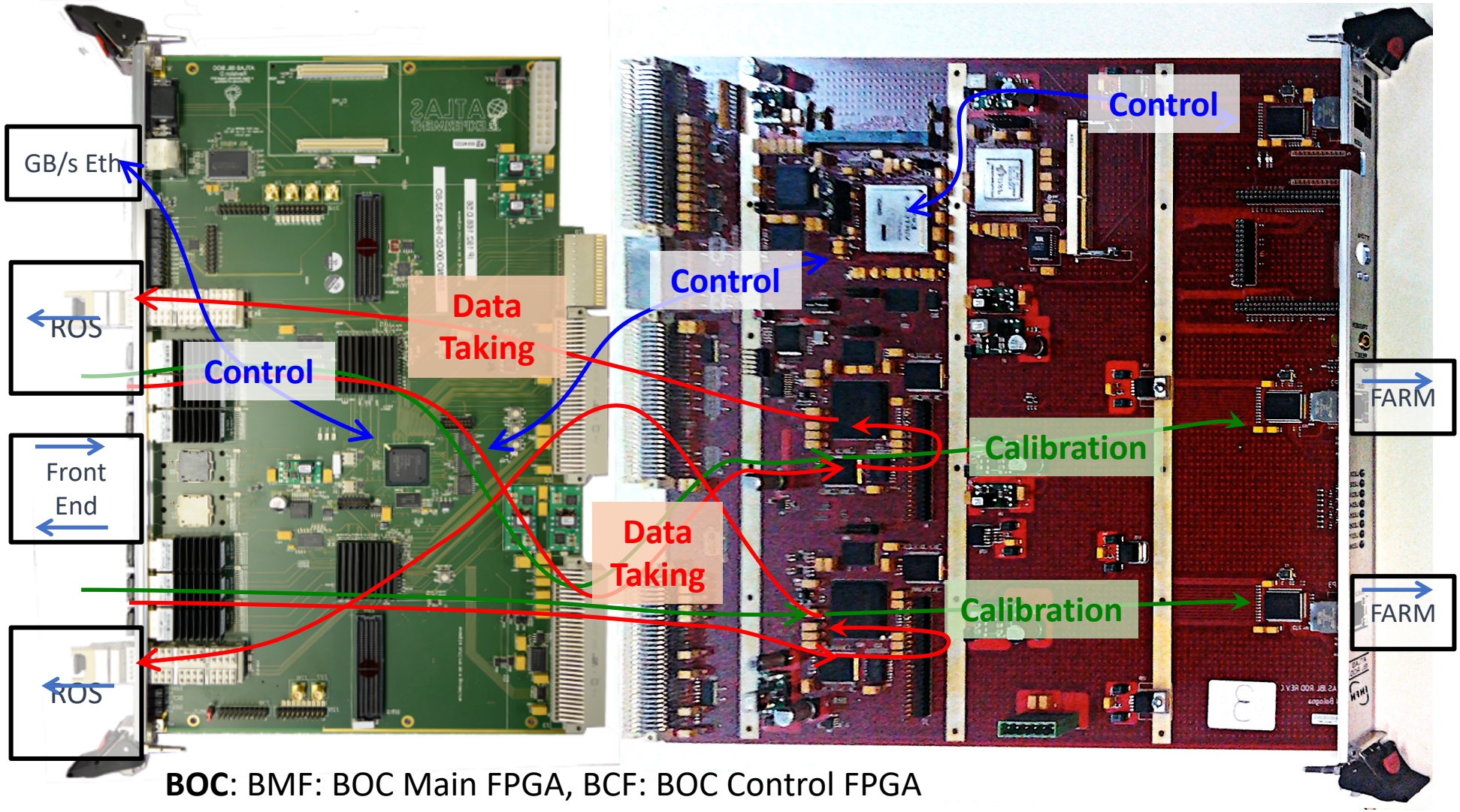
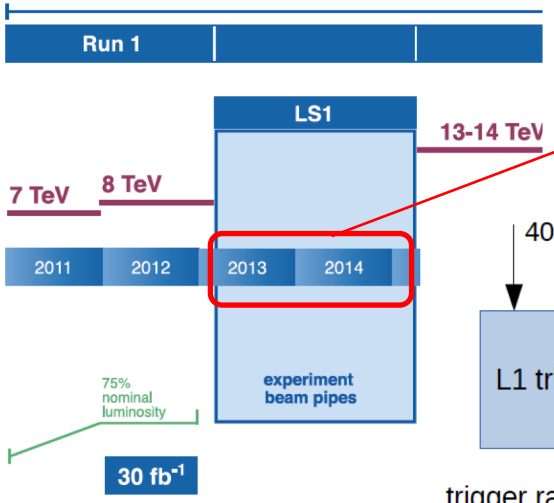
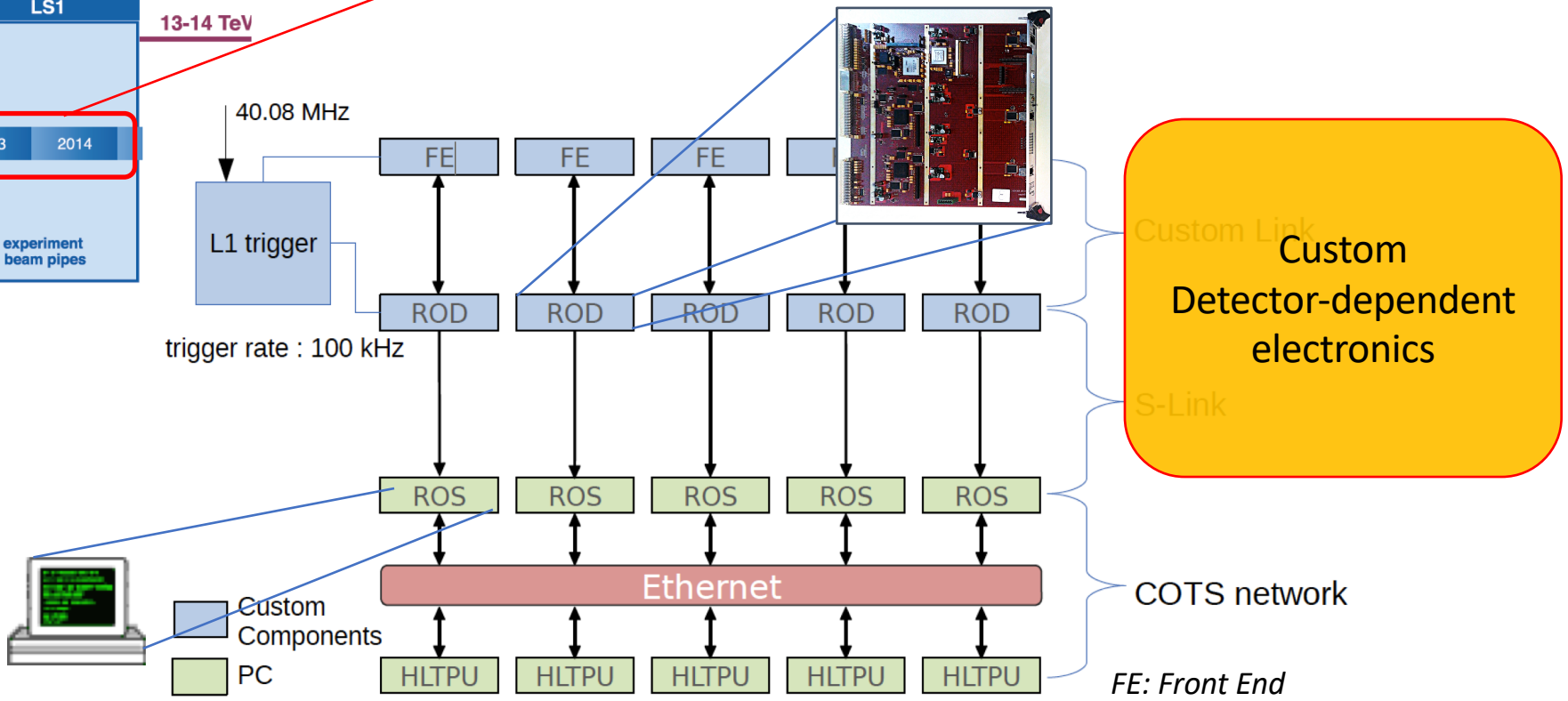


BOC: BMF: BOC Main FPGA, BCF: BOC Control FPGA

ROD: PRM: Program Reset Manager, Master and 2 x Slaves

Pixel DAQ today after Phase-0 upgrade (2017)



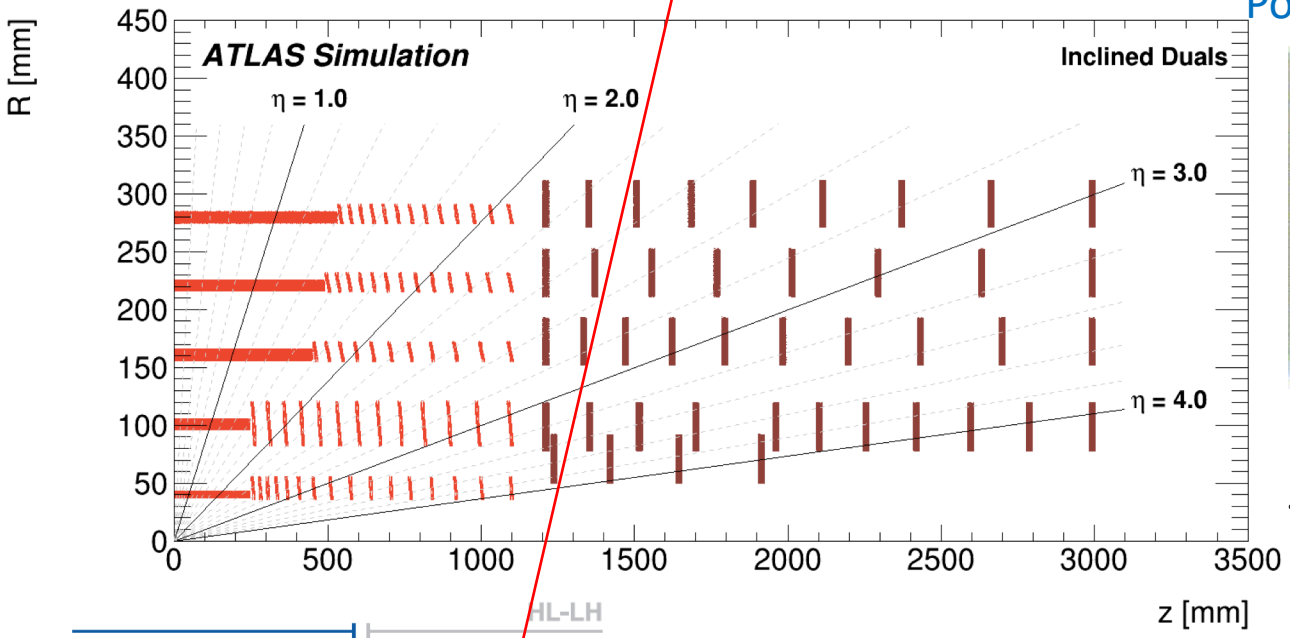


Points to be revised for the Upgrade of Phase-II

- Too much custom electronics
- Too rigid configuration (Detector Dependent)
- ROD card based on Firmware and Embedded Software

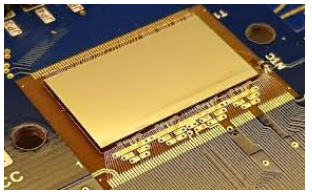
FE: Front End
ROD: ReadOut Driver
ROS: ReadOut System
HLTPU: High Level Trigger Processing Unit
COTS:Commercial Off the Shelf

Phase-II Pixel DAQ upgrade

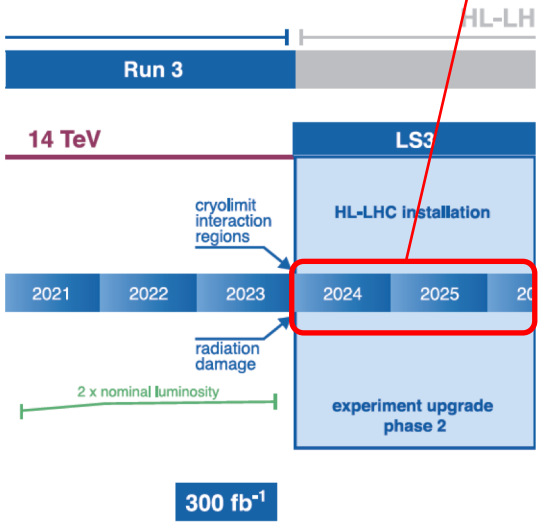


PoS(VERTEX2018)020

RD53A SCC module
and
RD53A Chip



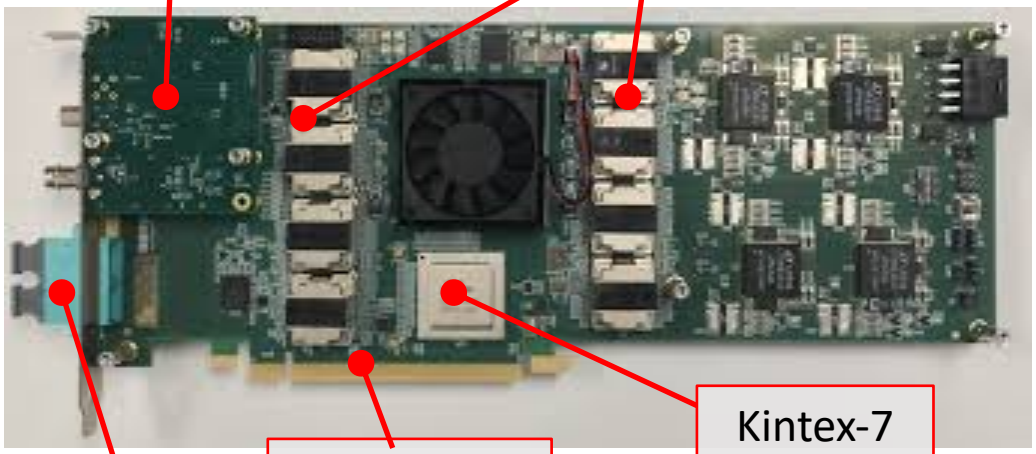
…. and RD53B will be the updated version



- Candidate Layout for the ITk pixel detector with 5 layers
- Pseudo rapidity of up to $\eta < 4$
- The expected data rates are as high as 5.12 Gbps per front-end module, over up to 4 AURORA lanes running at 1.28 Gbps per RD53B chip
- Readout carried out via FELIX cards

The The FrontEnd LInk eXchange (FELIX) readout system

https://atlas-project-felix.web.cern.ch/atlas-project-felix/



FELIX → off-detector readout system common to all the sub-detectors

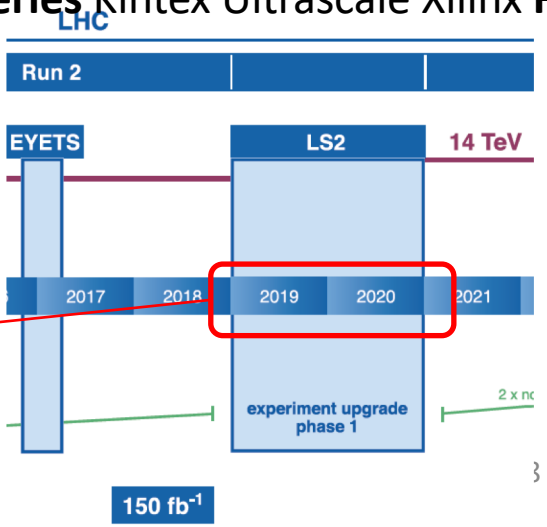
Will **replace the ATLAS RODs** during 2019-2021 **Phase-I upgrade** (partially) and during 2024-2026 **Phase-II upgrade** (completely)

Phase-II hardware design still **under investigation**

Phase-I cards under **production**

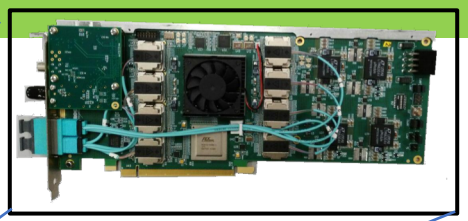
FELIX project involving several institutes

- (up to) **48 links** (optical fibers)
- **PCIe** gen 3 technology → **>100 Gbps**
- **7th series** Kintex Ultrascale Xilinx **FPGA**



Card used for Phase-I Upgrade

The FrontEnd LInk eXchange (FELIX) topology
Phase-II Configuration



40.08 MHz

FE

Custom Detector-dependent electronics

FE

L1 trigger

FELIX FELIX FELIX FELIX FELIX

Custom Links

HPC Network

D. H. D. H. D. H. D. H. D. H.

COTS network

HPC Network

Phase-0/I: ROS
Phase-II: D.H. DATA HANDLERS

HLTPU HLTPU HLTPU HLTPU HLTPU

Custom Components

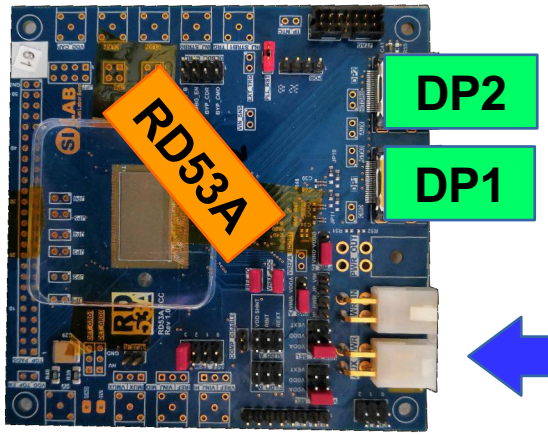
PC

✓ Custom electronics greatly reduced
✓ Previous HW tasks replaced by SW tasks

✓ FELIX **DETECTOR-INDEPENDENT**

RD53A readout demonstrator (Pixel readout chip)

Problem: current FELIX firmware not compatible with RD53A/B output data
Solution: use a **Protocol Converter** as a firmware and physical layer interface



Single Chip Card (SCC)

ELink
Aurora

Interface
GBT-elink
Aurora-Full_mode

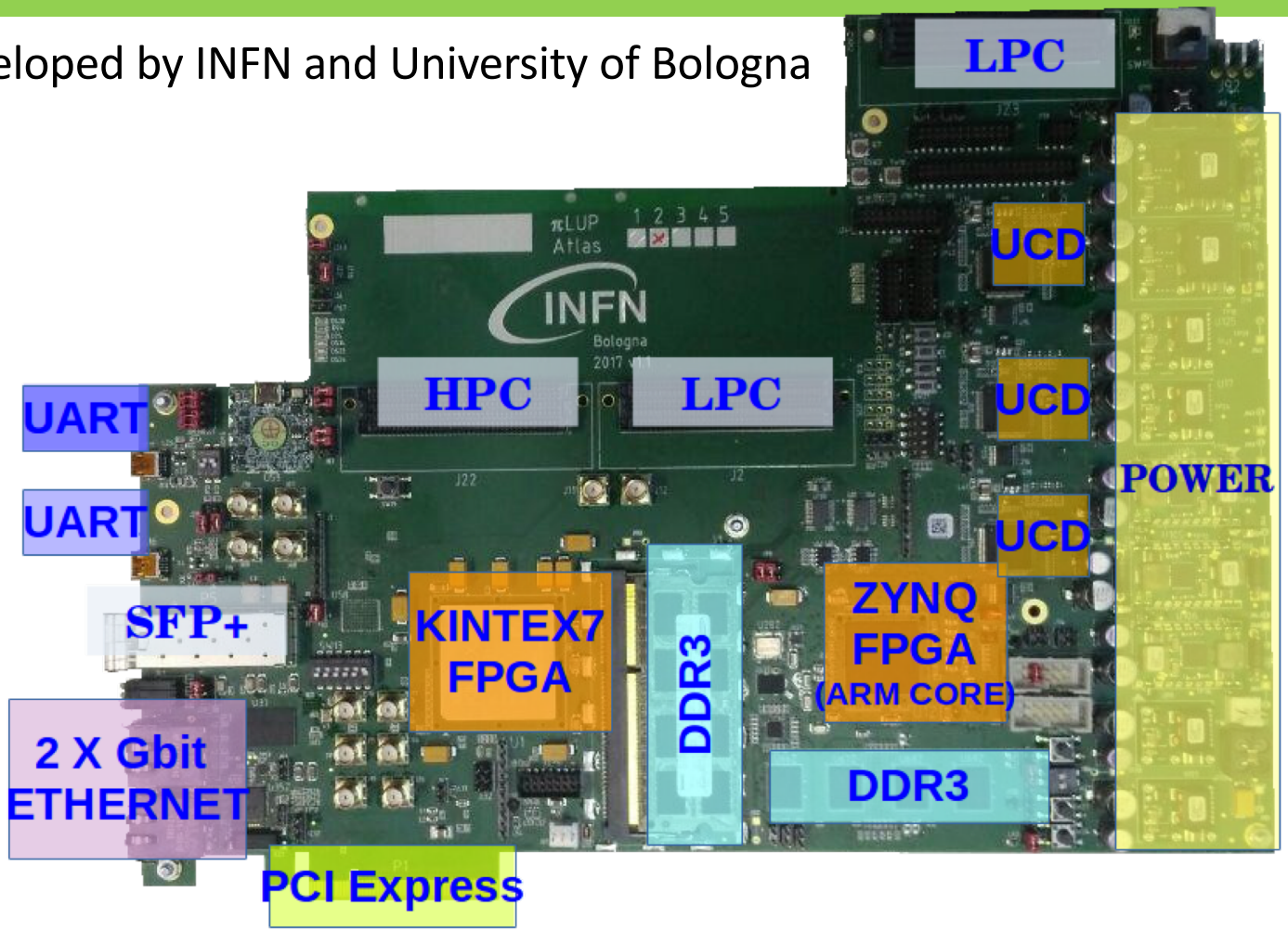
GBT
FULL_MODE

Protocol Converter πLUP board

FELIX Card (FLX712)

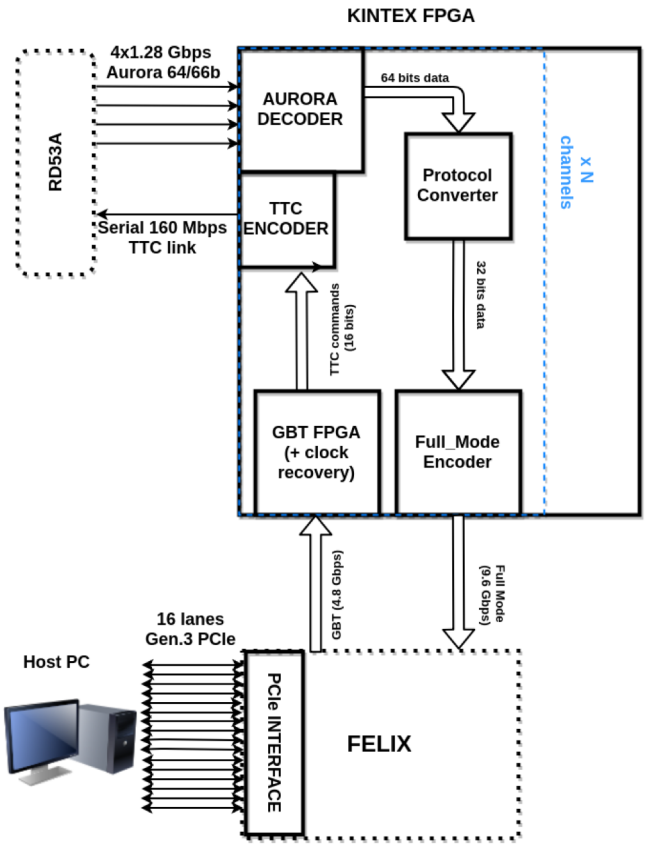
πLUP board

πLUP board developed by INFN and University of Bologna



- ✓ Two **7th series Xilinx FPGAs** in **Master-Slave** architecture
- ✓ **Embedded** ARM dual core **processor**
- ✓ **PCIe** bus → **32 Gbps**

Protocol Converter Overview



πLUP: system **interface**

FELIX: main **DAQ** board

→ **Can interface up to 4 SCC chips**

Main blocks:

- ✓ **Configuration** (FELIX → RD53A), decodes command from FELIX GBT and encodes them into RD53A compatible format
- ✓ **Data taking** (RD53A → FELIX) implemented, decodes Aurora 64/66b from SCC, merges 4 links into a single stream that is encoded into Full_mode protocol
- ✓ **Trigger generator** (if no TTC available)
- ✓ **RD53A emulator** (optional) implemented into protocol converter

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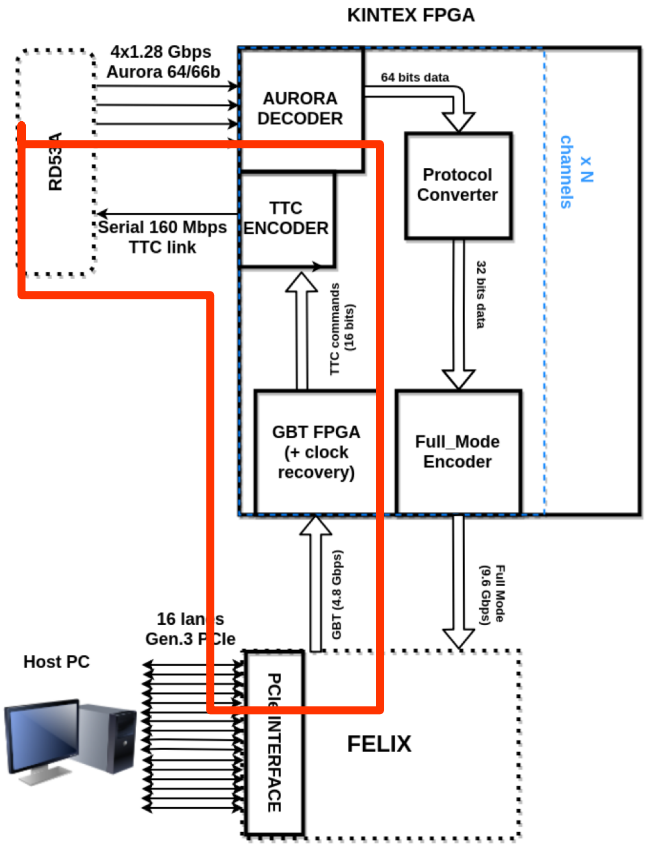

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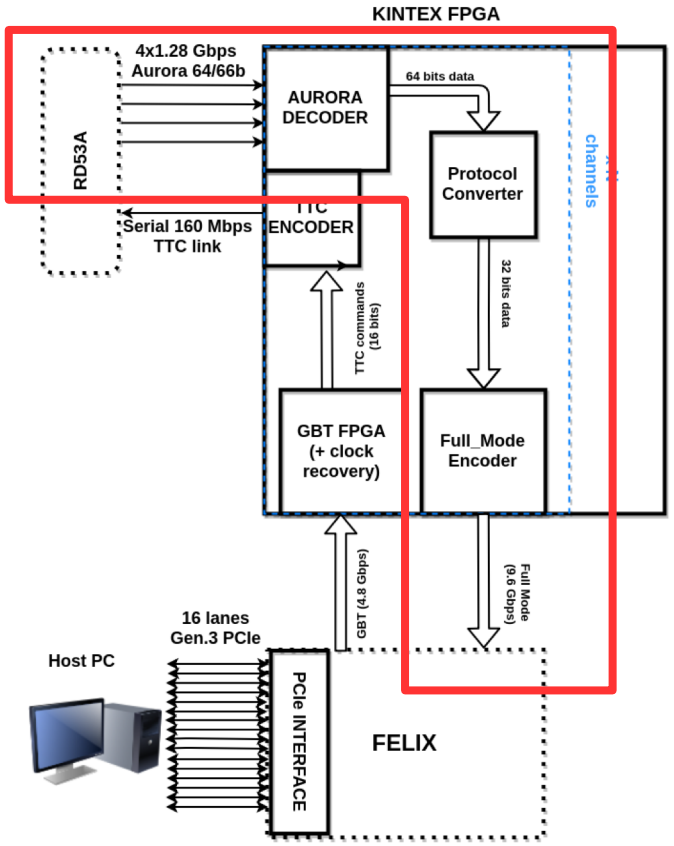

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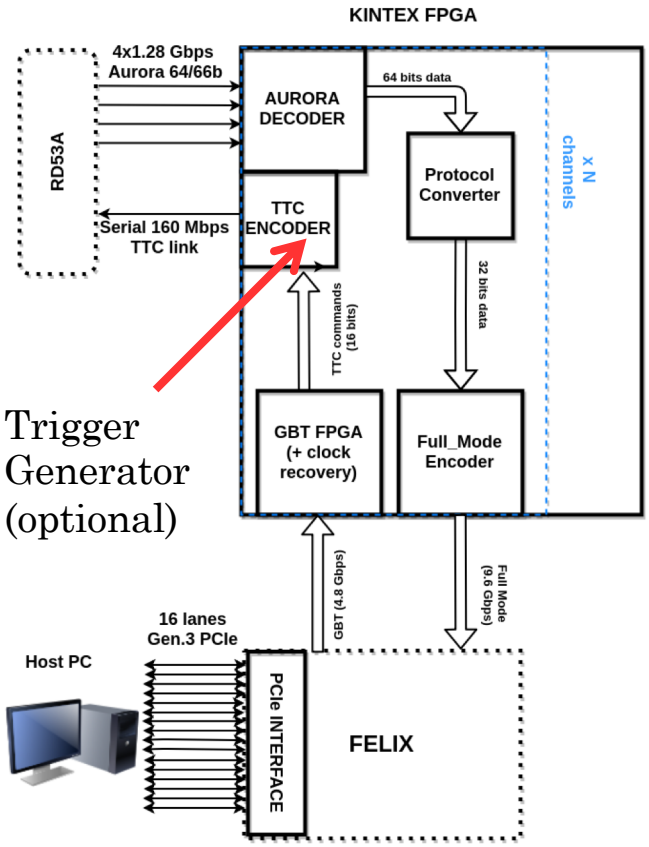

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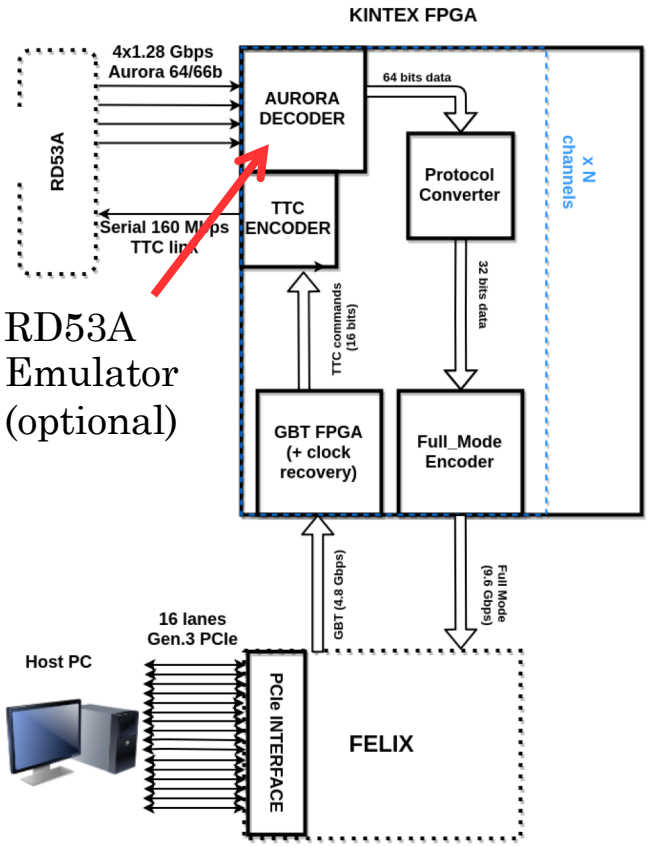

RD53A Emulator (optional)

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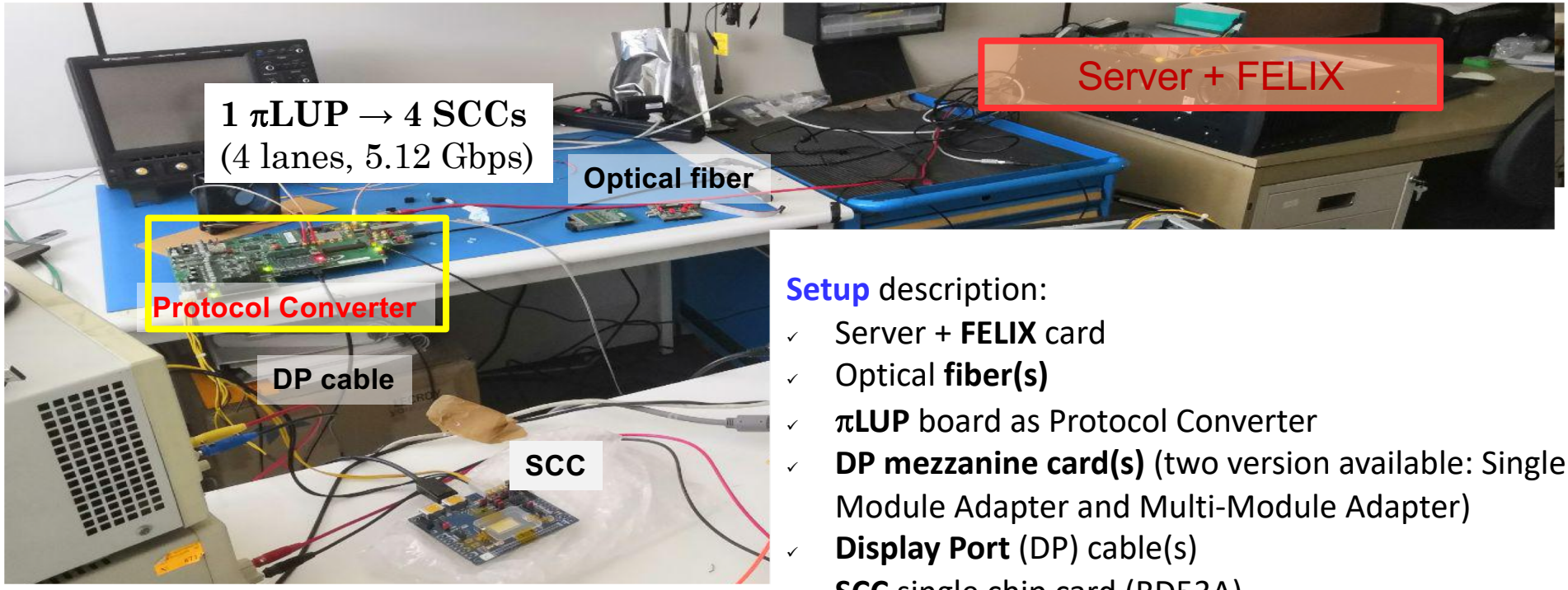
Setup Overview
System Integrated with FLX712 and RD53A



Setup description:

- ✓ Server + **FELIX** card
- ✓ Optical **fiber(s)**
- ✓ **πLUP** board as Protocol Converter
- ✓ **DP mezzanine card(s)** (two version available: Single Module Adapter and Multi-Module Adapter)
- ✓ **Display Port** (DP) cable(s)
- ✓ **SCC** single chip card (RD53A)

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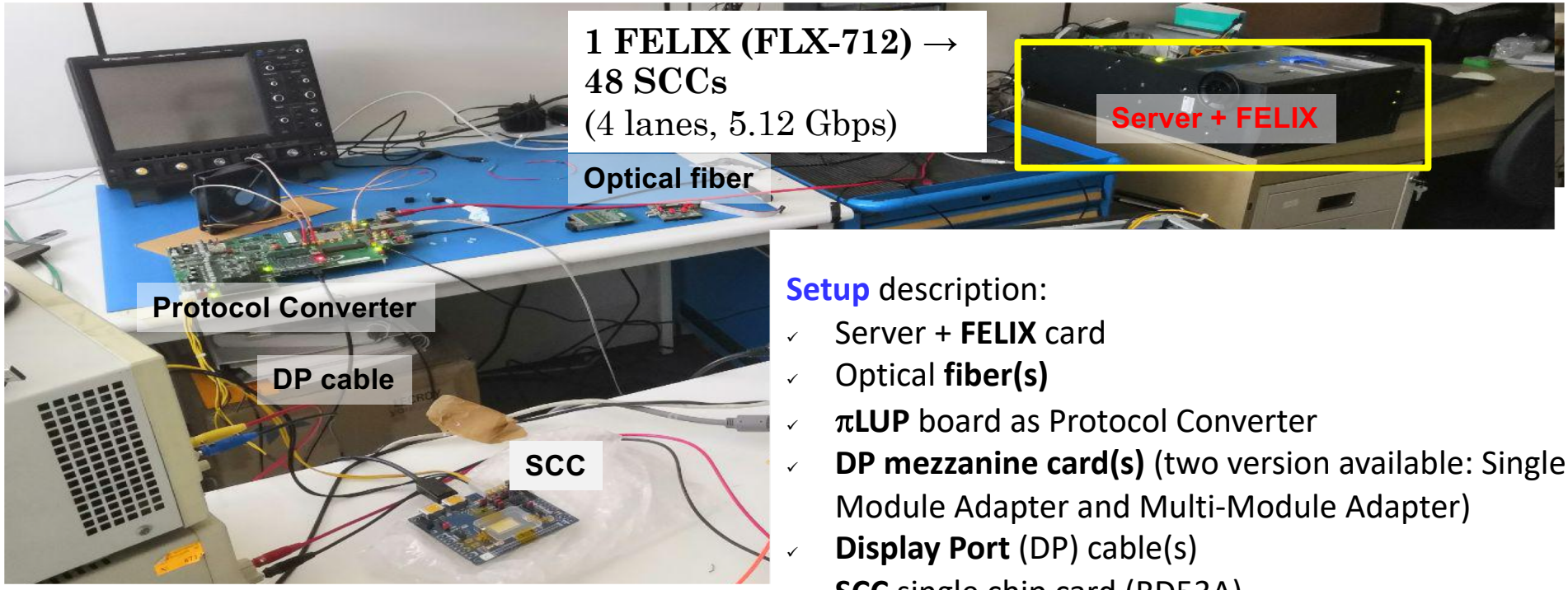

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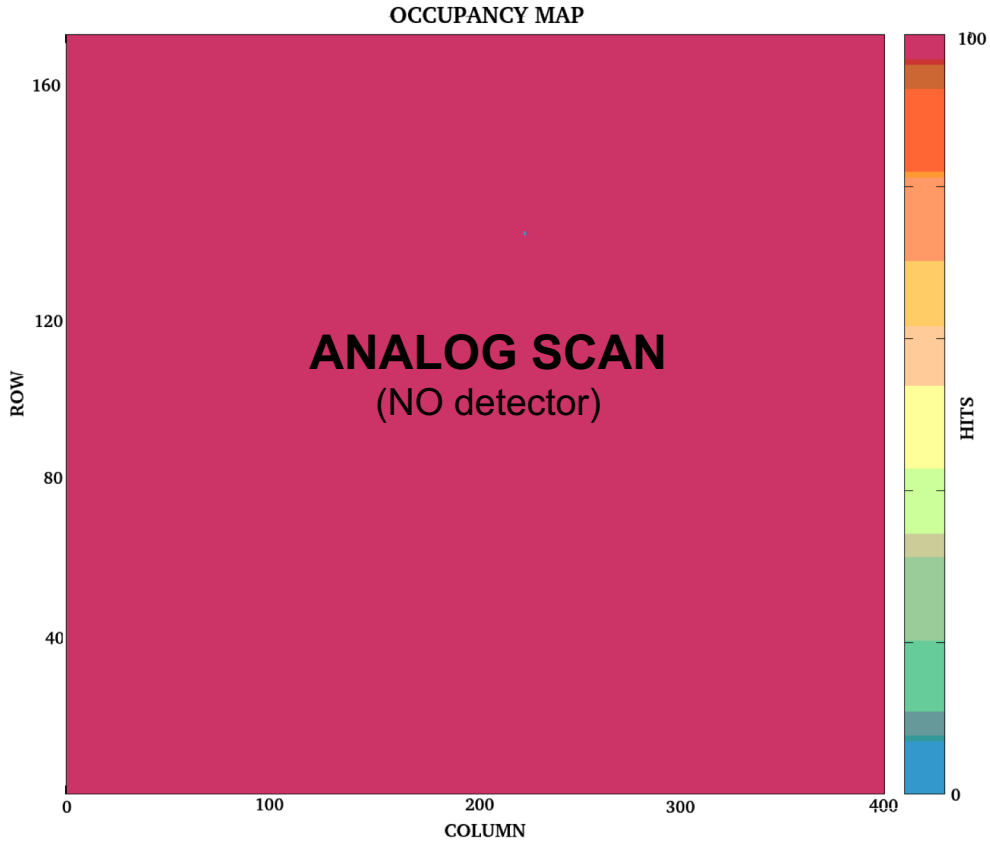
Setup at CERN

Example of an ANALOG SCAN

RD53A – πLUP – FELIX readout chain

- Up to 4 SCC chips interfaced with one πLUP
- Each SCC read out up to **4 x 1.28 = 5.12 Gbps**
- Readout software integrated with
  ITk Phase-II software
- Chip calibrations **(Digital, Analog Scans)**



Poster by Kazuki Todome
«Data-acquisition system developments for ATLAS pixel QA/QC test toward High Luminosity LHC»

Current demonstrator is a **baseline** for the **Phase-II implementation**

Conclusions

- **ATLAS Pixel Detector** fundamental to resolve particle tracks
- **Pixel Detector upgraded** to have more spatial resolution and channel density
- **Readout system to be upgraded** to face harsher environmental conditions
- **First prototype** (Front-End and readout chain) realized
  - **"Integrated"** for FELIX cards and RD53A prototypes (Demo at CERN)
- Real FE chip (**RD53B**) and **Phase-II readout system** development still **ongoing,** updated version of FELIX cards will be used