**Introduction**

Silicon pixel detectors are at the core of the detector system at the Circular Electron Positron Collider (CEPC). As the innermost part, it provides an extremely high input parameter resolution. The vertex system is crucial for the Higgs flavor physics, such as H→bb, H→cc, H→gg.

It consists of three cylindrical layers of double-sided silicon sensors and mechanical support. The spatial resolution of innermost layer should be less than 1 μm, which is very difficult to achieve when the power consumption and readout speed is also important.

Current, there are several R&D activities for CEPC vertex detectors. One is the CMOS, based on TowerJazz 0.18 μm process, the other is the SOI, based on LARS 0.12 μm FE-Soi process [1]. Comparing with the standard CMOS technology, the SOI takes advantage of fully depleted sensors, thus has a larger and faster signal response.

**Sensor: Pinned Depleted Diode (PDD)**

SOI-PDD structure is proposed by Shoji Kawahito [2] (Shizuoka U.). It has many advantages due to the multi doping layers:

- Pinned Si surface layer -> shielding layers to eliminate back gate effect and cross-talk, reduction of surface leakage by 2 orders, reduction of signal loss due to Si-Soi interface traps
- Depleted charge collection electrode -> reduction of diode capacitance
- Lateral electric field -> improved charge collection efficiency

Several complex ring structures placed in area of 10’’x10’’ μm²:

- Standard PDD structure
- Modify distance between BNW1 and BPW1 from 1 μm to 2 μm
- Remove BPW2 and BNW2 -> optimization of charge sharing effect
- Optimization of diode capacitance and bias
- In-pixel circuit

Even though SOI sensor has a 3 times larger signal than standard CMOS sensor, we still need a low noise in-pixel circuit to obtain a low threshold and better resolution performance. The baseline in-pixel circuit consists of:

- Common source amplifier as 1st stage
- DC gain: 13, 1 μA consumed only when the row is read out (static power consumption)
- Forced to initial state after readout by a pair of complementary reset transistors
- Correlated Double Sampling (CDS) to reduce ATC noise
- Cascade amplifier as 2nd stage with its active load shared on the column line
- 4 μA consumed only when pixel is fired and read output power consumption
- Intrinsinc threshold 525 mV, adjustable by Vclamp
- Rolling shutter mode (200μm/μs, < 1% duty cycle)

**Diode capacitance and bias**

- Key issue of this PDD structure: relative large diode capacitance dominated by cap between BNW1 and BPW1
- At least ~4V between BNW1 and BPW1 to gain a cap lower than 4 F
- Traditional solution: apply negative VBB2 at BPW1, this voltage cannot exceed ~2 V otherwise the circuit above won’t work
- Our solution: apply positive VPOS at BNW1 and the diode is ac-coupled with in-pixel circuit

**In-pixel circuit**

A 3-Transistor source follower used to read out the PDD sensing node:

- Large dynamic range to characterize the PDD structure
- CS-stage of the amplifier replaced by a cascode stage
- To optimize the miller effect and to improve the CVF
- To compensate to have a DC gain ~30 for a proper dynamic range
- Optimized the size of PD transistor (as the active load)
- Discriminator replaced with a source follower for analog output

**Preliminary test results**

- Meassurement results:
  - Apply Vbias of 2.5V, Vclamp of ~ 4V
  - M2: 1.2 μA, very small, due to the PDD structure
  - Leakage current coming from peripheral dominates (frame voltage = 10 V)
  - Leakage current coming from bw dominates (high voltage = 10 V)
  - Leakage current coming from bw can be suppressed by improving Vclamp

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**References**


**Statistical properties**

- 2% loss of signal over 100 μs integration time
- Readout current around 100 μA (pixel thanks to the PDD structure)

**Design goal**

- To mitigate the miller effect and to improve the CVF
- To compensate to have a DC gain ~30 for a proper dynamic range
- Optimized the size of PD transistor (as the active load)
- Discriminator replaced with a source follower for analog output

**SOI-PDD structure**

- Chip area: 6’’x4’’, sensor area: 4’’x4’’
- Pixel area: 1020 μm² to gain a high resolution
- Pixel array: 2400 pixels, include analog and digital
- In-pixel discriminator and 3T analog readout in the different diode and circuit design

**CPV2**

- W/L = 2.4/0.2 μm for the input Tr. of 2nd stage
- W/L = 0.63/0.2 μm for the input Tr. of 1st stage
- Process variation added to the HSPICE model and qualified with CPV2 results

- Statiscal simulation, FPN = 12 e-

- W/L = 2.4/0.2 μm for the input Tr. of 2nd stage
- W/L = 0.63/0.2 μm for the input Tr. of 1st stage
- Process variation added to the HSPICE model and qualified with CPV2 results

- Excessive FPN has been an issue in CPV2 design

- Temporal Noise (TN)

- 70% of integrated signal current

- |signal – bias| / signal

- Data collection for 1 hour with and without source

- Different diode and circuit design

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