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# A novel SOI-PDD design for the CEPC vertex detector

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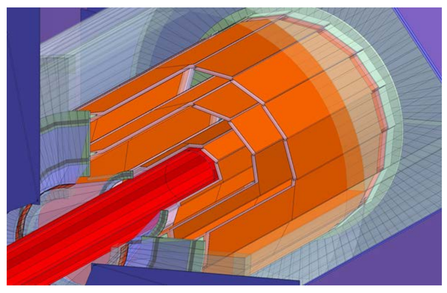
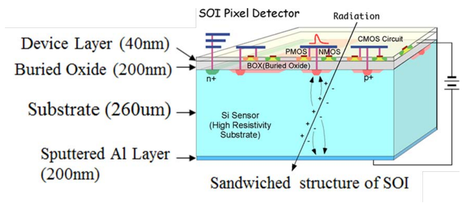
## Introduction



Silicon pixel detectors are at the core of the detector system at the Circular Electron Positron Collider (CEPC). As the innermost part, it provides a extremely high impact parameter resolution. The vertex system is crucial for the Higgs flavor physics, such as H->bb, cc, gg.

It consists of three cylindrical layers of double-sided silicon sensors and mechanical support. The spatial resolution of innermost layer should be less than 3 μm, which is very difficult to achieve when the power consumption and readout speed is also important.

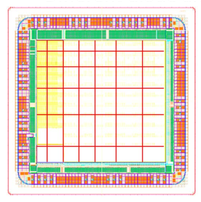
Currently, there are several R&D activities for CEPC vertex detectors. One is the CMOS, based on TowerJazz CIS 0.18 μm process, the other is the SOI, based on LAPIS 0.2 μm FD-SOI process [1]. Comparing with the standard CMOS technology, the SOI takes advantage of fully depleted sensors, thus has a larger and faster signal response.




Based on SOI technology, we developed Compact Pixel for Vertex 3 (CPV3). The design goal is to study new PDD sensor structure, explore low noise in-pixel circuit and realize a spatial resolution below 3 μm.

CPV3:

- Chip area: 6*6 mm$^2$, sensitive area: 4*4 mm$^2$
- Pixel area: 16*20 μm$^2$ to gain a high resolution
- Pixel array: 240*200, include analog and digital
- In-pixel discriminator and 3T analog readout
- Different diode and circuit design



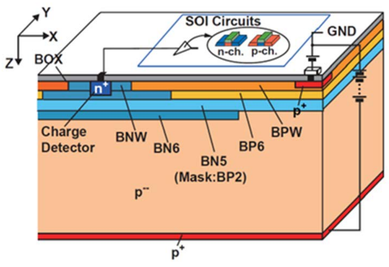
## Sensor: Pinned Depleted Diode (PDD)

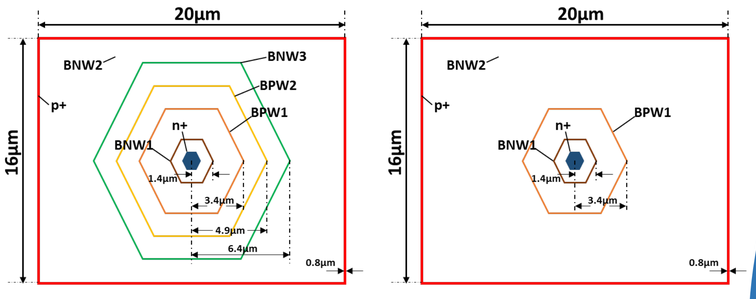
SOI-PDD structure is proposed by Shoji Kawahito [2] (Shizuoka U.). It has many advantages due to the multi doping layers:

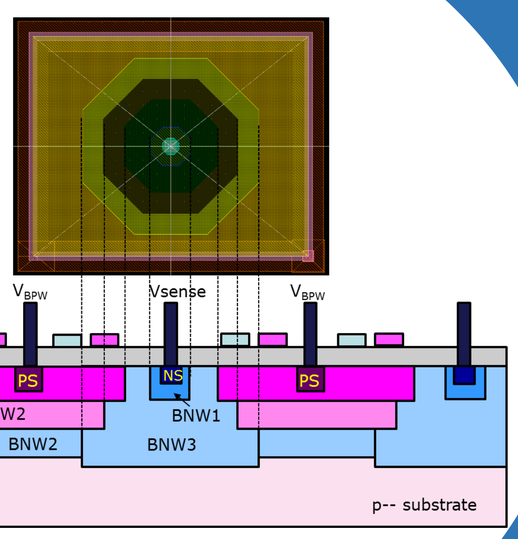
- Pinned Si surface layer -> shielding layers to eliminate back-gate effect and cross-talk, reduction of surface leakage by 2 orders, reduction of signal loss due to Si-$SiO_2$ Interface traps
- Depleted charge collection electrode -> reduction of diode capacitance
- Lateral electric field -> improved charge collection efficiency

Several complex ring structures placed in area of 16*20 μm$^2$:

- Standard PDD structure
- Modify distance between BNW1 and BPW1 from 1 μm to 2 μm -> optimization of diode capacitance
- Remove BPW2 and BNW3 -> optimization of charge sharing effect

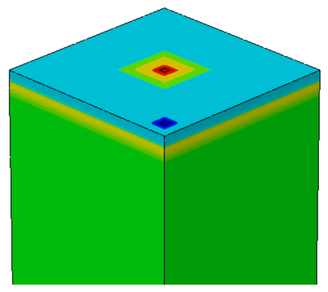


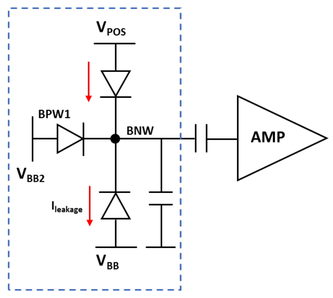



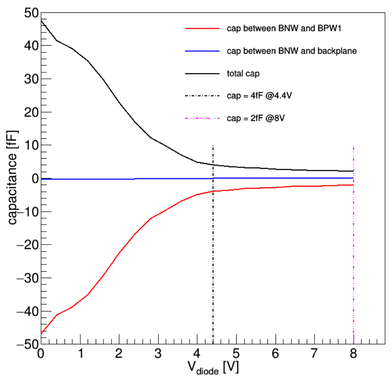

## Diode capacitance and bias

- Key issue of this PDD structure: relative large diode capacitance dominated by cap between BNW1 and BPW1
- At least +4V between BNW1 and BPW1 to gain a cap less than 4 fF
- Tradition solution: apply negative $V_{BB2}$ at BPW1, this voltage cannot exceed -2V otherwise the circuit above it won't work
- Our solution: apply positive $V_{POS}$ at BNW1 and the diode is ac-coupling with in-pixel circuit
- Advantages: larger $V_{bias}$ -> smaller $C_d$, $C_d$ decreases from 4 fF to 2 fF if $V_{bias}$ increases from +4V to +8V, MIM capacitor to allow Vbias up to +10V



2% loss of signal over 100 μs integration time
Leakage current around 100 fA/pixel thanks to the PDD structure

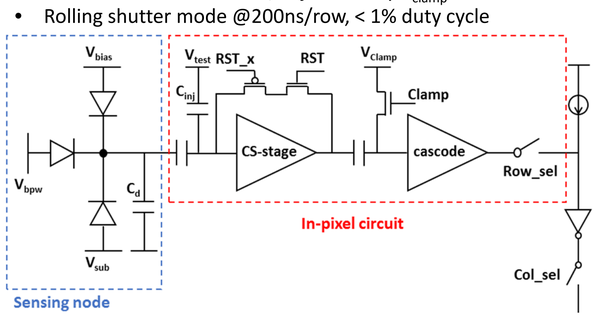


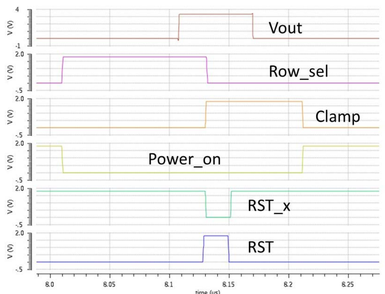




## In-pixel circuit

Even though SOI sensor has a 3 times larger signal than standard CMOS sensor, we still need a low noise in-pixel circuit to obtain a low threshold and better resolution performance. The baseline in-pixel circuit consists of:

- Common source amplifier as 1st stage
- DC gain ~13, 1 μA consumed only when the row is read out (static power consumption)
- Forced to initial state after readout by a pair of complementary reset transistors
- $C_{inj}$ = 0.27 fF for electrical pulse test
- Correlated Double Sampling (CDS) to reduce KTC noise
- Cascode amplifier as 2nd stage with its active load shared on the column line
- 4 μA consumed only when pixel is fired and read out(dynamic power consumption)
- Intrinsic threshold 525mV, adjustable by $V_{clamp}$
- Rolling shutter mode @200ns/row, < 1% duty cycle



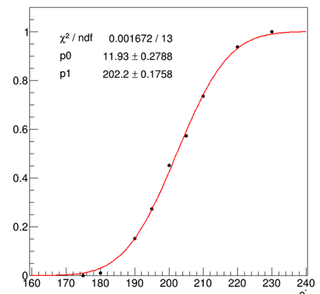




Temporal Noise (TN)

- Shot noise is negligible due to low leakage current
- Thermal noise is the dominant component
- 6 e$^-$ achieved on CPV2 design [3]

Fixed Pattern Noise (FPN)

- Excessive FPN has been an issue in CPV2 design
- W/L = 0.63/0.2 μm for the input Tr. of 1st stage
- W/L = 2.4/0.2 μm for the input Tr. of 2nd stage
- Process variation added to the HSPICE model and qualified with CPV2 results
- Statistical simulation, FPN = 12 e$^-$



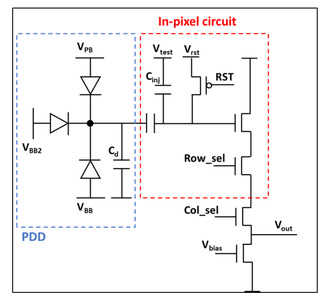

A 3-Transistor source follower used to read out the PDD sensing node

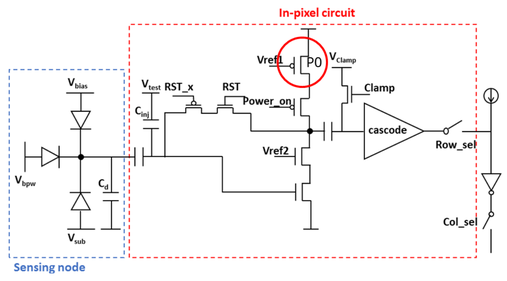
- Large dynamic range to characterize the PDD sensor

CS-stage of the amplifier replaced by a cascode stage

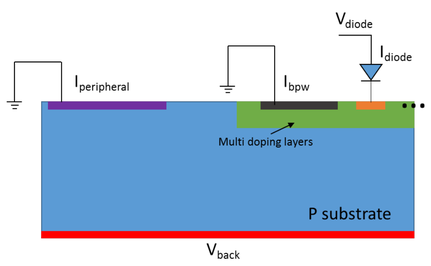
- To mitigate the miller effect and to improve the CVF
- Carefully tuned to have a DC gain < 30 (for a proper dynamic range)
- Optimized the size of P0 Transistor (as the active load)

Discriminator replaced with a source follower for analog output




## Preliminary test results

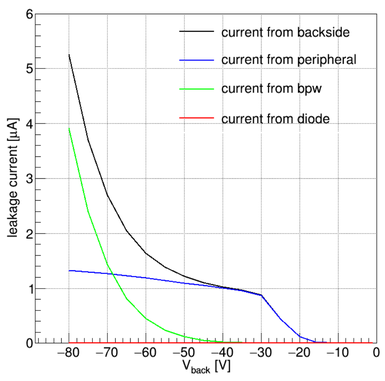


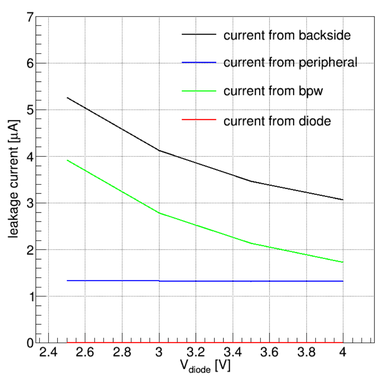

I-V measurements:

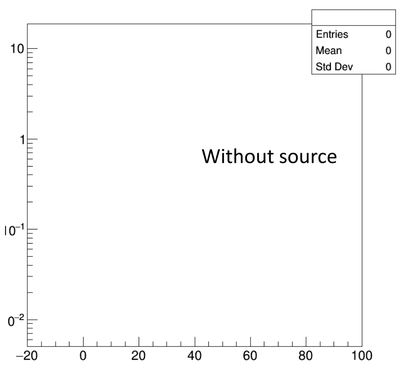
- Apply $V_{diode}$ = 2.5V, $V_{bpw}$ = $V_{peripheral}$ = 0V
- $I_{diode}$ ≈ 0, very small, due to the PDD structure
- Leakage current coming from peripheral dominates @low voltage (<70V)
- Leakage current coming from bpw dominates @high voltage (>70V)
- Leakage current coming from bpw can be suppressed by improving $V_{diode}$

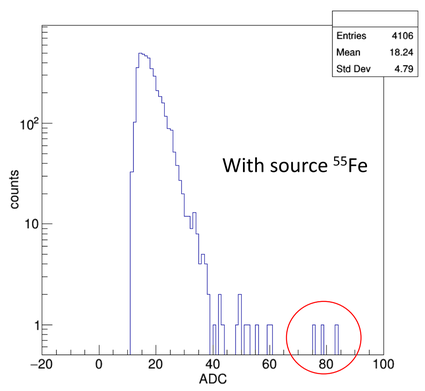
$^{55}$Fe source measurements:

- 5.9KeV X-ray measured by 3T circuit
- Data collection for 1 hour with and without source
- |signal – residual| > 10σ as cut condition
- No signals for experiment w/o source
- Clear signal for experiment with source
- Very low counting rate due to the low-level source, not fully depleted sensor and backside illumination
- This will be solved by applying a high-level $^{55}$Fe source
- $C_{diode}$ = 5fF if 5.9KeV energy => 80 ADC, expected from simulation




## Acknowledgements

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## References

[1] Y. Arai et al., Development of SOI pixel process technology, in: 7th International Hiroshima Symposium on the Development and Application of Semiconductor Tracking Detectors, Nucl. Instrum. Methods Phys. Res. A 636 (1, Supplement) (2011) S31– S36.

[2] Kamehama H, Kawahito S, Shrestha S, et al. A low-noise X-ray astronomical silicon-on-insulator pixel detector using a pinned depleted diode structure[J]. Sensors, 2018, 18(1): 27.

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