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A novel Pinned Depleted Diode design for the CEPC vertex detector

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The Circular Electron Positron Collider (CEPC) has been proposed in China as a Higgs and/or Z factory. Pixel sensors with high spatial resolution, low material budget and low power consumption are required for the inner most layer of vertex detector. As a part of R&D activities, a prototype of SOI pixel sensor with a novel Pinned Depleted Diode (PDD) design has been developed accordingly, to explore the small pixel pitch and low noise level.

The PDD structure has the same feature as the Double-SOI does, which realizes the shielding between the sensing node and electric circuit. Besides, the PDD structure has the advantages of very low leaking current and very high charge collection efficiency. However, due to the large area of shielding layer adjoining the sensing node, it suffers from large diode capacitance. A TCAD simulation has shown that at least -4V biased voltage must be applied between sensing node and shielding layer to maintain the capacitance below 6fF. On the other hand, the shielding layer cannot be connected to a very low voltage, as this will cause the circuit to work improperly. A traditional solution is adding -2V to the shielding layer and using HV_PMOS (3.3V) as the signal input transistor. In this way, at most -6V can be biased. A novel bias method is adopted in our design. We add the positive voltage to the sensing node through a diode and the signal is ac-coupled with the frond-end circuit. By using this structure, a biased voltage as low as -10V may be applied to achieve much small diode capacitance.

As for the in-pixel circuit, on one hand, a traditional 3T structure is chosen for the test of sensor performance. On the other hand, a complex circuit including amplifier, CDS and discriminator is developed to explore the low noise frond-end circuit. The characterization of sensor and circuit will soon be performed in the lab and experimental results will be presented in our report.

Submission declaration

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